

54LS83A/DM54LS83A/DM74LS83A 4-Bit Binary Adders with Fast Carry

General Description

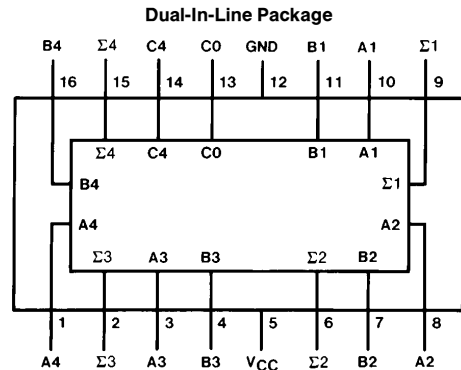
These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
 - Two 8-bit words 25 ns
 - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS83A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



TL/F/6378-1

Order Number 54LS83ADMQB, 54LS83AFMQB,
DM54LS83AJ, DM54LS83AW, DM74LS83AWM or DM74LS83AN
See NS Package Number J16A, M16B, N16E or W16A

54LS83A/DM54LS83A/DM74LS83A 4-Bit Binary Adders with Fast Carry

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS83A			DM74LS83A			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	DM54	2.5	3.4	V
			DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min	DM54		0.25	V
			DM74		0.35	
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25	0.4
I _I	Input Current @ Max Input Voltage	V _{CC} = Max V _I = 7V	A or B		0.2	mA
			C0		0.1	
I _{IH}	High Level Input Current	V _{CC} = Max V _I = 2.7V	A or B		40	μA
			C0		20	
I _{IL}	Low Level Input Current	V _{CC} = Max V _I = 0.4V	A or B		-0.8	mA
			C0		-0.4	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	-20	-100	mA
			DM74	-20	-100	
I _{CC1}	Supply Current	V _{CC} = Max (Note 3)		19	34	mA
I _{CC2}	Supply Current	V _{CC} = Max (Note 4)		22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 1$ or $\Sigma 2$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 1$ or $\Sigma 2$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 3$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 3$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 4$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 4$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to C4		17		26	ns

Truth Table

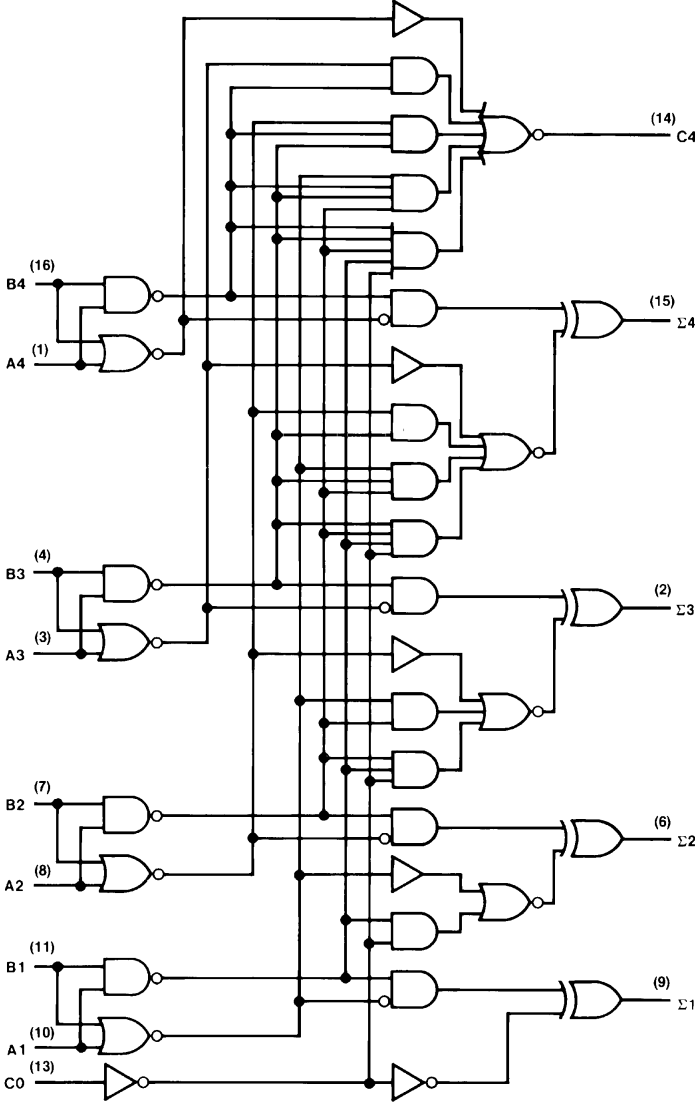
Inputs								Outputs											
								When C0 = L				When C0 = H							
				When C2 = L				When C2 = H											
A1	A3	B1	B3	A2	A4	B2	B4	$\Sigma 1$	$\Sigma 3$	$\Sigma 2$	$\Sigma 4$	C2	C4	$\Sigma 1$	$\Sigma 3$	$\Sigma 2$	$\Sigma 4$	C2	C4
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	H	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	H	H	L	L	L
H	H	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	L	L	L
L	L	H	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	L
H	L	H	L	L	L	L	L	H	H	H	L	L	L	L	L	L	L	L	H
L	H	H	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	H
L	L	L	L	H	L	H	L	L	H	H	L	L	L	H	H	H	L	L	L
H	L	L	L	H	H	H	L	H	L	H	L	L	L	L	H	H	L	L	H
L	H	H	L	H	H	H	L	L	L	L	L	L	L	L	L	H	L	L	H
H	L	H	H	H	H	H	L	H	L	L	L	L	L	L	L	H	L	L	H
H	H	H	H	H	H	H	L	L	H	H	L	L	L	H	H	H	L	L	H

H = High Level, L = Low Level

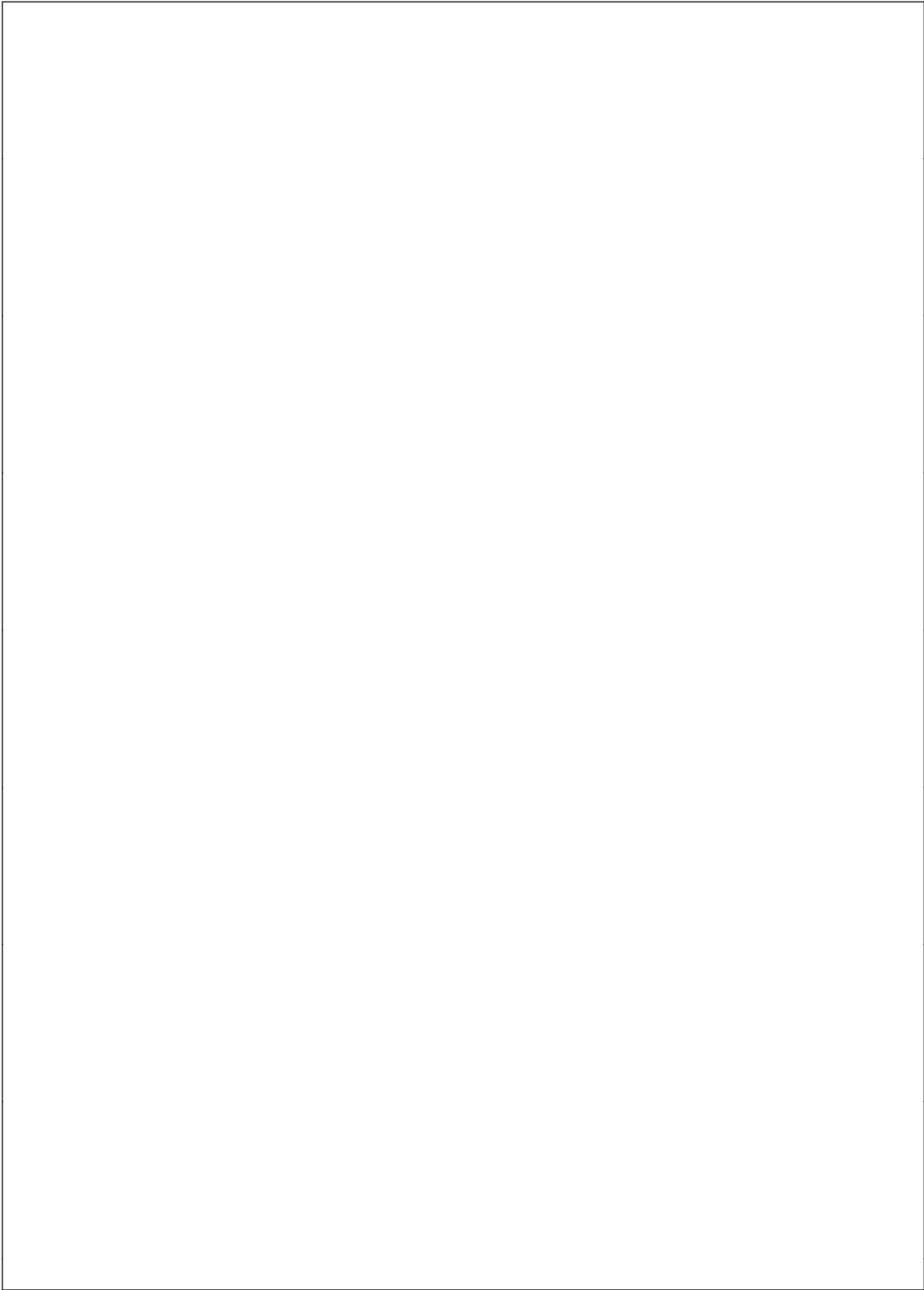
TL/F/6378-3

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma 3$, $\Sigma 4$, and C4.

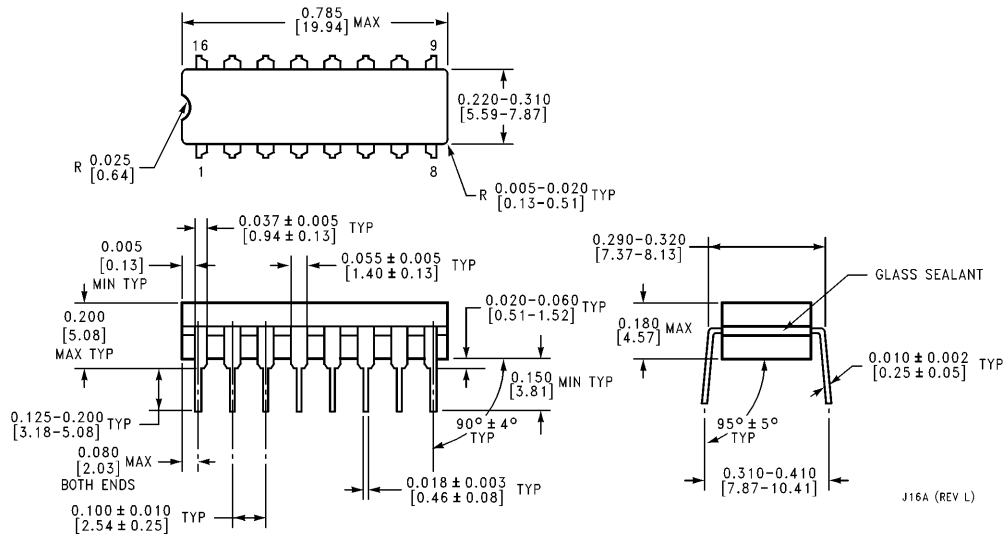
Logic Diagram



TL/F/6378-2



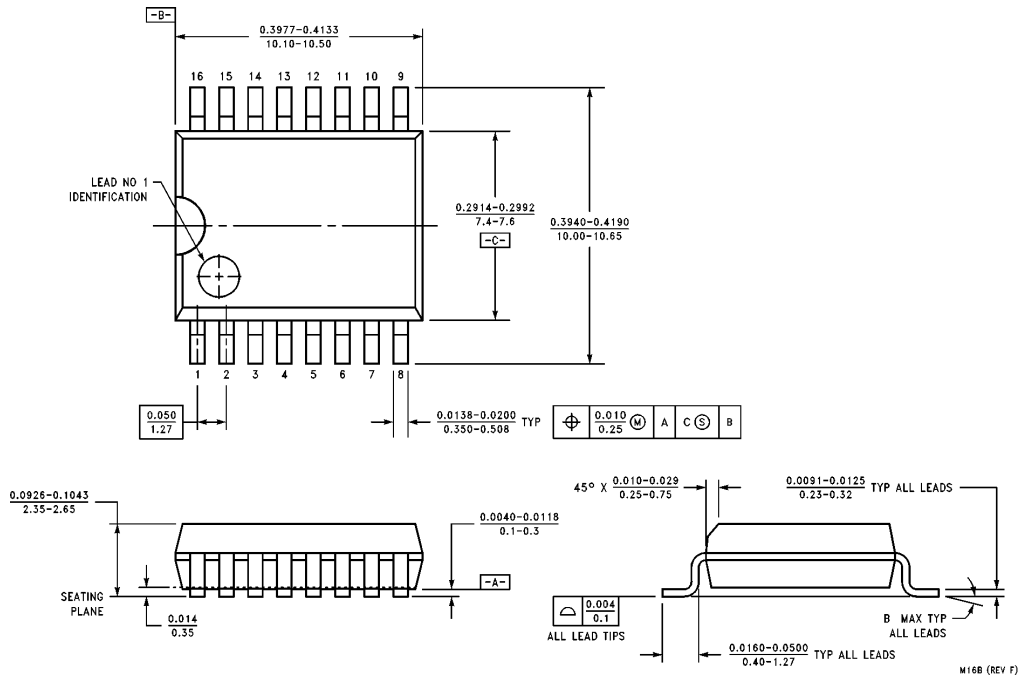
Physical Dimensions inches (millimeters)



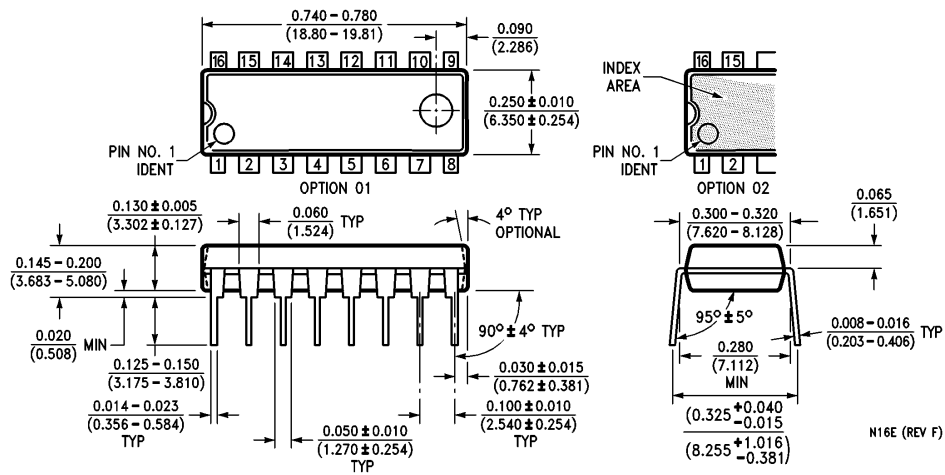
16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS83ADMQB or DM54LS83AJ
NS Package Number J16A

J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)

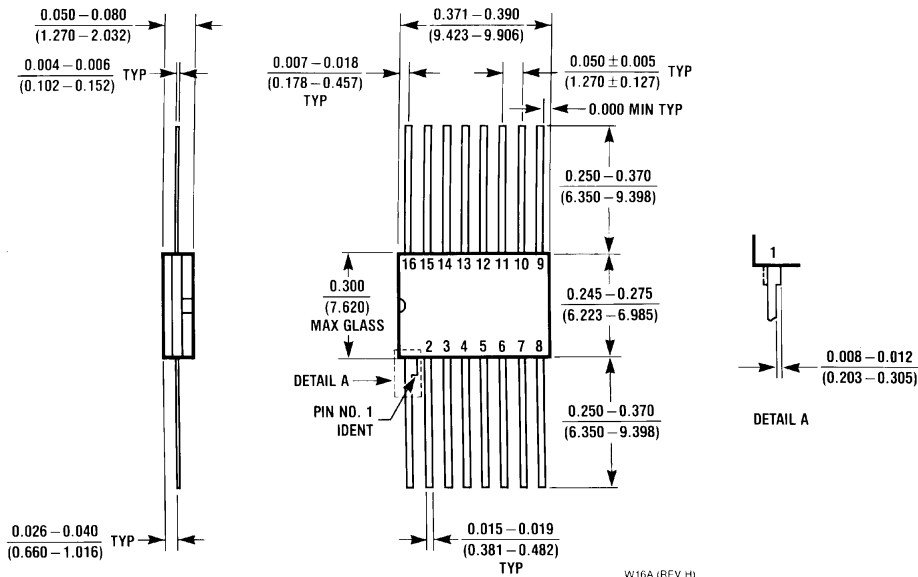


16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS83AWM
NS Package Number M16B



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS83AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS83AFMQB or DM54LS83AW
NS Package Number W16A

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