5-Bit Shift Registers

General Description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may also be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is low. Clearing is independent of the level of the clock input.

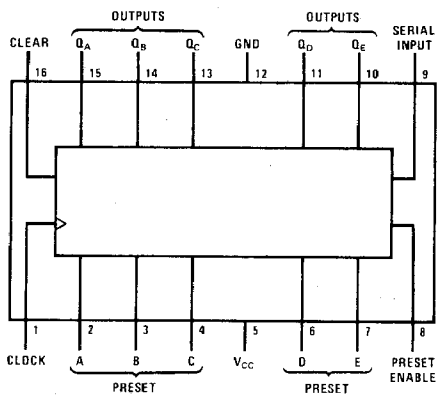
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting is also independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

Features

- N-bit serial-to-parallel converter
- N-bit parallel-to-serial converter
- N-bit storage register

Connection Diagram



5496(J), (W); 7496(J), (N), (W);
54LS96/74LS96(J), (N), (W)

Truth Table

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET					CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)

X = don't care (any input, including transitions)

↑ = transition from low to high level

Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., respectively before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively before the most recent ↑ transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM54/74 96 MIN	DM54/74 96 TYP(1)	DM54/74 96 MAX	DM54LS/74LS LS96 MIN	DM54LS/74LS LS96 TYP(1)	DM54LS/74LS LS96 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7	V
				DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5				V
			I_I = −18 mA							−1.5	
I_{OH}	High Level Output Current						−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = −400μA		DM54	2.4	3.4		2.5	3.5		V
				DM74	2.4	3.4		2.7	3.5		
I_{OL}	Low Level Output Current			DM54			16			4	mA
				DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IH} = 2V V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4	V
				DM74		0.2	0.4		0.35	0.5	
			I_{OL} = 4 mA	DM74					0.25	0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1				mA
			V_I = 7V							0.1	
I_{IH}	High Level Input Current — Any Input Except Preset Enable	V_{CC} = Max	V_I = 2.4V				40				μA
			V_I = 2.7V							20	
	High Level Input Current — Preset Enable		V_I = 2.4V				200				
			V_I = 2.7V							20	
I_{IL}	Low Level Input Current — Any Input Except Preset Enable	V_{CC} = Max, V_I = 0.4V					−1.6			−0.4	mA
	Low Level Input Current — Preset Enable						−8			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−57	−30		−130	mA
				DM74	−18		−57	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)		DM54		48	68		12	20	mA
				DM74		48	79		12	20	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

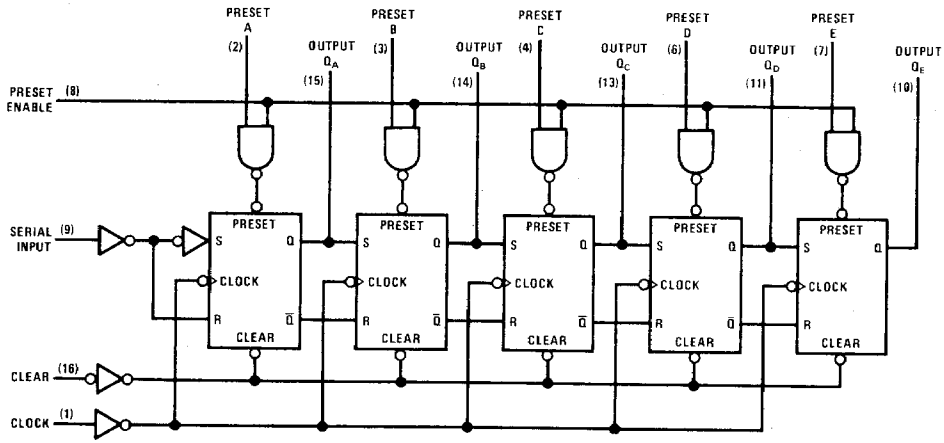
(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		DM54/74 96 CONDITIONS	DM54/74 96 MIN	DM54/74 96 TYP	DM54/74 96 MAX	DM54LS/74LS LS96 CONDITIONS	DM54LS/74LS LS96 MIN	DM54LS/74LS LS96 TYP	DM54LS/74LS LS96 MAX	UNITS
f_{max}	Maximum Shift Frequency		10				10			MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock	C_L = 15 pF, R_L = 400Ω		25	40	C_L = 15 pF, R_L = 2 kΩ		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock			25	40			25	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Preset or Preset Enable			25	35			28	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				55				55	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse		35				35			ns
t_W	Width of Preset and Clear Input Pulse		30				30			ns
t_{SETUP}	Serial Input Setup Time		30				30			ns
t_{HOLD}	Serial Input Hold Time		0				0			ns

Logic Diagram



Timing Diagram

TYPICAL CLEAR, SHIFT, PRESET, AND SHIFT SEQUENCES