National Semiconductor

# DM74S381 Arithmetic Logic Unit/Function Generator

## General Description

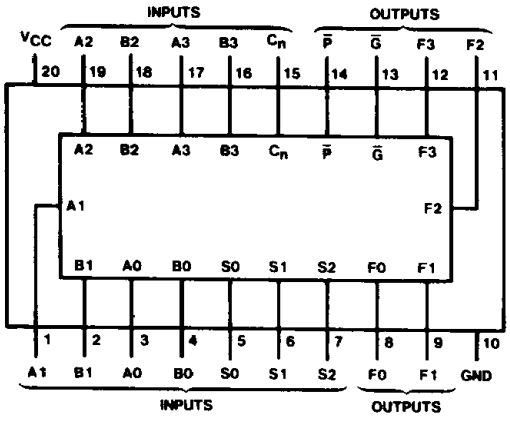
The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package. The method of cascading 54S182/74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustated under typical applications data for the 'S182. The typical addition times shown illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

## Features

- A fully parallel 4-Bit ALU in 20-pin package for 0.300-inch row spacing
- Ideally suited for high-density economical processors
- Parallel inputs and outputs and full look-ahead provide system flexibility
- Arithmetic and logic operations selected specifically to simplify system implementation:
  - A minus B
  - B minus A
  - A plus B
  - and five other functions
- Schottky-clamped for high performance
  - 16-bit add time . . . 26 ns typ using look-ahead
  - 32-bit add time . . . 34 ns typ using look-ahead

## Connection Diagram

**Dual-In-Line Package**




TL/F/6487–1

**Order Number DM74S381N**
**See NS Package Number N20A**

## Function Table

| Selection | | | Arithmetic/Logic Operation |
|---|---|---|---|
| S2 | S1 | S0 | |
| L | L | L | CLEAR |
| L | L | H | B MINUS A |
| L | H | L | A MINUS B |
| L | H | H | A PLUS B |
| H | L | L | A ⊕ B |
| H | L | H | A + B |
| H | H | L | AB |
| H | H | H | PRESET |

H = high level, L = low level

## Pin Designations

| Designation | Pin Nos. | Function |
|---|---|---|
| A3, A2, A1, A0 | 17, 19, 1, 3 | Word A Inputs |
| B3, B2, B1, B0 | 16, 18, 2, 4 | Word B Inputs |
| S2, S1, S0 | 7, 6, 5 | Function-Select Inputs |
| $C_n$ | 15 | Carry Input for Addition, Inverted Carry Input for Subtraction |
| F3, F2, F1, F0 | 12, 11, 9, 8 | Function Outputs |
| $\overline{P}$ | 14 | Inverted Carry Propagate Output |
| $\overline{G}$ | 13 | Inverted Carry Generated Output |
| $V_{CC}$ | 20 | Supply Voltage |
| GND | 10 | Ground |

## Absolute Maximum Ratings (Note)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High Level Input Voltage | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | 0.8 | V |
| $I_{OH}$ | High Level Output Current | | | −1 | mA |
| $I_{OL}$ | Low Level Output Current | | | 20 | mA |
| $T_A$ | Free Air Operating Temperature | 0 | | 70 | °C |

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max $V_{IH}$ = Min, $V_{IL}$ = Max | | | | 0.5 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max $V_I$ = 2.7V | Any S | | | 50 | μA |
| | | | Cn | | | 250 | |
| | | | Any Other | | | 200 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max $V_I$ = 0.5V | Any S | | | −2 | mA |
| | | | Cn | | | −8 | |
| | | | Any Other | | | −6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 2) | | −40 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 105 | 160 | mA |

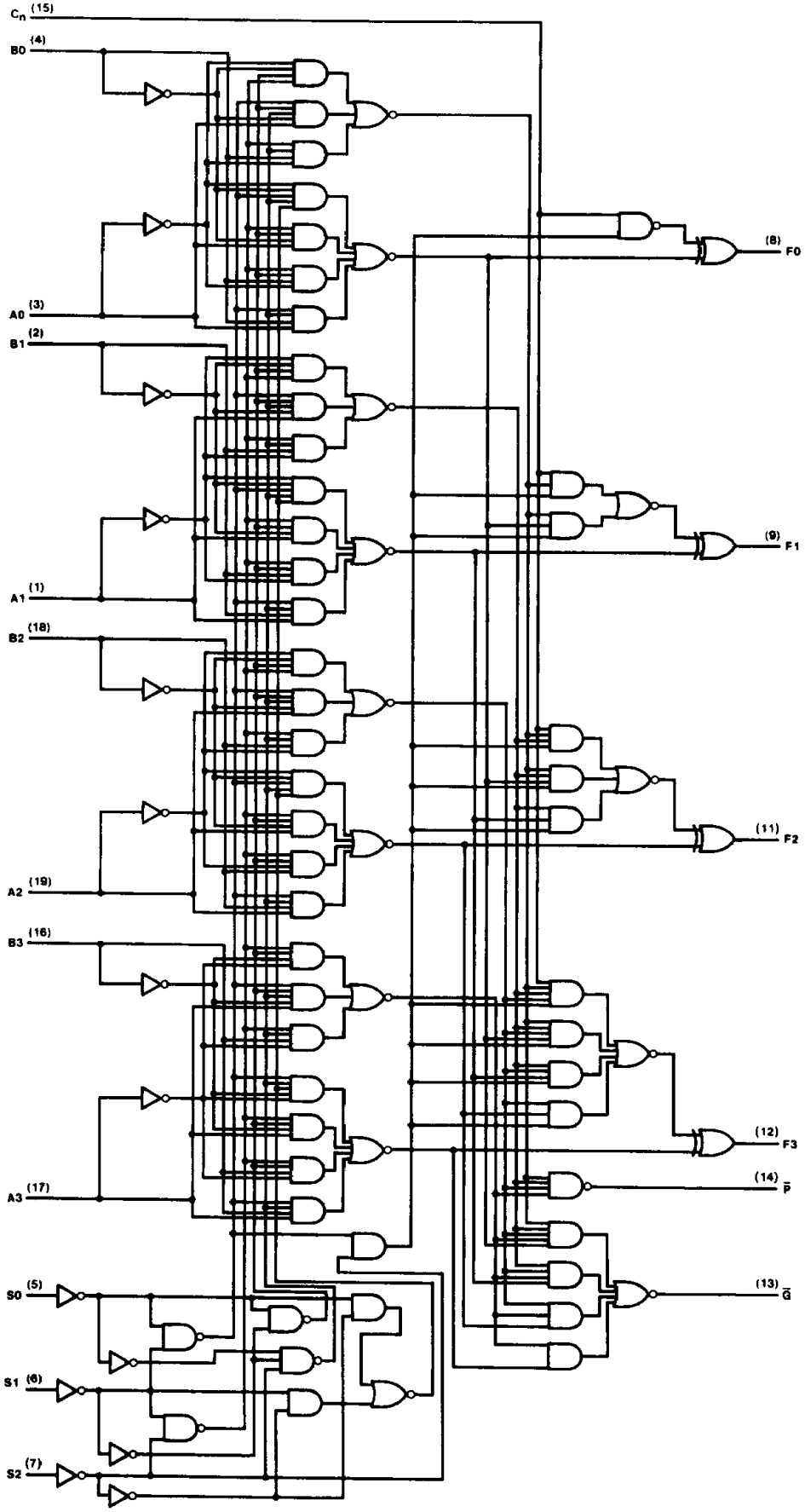
**Note 1:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics at $V_{CC}$ = 5V and $T_A$ = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $R_L$ = 280Ω | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Cn to Any F | | 17 | | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Cn to Any F | | 17 | | 19 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | A or B to $\overline{G}$ | | 20 | | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | A or B to $\overline{G}$ | | 20 | | 23 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | A or B to $\overline{P}$ | | 18 | | 21 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | A or B to $\overline{P}$ | | 18 | | 21 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | $A_i$ or $B_i$ to $F_i$ | | 27 | | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | $A_i$ or $B_i$ to $F_i$ | | 25 | | 27 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | S to Any | | 30 | | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | S to Any | | 30 | | 33 | ns |

## Logic Diagram

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