Dual/Quad Gated Flip-Flops

General Description

The DM7511/8511 or the low-power versions DM75L11/85L11, are dual, gated, D-type flip-flops. Each flip-flop has its own clock, clear line, and two gated inputs. Both gate inputs must be low to enable data transfer to the output.

The DM7512/8512, and DM75L12/85L12 are dual, gated flip-flops which can operate in either a J-K mode, or as D-type flip-flops. They have a common clock and common, asynchronous clear, but have separate mode inputs such that one side can operate as J-K while the other side operates as a D-type flip-flop.

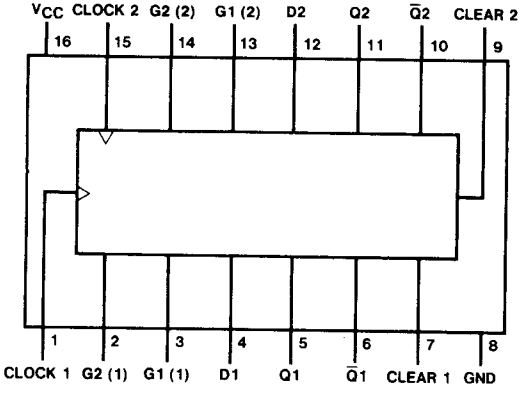
The DM7613/8613, and DM76L13/86L13 are quad, gated, D-type flip-flops with common clock, common clear, and gated input. When a high logic level is applied to the gated input, data entry to the flip-flop is inhibited.

Features

- Positive-edge triggered
- Do-nothing state
- Buffered inputs

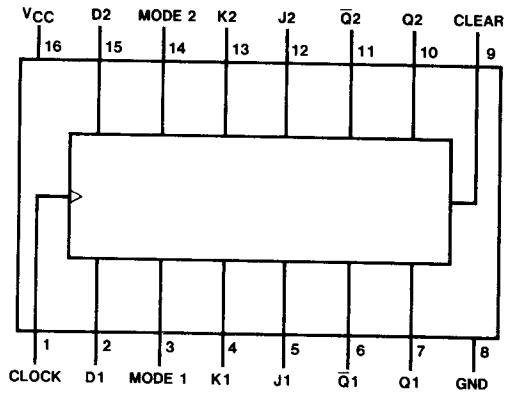
Type	Typical Toggle Rate	Typical Power Dissipation
DM7511/8511	45 MHz	210 mW
DM75L11/85L11	9 MHz	17.5 mW
DM7512/8512	28 MHz	220 mW
DM75L12/85L12	10 MHz	16.0 mW
DM7613/8613	30 MHz	290 mW
DM76L13/86L13	7 MHz	28.5 mW

Connection Diagrams



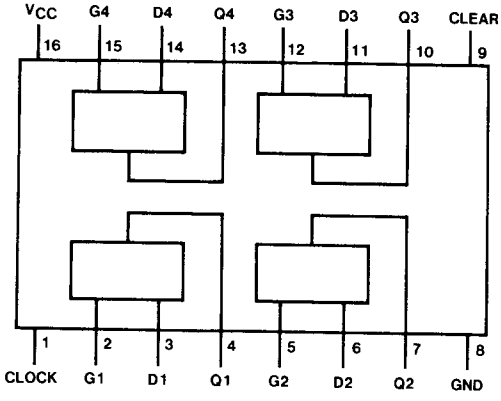
7511 (J,W)
75L11 (J,W)

8511 (N)
85L11 (N)



7512 (J,W)
75L12 (J,W)

8512 (N)
85L12 (N)



7613 (J,W)
76L13 (J,W)

8613 (N)
86L13 (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM75/85 11, 12			DM76/86 13			DM75L/85L11, 12 DM76L/86L13			Units
				Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			N/A	V
I_{OH}	High Level Output Current					−800			−800			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OH} = Max		2.4			2.4			2.4			V
I_{OL}	Low Level Output Current		Military			16			16			2.0	mA
			Commercial			16			16			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OL} = Max	Military			0.4			0.4			0.3	V
			Commercial			0.4			0.4			0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1.0			1.0			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40			40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V									−0.18	mA
			V_I = 0.4 V			−1.6			−1.6				
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		−18		−55	−18		−55	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max (3)	11, L11		42	55					3.5	4.9	mA
			12, L12		44	57					3.2	4.5	
			13, L13					58	76		5.7	7.9	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Supply current is measured with clear/clock at 3 V, all other inputs at 0 V.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C.

Parameter			From	To	Conditions	DM75/85 11, L11			DM75/85 12, L12			DM76/86 13, L13			Units
						Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 400 Ω (Standard) C_L = 50 pF, R_L = 4 kΩ (Low Power)	30	45		20	28		20	30		MHz
						6	9		6	10		5	7		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q			14	20		21	35		17	24	ns
							55	95		35	70		41	60	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Q			19	30		26	40		22	33	ns
							75	125		60	120		70	100	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear	$\overline{Q}$			14	20		22	35		N/A		ns
							55	95		32	65		N/A		
t_{PHL}	Propagation Delay Time, High-to-Low Output		Clear	Q			19	30		26	40		21	31	ns
							75	125		57	114		68	100	
$t_{W(CLOCK)}$	Width of Clock Pulse					20	11		25	15		24	16		ns
						100	30		100	30		100	50		
$t_{W(CLEAR}$	Width of Clear Pulse					20	10		25	13		27	18		ns
						100	30		100	30		100	50		
t_{SETUP}	Setup Time	J, D Inputs				15	9		15	9		24	16		ns
						80	40		110	55		100	55		
		Mode Inputs					N/A		30	20			N/A		ns
							N/A		150	85			N/A		
		K Inputs					N/A		20	13			N/A		ns
							N/A		150	80			N/A		
		G1 or G2 Inputs				30	21			N/A		30	21		ns
						120	60			N/A		150	85		
t_{HOLD}	Hold Time	All				0			0			0			ns
						0			0			0			

Truth Tables

11, L11

D	G1	G2	CLR	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	L	L	L	H
H	L	L	L	H	L
X	H	X	L	Q_n	$\overline{Q}_n$
X	X	H	L	Q_n	$\overline{Q}_n$
X	X	X	H	L	H*

12, L12

J	K	M	Clear	Q_{n+1}
L	L	H	L	Q_n
H	L	H	L	H
L	H	H	L	L
H	H	H	L	$\overline{Q}_n$
X	X	L	L	D
X	X	X	H	L*

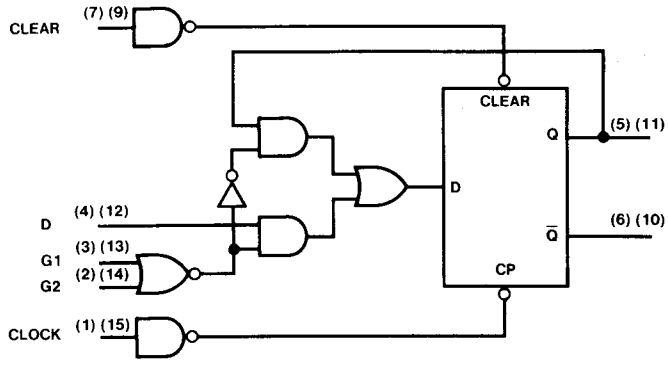
13, L13

D	G	CLR	Q_{n+1}
H	L	L	H
L	L	L	L
X	H	L	Q_n
X	X	H	L*

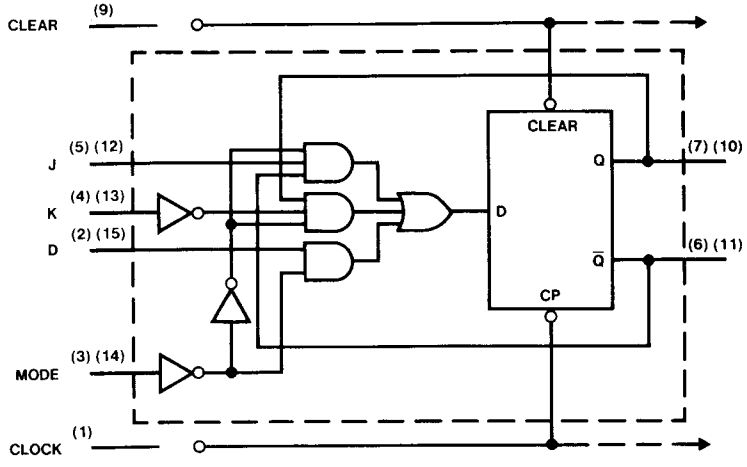
*Asynchronous Transition
X = Don't Care

Logic Diagrams

11, L11



12, L12



Logic Diagrams (Continued)

13, L13