New Products

DM7833/DM8833,DM7834/DM8834,DM7835/DM8835, DM7839/DM8839 quad TRI-STATE® transceivers

general description

This family of $\mathsf{TRI}\text{-}\mathsf{STATE}^{(\!g\!)}$ party line transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when $V_{CC} = 0V$. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DM7833/ DM8833 and DM7835/DM8835 employ TR1-STATE outputs on the receiver also, while on the DM7834/DM8834 and DM7839/DM8839 the receiver outputs are standard active pull up T2L.

The DM7833/DM8833 are non-inverting guad transceivers with a common driver disable control and a common receiver disable control.

The DM7839/DM8839 are non-inverting quad transceivers with a common two-input driver disable control.

The DM7834/DM8834 are inverting quad transceivers with a common two input driver disable control

The DM7835/DM8835 are inverting quad transceivers with a common driver disable control and a common receiver disable control.

features

Receiver hysteresis

450 mV (typ)

Receiver noise immunity

1.4V (typ)

Receiver input current

50 uA (max)

for normal V_{CC} or $V_{CC} = 0V$

Receivers

Sink Source 16 mA at 0.4V (max)

2.0 mA (mil)

5.2 mA (com) at 2.4V (min)

Drivers

Sink

50 mA at 0.5V (max) or 32 mA at 0.4V (max)

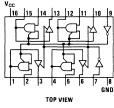
10.4 mA at

Source

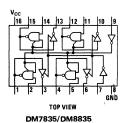
2.4V (min)

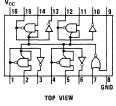
- Drivers have TRI-STATE outputs
- DM7833/DM8833 and DM7835/DM8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω DC terminated buses
- 74 series TTL compatible

connection diagrams

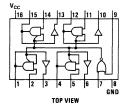


DM7833/DM8833





DM7834/DM8834



DM7839/DM8839