DM8108

8 port 10/100M Fast Ethernet Switching Controller

General Description

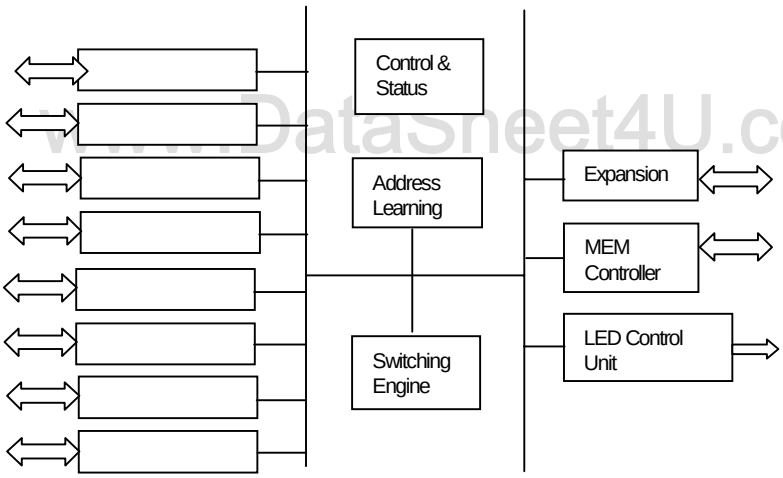
The DM8108 is an 8 port 10/100Mbit/s nonblocking Ethernet switch with on-chip address-lookup engine. The DM8108 provides a low-cost, high-performance switch solution with PHYs and single SGRAM.

The DM8108 provides eight 10/100Mbit/s Fast Ethernet interface. In half-duplex mode, all ports support back-pressure capability to reduce the risk of data loss for a long burst of activity. In the full-duplex mode of operation, the device uses IEEE std. 802.3 frame-based pause protocol for flow control. With full-duplex capability, port 0 – 7 support 1.6Gbit/s aggregate bandwidth connections. The DM8108 also supports port trunking/load balancing on the 10/100Mbit ports. This can be used to group ports on inter-switch links to increase the effective bandwidth between the systems.

The internal address-lookup engine supports up to 16.25K unicast and unlimited multicast and broadcast addresses. This engine performs destination and source addresses book-keeping and comparison which also forwards unknown destination address packets to all ports.

The DM8108 is fabricated with a .35um technology. Working at 3.3V, the inputs are 5V tolerant and the outputs are capable of directly driving at TTL levels.

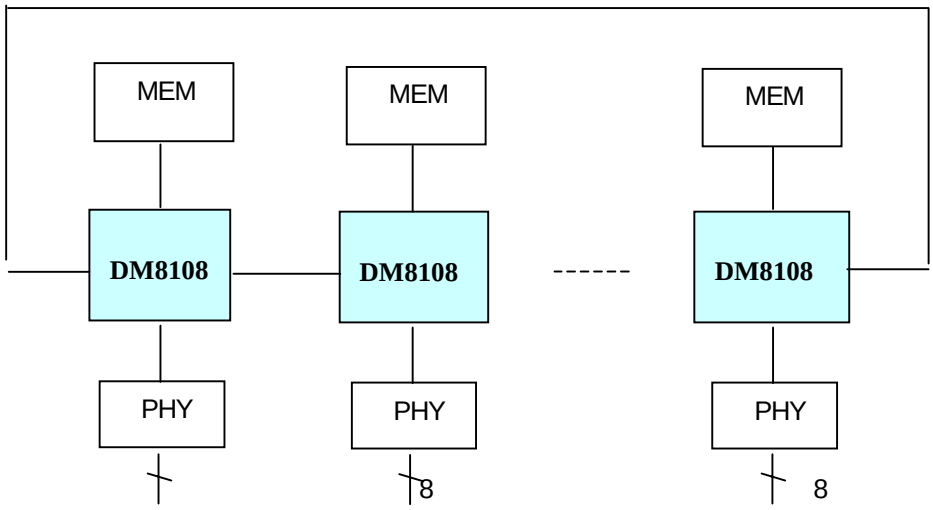
Block Diagram



Features

- Low cost Fast Ethernet Switching Controller.
  - Provide packet switching functions between eight 10/100Mbps, auto-negotiated on-chip Fast Ethernet ports and a proprietary Full-duplex Expansion port.
  - Cascade max. 8 DM8108s without extra glue logic for 64-port configuration.
- Incorporates three 802.3 compliant 10/100Mbps Media Access Controllers
  - Direct interface to MII (Media Independent Interface)
  - Half/Full Duplex Support for individual port (up-to 200Mbps/port)
  - IEEE 802.3 100Base-TX, T4.FX compatible
- Auto-negotiation supported through Serial MII interface
- High-performance Distributed Switching Engine
  - Performs packet forwarding and filtering at full wire-speed
  - 148,800 packets/sec. on each Ethernet port
- Direct support for packet buffering
  - Glue-less interface with 1 or 2 Mbytes of SDRAM (SGRAM)
  - 32 bit memory bus configuration
  - 66 Mhz – 90Mhz memory bus speed
  - Up-to 1.1K buffers, 1536-byte each, allocated to receive ports
- Support Store and Forward switching approach
  - Low last-bit to first-bit out delay
  - Allow mixed speed Ethernet packet switching
  - Allow conversion between different protocols
- Flow control
  - Support partitioning function
  - Support back-pressure while lack of internal resources
  - Support 802.3x PAUSE function in full duplex mode
  - Support up to 4-port trunking for 800Mbps bandwidth
- Advanced Address Learning and Searching
  - Self learning mechanism
  - Cache 128 address entries internally
  - Record up-to 16K Uni-cast MAC addresses and unlimited Multicast and Broadcast addresses
  - Automatic aging scheme
  - Broadcast filtering rate control
- Expansion Bus
  - Up-to 8 SW devices can be cascaded via expansion bus without extra logic
  - Full duplex mode transfer
  - Less Bus overhead
  - Automatic flow control
- Complete status report to a simple LED interface
- Suitable for low cost Switch market to replace Hub
- 0.35 μm process, 3.3V with 5V tolerant I/O
- 208-pin PQFP package

Application Example: Low cost 8 to 64 ports 10/100 Mbps auto-sensing switch



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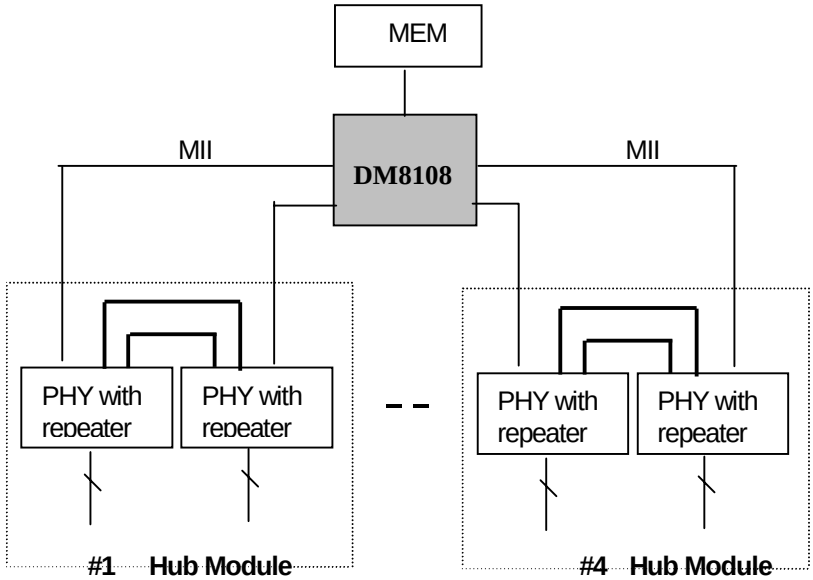
10/100 BaseTx

Cascaded up-to 64 10/100Mbps Fast Ethernet ports

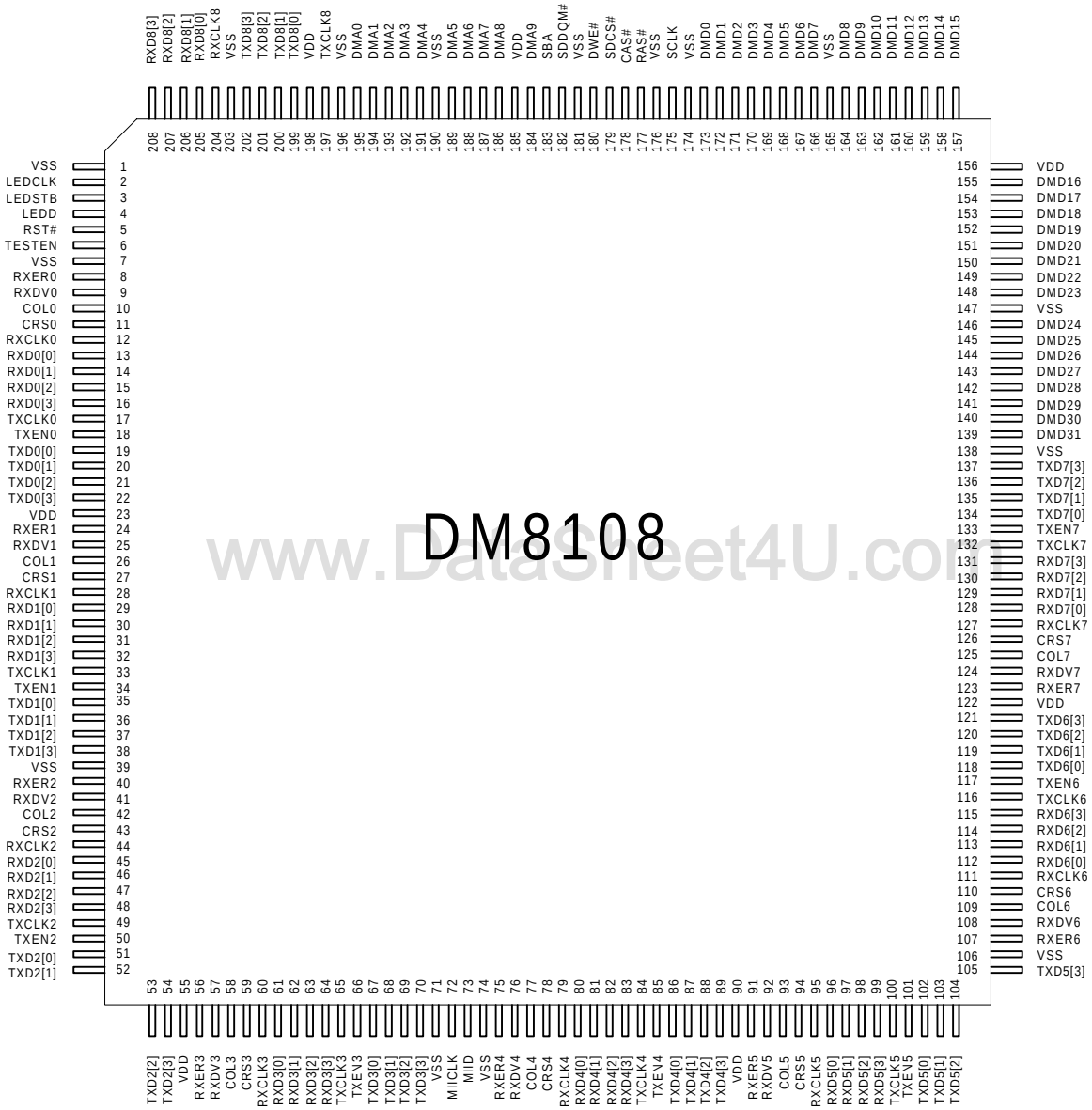
Application Example: Low cost auto-sensing switching hub implementation



10/100 BaseTx

High density mixed switching and hub ports with 8 collision domains

Pin Configuration



Pin Description

Pin Assignment

#	NAME	#	NAME	#	NAME	#	NAME	#	NAME
1	VSS	43	CRS2	85	TXEN4	127	RXCLK7	169	MD(4)
2	LEDCLK	44	RXCLK2	86	TXD4(0)	128	RXD7(0)	170	MD(3)
3	LEDSTB	45	RXD2(0)	87	TXD4(1)	129	RXD7(1)	171	MD(2)
4	LEDD	46	RXD2(1)	88	TXD4(2)	130	RXD7(2)	172	MD(1)
5	RST*	47	RXD2(2)	89	TXD4(3)	131	RXD7(3)	173	MD(0)
6	TESTEN*	48	RXD2(3)	90	VDD	132	TXCLK7	174	VSS
7	VSS	49	TXCLK2	91	RXER5	133	TXEN7	175	SCLK
8	RXER0	50	TXEN2	92	RXDV5	134	TXD7(0)	176	VSS
9	RXDV0	51	TXD2(0)	93	COL5	135	TXD7(1)	177	SRAS*
10	COL0	52	TXD2(1)	94	CRS5	136	TXD7(2)	178	SDCAS*
11	CRS0	53	TXD2(2)	95	RXCLK5	137	TXD7(3)	179	SDCS*
12	RXCLK0	54	TXD2(3)	96	RXD5(0)	138	VSS	180	SDWE*
13	RXD0(0)	55	VDD	97	RXD5(1)	139	MD(31)	181	VSS
14	RXD0(1)	56	RXER3	98	RXD5(2)	140	MD(30)	182	SDQM*
15	RXD0(2)	57	RXDV3	99	RXD5(3)	141	MD(29)	183	MA(10) – SBA
16	RXD0(3)	58	COL3	100	TXCLK5	142	MD(28)	184	MA(9)
17	TXCLK0	59	CRS3	101	TXEN5	143	MD(27)	185	VDD
18	TXEN0	60	RXCLK3	102	TXD5(0)	144	MD(26)	186	MA(8)
19	TXD0(0)	61	RXD3(0)	103	TXD5(1)	145	MD(25)	187	MA(7)
20	TXD0(1)	62	RXD3(1)	104	TXD5(2)	146	MD(24)	188	MA(6)
21	TXD0(2)	63	RXD3(2)	105	TXD5(3)	147	VSS	189	MA(5)
22	TXD0(3)	64	RXD3(3)	106	VSS	148	MD(23)	190	VSS
23	VDD	65	TXCLK3	107	RXER6	149	MD(22)	191	MA(4)
24	RXER1	66	TXEN3	108	RXDV6	150	MD(21)	192	MA(3)
25	RXDV1	67	TXD3(0)	109	COL6	151	MD(20)	193	MA(2)
26	COL1	68	TXD3(1)	110	CRS6	152	MD(19)	194	MA(1)
27	CRS1	69	TXD3(2)	111	RXCLK6	153	MD(18)	195	MA(0)
28	RXCLK1	70	TXD3(3)	112	RXD6(0)	154	MD(17)	196	VSS
29	RXD1(0)	71	VSS	113	RXD6(1)	155	MD(16)	197	TXENCLK
30	RXD1(1)	72	MDCLK	114	RXD6(2)	156	VDD	198	VDD
31	RXD1(2)	73	MDIO	115	RXD6(3)	157	MD(15)	199	TXD8(0)
32	RXD1(3)	74	VSS	116	TXCLK6	158	MD(14)	200	TXD8(1)
33	TXCLK1	75	RXER4	117	TXEN6	159	MD(13)	201	TXD8(2)
34	TXEN1	76	RXDV4	118	TXD6(0)	160	MD(12)	202	TXD8(3)
35	TXD1(0)	77	COL4	119	TXD6(1)	161	MD(11)	203	VSS
36	TXD1(1)	78	CRS4	120	TXD6(2)	162	MD(10)	204	RXDVCLK
37	TXD1(2)	79	RXCLK4	121	TXD6(3)	163	MD(9)	205	RXD8(0)
38	TXD1(3)	80	RXD4(0)	122	VDD	164	MD(8)	206	RXD8(1)
39	VSS	81	RXD4(1)	123	RXER7	165	VSS	207	RXD8(2)
40	RXER2	82	RXD4(2)	124	RXDV7	166	MD(7)	208	RXD8(3)
41	RXDV2	83	RXD4(3)	125	COL7	167	MD(6)		
42	COL2	84	TXCLK1	126	CRS7	168	MD(5)		

Pin Description (continued)

Please refer to the "Strap pin default value after reset section" for the detail description of the Strap pins.

DRAM Interface

Pin No.	Pin Name	I/O	Description
139 – 146, 148 – 155, 157 – 164, 166 – 173	MD(31:0)	I/O	DRAM data lines 31 – 0
183 – 184, 186 – 189, 191 – 195	MA(10:0)	I/O	DRAM address lines 10-0; strap pins during reset MA9: 0= enable limit4, 1=disbale limit 4 MA8: DRAM size selection; 0= 1M, 1=2M MA7-0: Auto-negotiation enable for port 7-0; 0= enabled
177	SRAS*	O	Row address strobe for SDRAM
178	SDCAS*	O	Column address strobe for SDRAM
180	SDWE*	O	Write cycle indication, internally pulled up
182	SDQM	O	Data Mask for SDRAM
179	SDCS*	O	Chip select for SDRAM

Expansion Bus

Pin No.	Pin Name	I/O	Description
204	RXDVCLK	I/O	Expansion port's receiving data valid
208 – 205	RXD8[3:0]	I/O	Expansion port's receive data input
197	TXENCLK	I/O	Expansion port's transmit enable output

202 – 199	TXD8[3:0]	I/O	Expansion port's transmit data output
			Strap pins during reset:
			TXD8[2:0] = device # setting
			TXD8[3] = dram timing

LED Interface

Pin No.	Pin Name	I/O	Description
2	LEDCLK	O	LED data clock
4	LEDD	O	LED data: active low. Data stream that contains LED indicators per port. The data is shifted out and should be qualified by LDSTB* to clock into external registers to drive LEDs. Strap pin during reset: 0: expansion port with fast speed 1: expansion port with lower apees
3	LDSTB	I/O	LED data strobe: active high. Used to strobe the LD into an external register Strap pin during reset: 0: force link 1: link detection through serial MII

MII Interface

Pin No.	Pin Name	I/O	Description
133,117,101, 85,66,50,34,18	TXEN(7:0)	B	Transmit Enable: Active high, synchronous to TXCLK; indicate that the transmission data is valid. Strap function during reset-- TXEN(7:0): 0 = port 7-0 full duplex
132,116,100,84, 65,49,33,17	TXCLK(7:0)	I	Transmit Clock: Provides the timing reference for the transfer of TXEN, TXD signals. It is 25MHz for 100Mbps and 2.5MHz for 10Mbps.
22 – 19	TXD0(3:0)	B	Transmit data for port 0; synchronous to TXCLK0. Strap function during reset-- TDX0[0]: 0=80Mhz, 1=66Mhz CLOCK operation TXD0[1]: 0=enable partition mode, 1=disable partition mode TXD0[2]: 0=enable expansion port, 1=disable expansion port TXD0[3]: 0=init only, 1= enable BIST
38 – 36	TXD1(3:0)	B	Transmit data for port 1; synchronous to TXCLK1. Strap function during reset -- TXD1[2:0]: test mode TXD1[3]: 0=enable CRC, 1=disbale CRC
54 – 51	TXD2(3:0)	B	Transmit data for port 2; synchronous to TXCLK2. Strap function during reset -- TXD2[2:0]: device # setting TXD2[3]: DRAM timing 0=fast, 1=slow
70 – 67	TXD3(3:0)	B	Transmit data for port 3; synchronous to TXCLK3. Strap function during reset -- TXD3[0]: 0=max. packet size 1536, 1=max. packet size 1518(default) TXD3[1]: 0=enable back_pressure, 1= disable (default) TXD3[3:2]: age strap pins 00= 64 sec. 01= 128 sec. 10= 256 sec. 11= disbale
89 – 86	TXD4(3:0)	O	Transmit data for port 4; synchronous to TXCLK4. Strap function during reset – TXD4[0]: 0= port 0 trunking enable 1= port 0 no trunking (default) TXD4[1]: 0= port 1 trunking enable 1= port 1 no trunking (default) TXD4[2]: 0= port 2 trunking enable 1= port 2 no trunking (default) TXD4[3]: 0= port 3 trunking enable 1= port 3 no trunking (default)
105 –102	TXD5(3:0)	O	Transmit data for port 5; synchronous to TXCLK5. Strap function during reset – TXD5[1:0]: broadcast filtering rate selection 00 = 8k/sec 01 = 16k/sec 10 = 64k/sec 11= disable
121 –118	TXD6(3:0)	O	Transmit data for port 6; synchronous to TXCLK6.
137 –134	TXD7(3:0)	O	Transmit data for port 7; synchronous to TXCLK7.
16 – 13	RXD0(3:0)	I	Receive data for port 0; synchronous to RXCLK0.
32 – 29	RXD1(3:0)	I	Receive data for port 1; synchronous to RXCLK1.
48 – 45	RXD2(3:0)	I	Receive data for port 2; synchronous to RXCLK2.
64 – 61	RXD3(3:0)	I	Receive data for port 3; synchronous to RXCLK3.
83 – 80	RXD4(3:0)	I	Receive data for port 4; synchronous to RXCLK4.

99 – 96	RXD5(3:0)	I	Receive data for port 5; synchronous to RXCLK5.
115 - 112	RXD6(3:0)	I	Receive data for port 6; synchronous to RXCLK6.
137 - 128	RXD7(3:0)	I	Receive data for port 7; synchronous to RXCLK7.
127,111,95,79, 60,44,28,12	RXCLK(7:0)	I	Receive clock for port 7 – 0; synchronous to RXD, RXDV,RXER; has same clock rate as TXCLK.
124,108,92,76, 57,41,25,9	RXDV(7:0)	I	Receive data valid indication for port 7 – 0.
123,107,91,75, 56,40,24,8	RXER(7:0)	I	Receive data error indication for port 7 – 0.
126,110,94,78, 59,43,27,11	CRS(7:0)	I	Carrier sense; active high. Indicates that either the transmit or receive medium is not Idle. CRS is not synchronous to any clock.
125,109,93,77, 58,42,26,10	COL(7:0)	I	Collision Detect; active high. Indicates a collision has been detected on the wire. This input is ignored during full duplex operation and in the half duplex mode while TXEN of the same port is low.
72	MDCLK	I/O	Serial MII management interface clock signal: 1MHz clock for MDIO data reference. Connected to all PHY ports; It is an input pin if the device # is not 0 in SDRAM mode; else, it is an output pin.
73	MDIO	I/O	Serial MII management interface data; this bi-direction line is used to transfer control Information and status between the PHY and the DM8108. It conforms to the IEEE-802.3 specifications. This signal may be connected to the PHY devices of all ports. Pulled down if not used.

Miscellaneous Interface pins

Pin No.	Pin Name	I/O	Description
175	SCLK	I	Memory clock: used by the DRAM state machine.
5	RST*	I	Reset signal for the chip.
6	TESTEN*	I	Test pin to enable test functions

Power pins

Pin No.	Pin Name	I/O	Description
23,55,90,122, 156,185,198	VCC	Power	Connected to 3.3V Power plane
1,7,39,71,74, 106,138,147, 165,174,176, 181,190,196, 203	GND	Ground	Connected to Ground plane

Functional Description

Fast Ethernet Ports Functional Overview

The DM8108 is a high-performance, low-cost Fast Ethernet Switching Controller which provides packet switching between eight on-chip, 10/100 Mbps ports and one optional expansion port. It is suitable for the auto-sensing 10/100Mbps switch application.

Switching Architecture

The switching architecture is based on the shared memory and handshaking signals to switch packets between on-chip ports hard-wired.

For an incoming packet, the receiving port's MAC stores it in the receiving buffers if it is a good packet. At the same time, the switching engine determines which port the packet will forward to and update the address table which will be used for future packet forwarding reference.

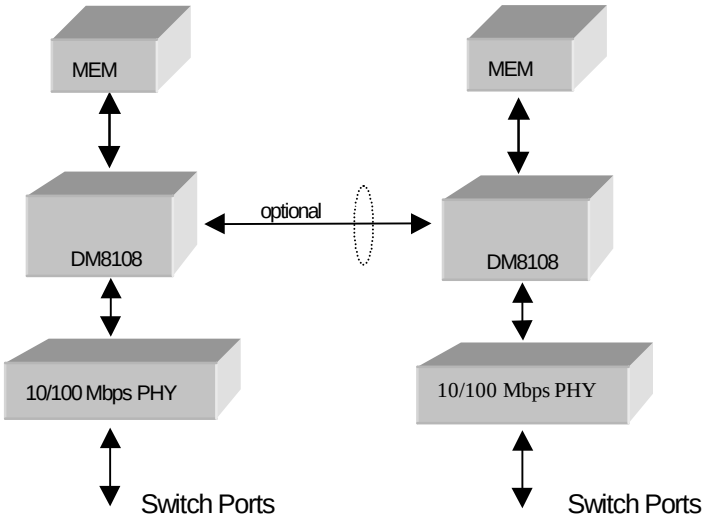
Fast Ethernet Ports

The DM8108 integrates eight Fast Ethernet ports, working at 10/100Mbps (half-duplex) or 20/200Mbps (full-duplex) with off-the-shelf PHY chips. The interface is glue-less through Media Independent Interfaces (MII). The auto-negotiation function determines the port's operating mode. With auto-negotiation disabled, the ports can be forced to operate at a certain mode, if so desired. Each port includes the Media Access Control function (MAC), LED signals for Link, Collision, Receive/Transmit, Half/Full duplex and Receive Buffer Full indications.

Address Recognition

The DM8108 in a system can recognize up to 16K Uni-cast MAC addresses and unlimited Multicast/Broadcast MAC addresses. An intelligent address recognition mechanism enables filtering and forwarding packets at full Ethernet wire speed. The DM8108 provides an address self-learning mechanism. As each DM8108 learns new address, it updates the address table in the storage.

Fig.1: Typical 10/100 Mbps auto-sensing switching hub application



Packet Routing

As any port in the DM8108 receives a packet, the DM8108 will put the received data in the receiving buffer and start the address recognition at same time.

1. If the destination address is pointed to a local port other than receiving port, the DM8108 will update the Transmit Descriptor of the target port with the buffer location and byte count information and wait for transmission.
2. If the destination address is pointed to a port located in other devices, the DM8108 will update the Transmit Descriptor of the expansion port with the receiving buffer location and byte count information and wait for transmission.
3. f the destination address is not found in the Address Table, the DM8108 will update all the Transmit Descriptors, except the one of the receiving port, for transmission.
4. For the Multicast/Broadcast addresses, the DM8108 simply updates all the Transmit Descriptors, except the one of the receiving port or the ports that are disabled, for Transmission.
5. For bad packet, the DM8108 simply discards it.
6. If the receiving buffer or the Transmit Descriptor for a particular port is full, the packet will be lost.

Network Management Features

The DM8108 is targeted for the non-managed Ethernet Switching application. No management functions provided.

DRAM Interface

The DM8108 interfaces to 1M or 2M bytes of SGRAM or SDRAM. The DRAM is used to store incoming packets as well as he address table and Transmit Descriptors. The DRAM can operate at up to 90MHz. One 256kx32 or 512kx16 SGRAM are required respectively for 1M or 2M shared memory size.

Expansion Bus

The expansion bus contains Receive Port and Transmit Port. Each port is 4-bit wide.

The Receive Port takes the incoming packet into a FIFO that has to be distributed to the Receiving Buffer immediately. At the same time, the DM8108 will check the destination and source addresses to determine the target port and update the Address Table if necessary.

The Transmit Port is dedicated for transferring packets out to other switching members if the Transmit Descriptor for this port saying the transmission is pending.

Total of 8-DM8108 can be cascaded for a 64-port switching system.

Operation Overview

The SW Architecture Family of switching devices has been defined as low cost, high performance and scalable architecture for a small switching system of packetized data. Various devices will be developed. The OEMs will be able to design robust switching configurations based on the SW architecture.

The SW Architecture Family uses a "store-and-forward' switching approach. This approach has the following advantages:

- Store-and-forward switches allow switching between differing speed media (e.g. 10Mbps and 100Mbps).
- Store-and-forward switches improve overall network performance by acting as a 'network cache', effectively buffering packets during times of heavy congestion.
- Store-and-forward switches prevent the erroneous packets from forwarding by analyzing the frame check sequence (FCS) before forwarding to the destination port.
- Store-and-forward switches prevent illegal frames (runt or oversized) from being forwarded and thereby reduce the congestion caused by bad packets.

The basic operation of DM8108 is very simple. The DM8108 receives the incoming packets from the Ethernet ports, searches in the Address Table for the destination MAC address, and forwards the packet to the appropriate port, which could be either local (one of the DM8108's port) or in a different DM8108 device that resides on the expansion bus. If the destination address is not found, the packet will be treated as a multicast packet and sent to every port (other than the source port) and other devices on the expansion bus.

The DM8108 automatically learns the port number of attached network devices by examining the Source MAC address of all incoming packets. If the Source Address is not found in the Address Table, the device adds it to the table (with source port and device information). The Address Table is managed by DM8108 individually.

Address Learning

The DM8108 can learn up to 16K unique MAC addresses. Addresses are stored in the Address Table located in the DRAM which will be initialized after RESET.

Packet Buffering

Incoming packets are buffered in the DRAM array. These buffers provide elastic storage for transferring data between low-speed and high speed segments. The packet buffers are managed automatically by the DM8108.

Packet Forwarding Protocol

The DM8108 updates the Transmit Descriptor of the target port, which is learned from Address Table, with the received packet buffer location and packet length. The MAC of target port will fetch the packet for transmission once the memory bus is available.

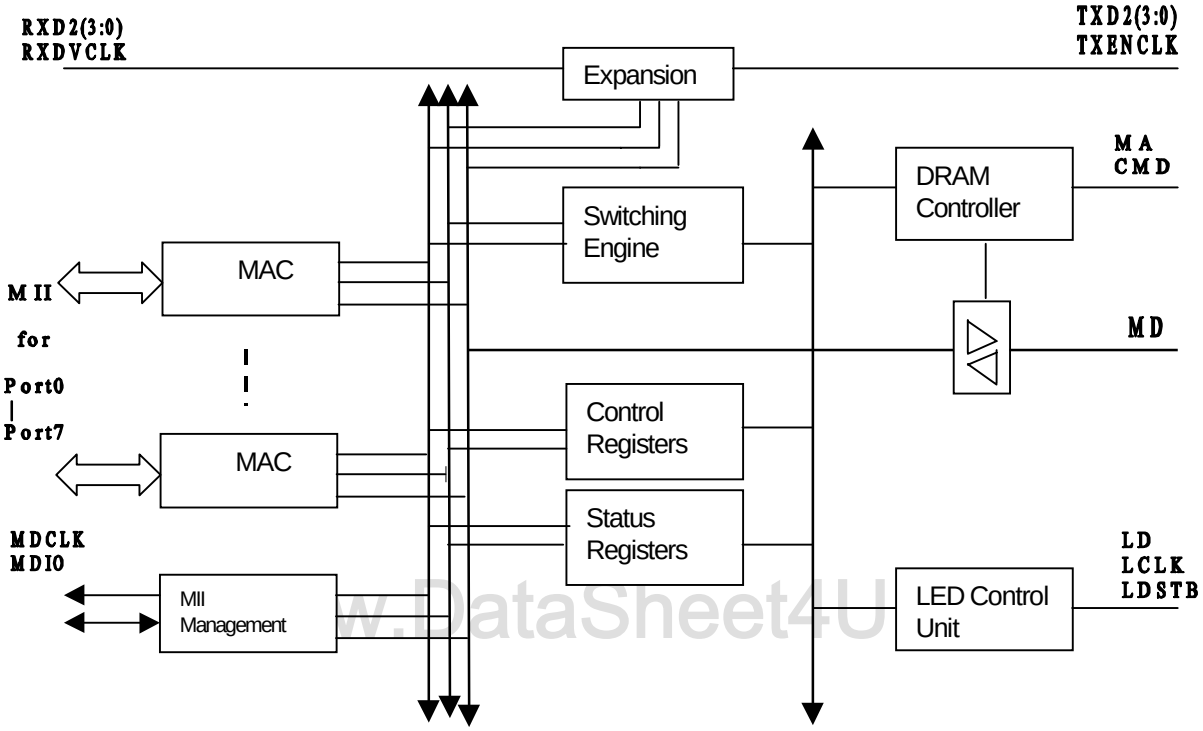
Expansion Bus

The Expansion Bus is defined as a special case of a normal Fast Ethernet MII port except running at much higher data rate.

The designer can link several DM8108s within a switching box or can link several switching boxes.

Theory of Operation

Block Diagram



Media Access Control

The MAC Engine incorporates the essential protocol requirement for an Ethernet IEEE-802.3 compliant node, and provides the interface between the FIFO subsystem and the MII. The MAC has two primary attributes:

Transmit and receive message data encapsulation

The MAC will discard the illegally short (less than 64 bytes of frame data) or oversized (greater than 1536 bytes) messages to be transmitted or received.

- Framing (frame boundary delimitation, frame synchronization)

The MAC engine will automatically handle the construction of the transmit frame. Once the transmit FIFO has been filled to the predetermined threshold and access of the channel is permitted, the MAC will commence the following for transmission:

The receiving section of the MAC will detect an incoming preamble sequence when the RXDV signal is activated by the external PHY. The MAC will discard the preamble and begin searching for the SFD. Once the SFD is detected, all the subsequent nibbles are treated as part of the frame. The MAC will discard the message if it is shorter than 64-bytes or longer than 1518 (1536) bytes. The received frame will be sent to Receiving Buffer for switching.

If the frame terminates or suffers a collision before 64-bytes (after SFD) have been received, the MAC will automatically delete the frame from FIFO.

- Addressing (source and destination address handling)

  The MAC intercepts the source and destination address from the incoming frame and send them to switching engine for the following purposes:

  . To update the address table
  . To learn the switching target
  . To detect the DM8108 predefined address for the device control functions.

- Error detection (physical medium transmission errors)

  During transmission, if the switching engine failed to keep the transmit FIFO filled sufficiently, cause an underflow, the MAC engine will guarantee the message is either sent as runt packet (which will be detected by the receiving station) or as an invalid FCS (which will cause the receiver to reject the packet).

  During reception, the FCS is generated on every nibble (including the dribbling bits) coming from the cable, although the internally saved FCS value is only updated on the eighth bit (on each byte boundary). The MAC engine will ignore up to 7 additional bits at the end of a message (dribbling bits), that can occur under normal network operating conditions.

Preamble 1010…1010	SFD 10101011	Destination Address	Source Address	Length	Data	FCS
7 Bytes	1 Bytes	6 Bytes	6 Bytes	2 Bytes	40 – 1500 Bytes	4 Bytes

Media access management

IEEE 802.3 protocols define a media access mechanism that permits all stations to access the channel with equality. Any node can attempt to connect for the channel by waiting a predefined period of time (Inter Packet Gap) after the last activity before transmitting on the media. If two nodes simultaneously contend for the channel, their signals will interact causing loss of data, defined as collision. It is the responsibility of the MAC to attempt to avoid and recover from the end-to-end transmission to the receiving station.

- Medium allocation (collision avoidance, except in full-duplex operation)

The MAC will monitor the medium for traffic by watching for carrier activity. When the carrier is detected, the media is considered as busy, and the MAC should defer to the existing message.

The MAC implements the IEEE-802.3 defined two part deferral algorithm, with Inter-Frame-Spacng-Part1 (IFS1) time for 64-bit time (6.4 us for10-BASE and 640 ns for 100-BASE). The Inter-Frame-Spacing-Part2 (IFS2) interval is, therefore, 32-bit time. The Inter Packet Gap (IPG) timer will start timing the 96-bit time Inter-Frame-Spacing after the receiving carrier is de-asserted. During the IFS1, the MAC will defer any pending transmit frame and respond to the receive message. The IPG counter will be cleared to 0 continuously until the carrier de-asserts, at which point the IPG will resume the 96-bit time count again. Once the IFS1 period has completed and the IFS2 has commenced, the MAC will not defer to the receiving frame if a transmit frame pending. The MAC will not attempt to receive the receiving frame, since it will start transmit and generate a collision at 96-bit time. The MAC will complete the preamble (64-bit) and JAM (32-bit) sequence before ceasing transmission and invoking the random back-off algorithm.

- Contention resolution (collision handling, except in full-duplex mode)

If a collision is detected through COL pin before the complete preamble/SFD sequence has been transmitted, the MAC engine will complete the preamble/SFD before appending the JAM sequence. If a collision is detected after the preamble/SFD has been completed, but prior to 512 bits being transmitted, the MAC will abort the transmission and append the JAM sequence immediately. The JAM sequences is a 32-bit all “34” pattern.

The MAC will attempt to transmit a frame a total of 16 times (15-retries) due to normal collisions (those within the slot time). Detection of collision will cause the transmission to be re-scheduled to a time determined by the random back-off algorithm. If 16 attempts experienced collisions, the transmitting message will be flushed from FIFO.

If a collision is detected after 512-bit times have been transmitted, the collision is termed “Late” collision. The MAC will abort the transmission, append the JAM sequence. No retry attempt will be scheduled on detection of late collision, and transmit message will be flushed from the FIFO.

The MAC implements the truncated exponential back-off algorithm defined by the 802.3 standard.

In full-duplex mode, the MAC transmits unconditionally.

10/100 Mbps MII Half–duplex Transmission

When the MAC has a frame ready for transmission, it samples the link activity. If the CRS signal is inacive (no activity on the link), and the IPG counter has expired, frame transmission begins. The data is transmitted through TxD(3:0) of the transmitting port, clocked on the rising edge of TxCLK. The TxEN is asserted at same time. In case of collision, the PHY asserts the COL signal on the MAC, which will then stop the transmission and will perform contention resolution. The retry policy is based on the:

Transmit Exception Conditions

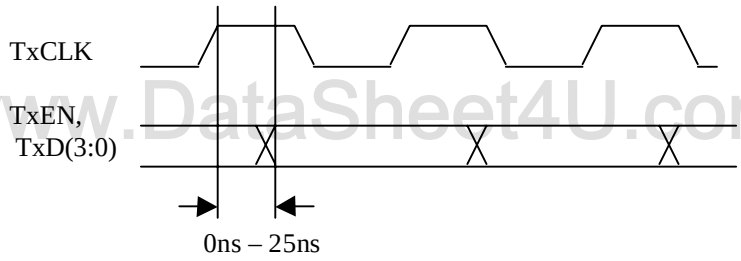
- Under normal operating conditions

  The MAC will ensure that the collisions that occurred within 512 bit times from the start of transmission (including preamble) to be automatically retried with no switching engine intervention. The transmit FIFO ensures this by guaranteeing that the data contained within the FIFO will not be overwritten until at least 64 bytes (512 bits) of preamble plus address, length, and data fields have been transmitted onto the network without encountering a collision. In full-duplex mode, the data in the FIFO can be overwritten as soon as it is transmitted.

- Under abnormal operating conditions

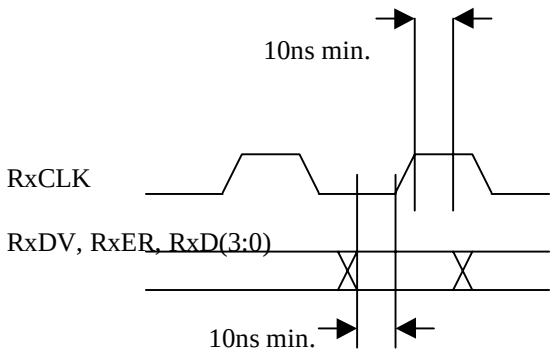
  . Late collision

  The MAC will abandon the transmit process for that frame, and process the next transmit frame in the ring. Frame experiencing a late collision will not be retried.



10/100 Mbps MII Half-duplex Reception

Frame reception starts with the assertion of RxDV (while the MAC is not transmitting) by the PHY. Once RxDV is asserted, the MAC will begin sampling the incoming data on pins RxD(3:0) on the rising edge of RxCLK. Reception ends when the RxDV is de-asserted by the PHY. The last nibble sampled by the MAC is the nibble present on RxD(3:0) on the last RxCLK rising edge in which RxDV is still asserted. If MAC detected the assertion of RxER while RxDV is asserted, it will designate this packet as corrupted. The following figure shows the MII receive signals timing.



Receive Exceptional Conditions

- Normal network operating conditions

  During the reception, the MAC will ensure that if collision occurs during packet reception, the packet will be automatically deleted from the receive FIFO. The Receive FIFO also will delete any frame that is composed of fewer than 64 bytes (Runt Packet).

- Abnormal network operating conditions

  Abnormal network conditions include:

  . FCS errors

  Reception and checking of the received FCS is performed automatically by the MAC. The equation is:

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

If any FCS error occurred, the MAC will discard the packet.

. Late Collision

Late Collision is the collision being detected after 512-bit times while receiving.

. FIFO transfer error

The MAC also monitors FIFO overflow status, which will force the most recent receiving packet (not finished) in the FIFO be discarded.

- Back-pressure

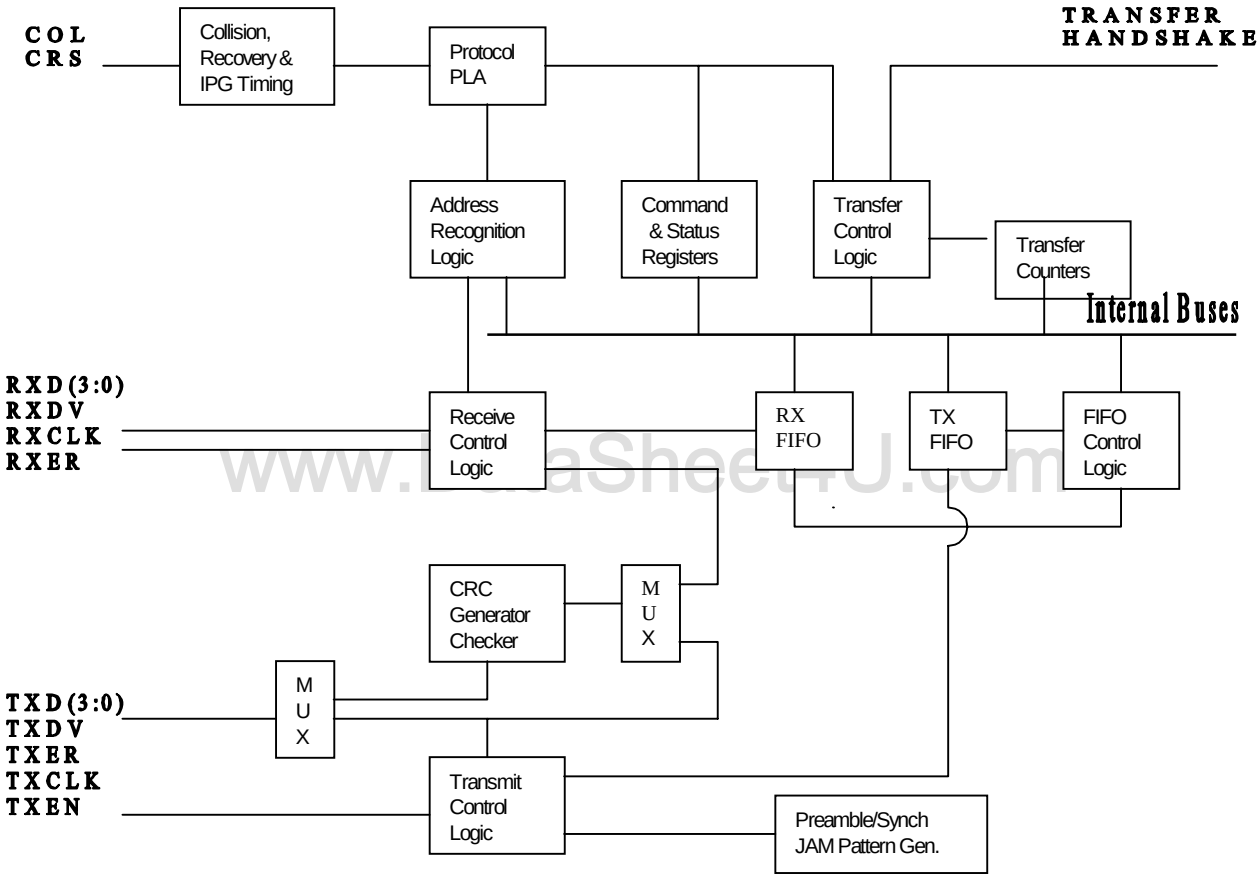
The DM8108 will generate “jam pattern” to force collision on the media as far as it finds out that the internal resources can not meet it demands.

10/100 Mbps Full-Duplex Operation

When operating in the Full-duplex mode, the CRS signal is associated with the received frames only and has no effect on the transmitted frames. The COL signal is ignored by the MAC while in Full-duplex mode. Transmission starts when TxEN goes active; regardless the state of RxDV. Reception starts when the RxDV signal is asserted indicating traffic on the receiving port. The DM8108 supports IEEE 802.3x PAUSE function in the full duplex mode operation.

During receiving, the DM8108 will issues PAUSE command with the largest timer value to stop the transmitter if the receiving buffer pointer is above the full threshold value (high water mark). When the receiving buffer pointer is below the not-full threshold value (low water mark), it will issue another PAUSE command with zero timer value to start the transmitter. The DM8108 is able to monitor the PAUSE command and stop transmitting accordingly to the timer value specified in the command packet.

Functional Blocks of the MAC



MII Management

MII Management Registers Serial Access

The MII specification defines a set of 32 16-bit status and control registers that are addressable through the serial data interface pins MDCLK and MDIO. Please refer to a PHY device's spec for the definition of the registers.

The DM8108 will initialize MII management registers accessing after RESET. In EDO memory configuration mode, the DM8108 acts as Serial MII initiator. In SDRAM memory configuration, only the DM8108 whose device # equals to 0 is the initiator. Other devices cascaded will be the listener to extract the auto-negotiation information from MID stream.

MDCLK has a maximum clock rate of 2.5MHz. The MDIO line is bi-directional and may be shared by up to 32 devices. The protocol and the access waveform are shown below:

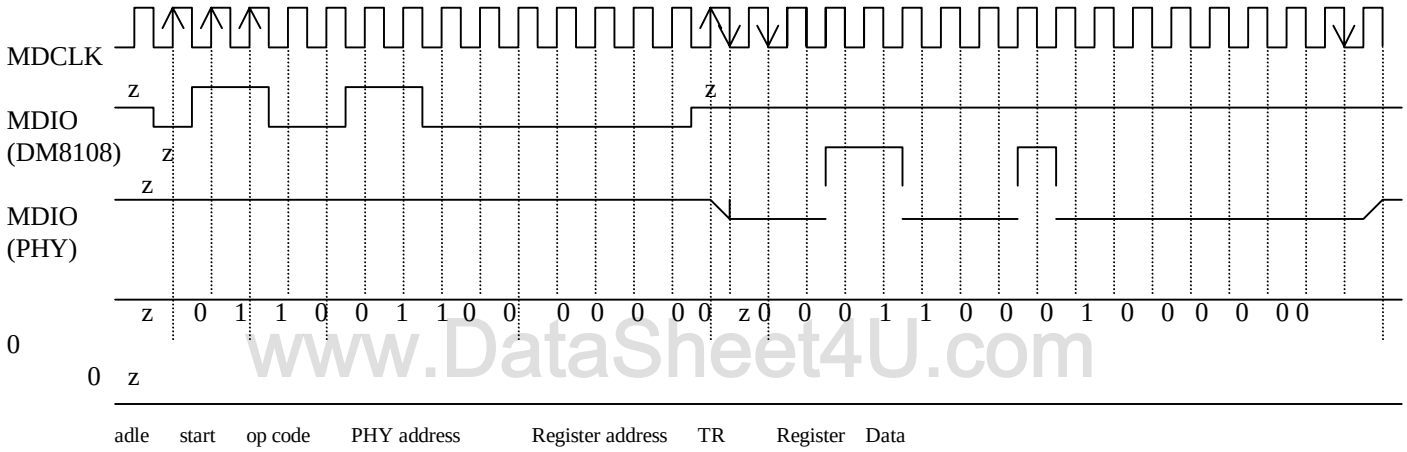


Figure Typical MDIO Read Operation

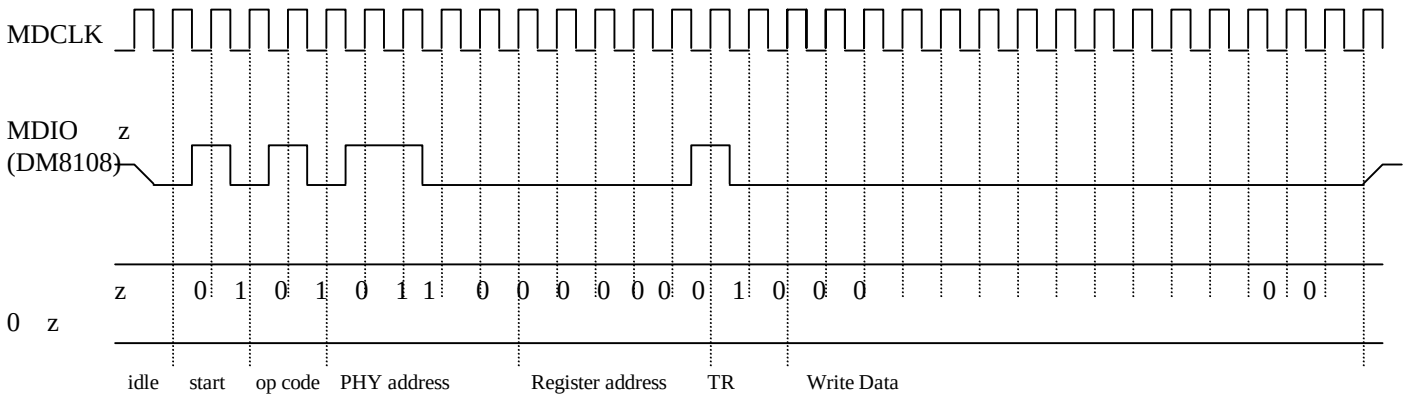


Figure Typical MDIO Write Operation

Protocol	<idle><start><op code><device address><register addr.><Turnaround>< data ><idle>
Read Operation	< z >< 01 >< 10 >< xxxxx >< xxxxx >< z0 ><xxxxh><idle>
Write Operation	< z >< 01 >< 01 >< xxxxx >< xxxxx >< 10 ><xxxxh><idle>

Table MII Management Serial Protocol

Auto-Negotiation

Auto-negotiation disabled

When ANEG* (MA[7:0]) strap pin is high, auto-negotiation is disabled, and the corresponding port can be selected as half- or full- duplex mode respectively. Following the RESET the port duplex mode is set by the state sampled on the TXEN(7:0) pins. The speed that each port operates in (10Mbps or 100Mbps) is determined by the frequency of TxCLK(7:0) and RxCLK(7:0) generated by PHY. The PHY generates 25MHz clock for both TxCLK and RxCLK in 100Mbps operation and 2.5MHz clock in 10Mbps operation.

Auto-negotiation enabled

When ANEG* (MA[7:0]) pins are tied low, the MAC decodes the duplex mode from the values of the Auto-Negotiation Advertisement Register and the Auto-Negotiation Link Partner Ability Register at the end of Auto-negotiation process. Once the duplex mode is resolved, the DM8108 updates the port control registers. The DM8108 will continuously perform the following operations for each port (PHY address 0-7 alternatively), implemented as READ commands issued via the MDCLK/MDIO interface:

Link Detection and Link Detection Bypass (FLNK*)

The DM8108 will continuously query the PHY devices for their link status associated with Auto-Negotiation Process. The DM8108 will alternatively read registers from PHY address 0 to 7 and update the internal link bits according to the value of bit 2 of register 1. In case of link down (bit 1.2=0), that port will enter “link test fail state”. In this state, all the port’s logic go to a reset state. The port will enter the “link up state” if the bit 1.2 is “1” or the FLNK* (force link, LEDSTB* strobed low during reset) pin is sampled low during reset.

Partition Mode

A port enters partition mode when more than 64 consecutive collisions are seen on the port. In partition mode the port continuous to transmit but it will not receive. A port returned to normal operation mode when a good packet is seen on the wire.

Enabling Partition Mode

Partitioned mode is enabled always.

Entering Partition State

A port will enter the Partition state when PAEN* strap pin sampled low during reset and when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.

While in Partition state:

- The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission, will be transmitted, while ignoring the internal collision indication. This frees up the port’s transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition. The partition indication is available via the LED interface.

Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

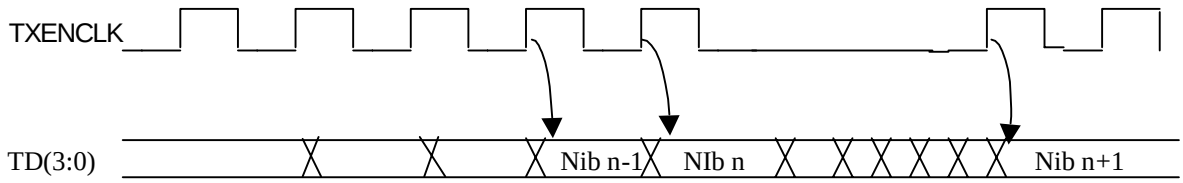
Expansion Bus

The expansion bus operates at Full-Duplex mode that provides up-to 7200Mbps bandwidth for device to device connection. Several DM8108 can be cascaded as a pipe to provide a robust Ethernet Switching system.

The bus itself is very simple. The transmit and receive ports contain independent data, valid and handshake signals. No bus arbitration is involved.

The receive port utilizes the RDVCLK to clock in the received data into FIFO and uses RXTOG requests for a Receiving Buffer block. The switching engine will execute the similar process as for the Ethernet Ports.

The transmit port appends the Sync. field to a normal Ethernet packet and sends the packet out through TD(3:0) at the rising edge of TXENCLK.



Switching Engine

All the packet switching is processed by the Switching Engine, which has following functions:

MAC Address Learning Process

The DM8108 has a self-learning mechanism for learning the MAC addresses of attached Fast Ethernet devices in real time. The DM8108 searches for the source address of an incoming packet in the Address Table and acts as follows:

If the source address was not found in the Address Table, the DM8108 waits until the end of the packet (no error) and updates the Address Table.

If the source address was found in the Address Table, the DM8108 waits for a good packet received indication.

Address Recognition

The DM8108 forwards the incoming packets to appropriate port(s) according to the Destination Address as follows:

- If the packet is from a local port--

  1) If it is a Unicast address and the address is found in the Address Table, the DM8108 will:

     . If the port number recorded is matched to port number on which the packet received, the packet is discarded.
     . If the port numbers are different, the packet is forwarded to the appropriate port.

  2) If it is a Unicast address and the address is not found in the Address Table, the DM8108 acts as if the packet is a Multicast packet and forwards it to the Expansion Transmit port and all the local ports except the incoming port,

  3) If it is a Multicast/Broadcast address, the packet is forwarded to the Expansion Transmit port and all local ports (except to the port on which the packet was received).

- If the packet is from Expansion Bus—

  1) If it is a Unicast address specified in the Destination Address in the Ethernet Packet, the DM8108 will:

     . If the recorded port pointed to a local port, the packet will be forwarded to that port.
     . If the destination address is not found (not recorded by the Mac address learning process), the packet will be forwarded to all the local ports and the Expansion Transmit port.

  2) If it is a Multicast/Broadcast address (destination device # should set invalid), the packet will be forwarded to all the local ports and the Expansion Transmit port.

Address Aging

The DM8108 includes hardware to support for automatic address aging.

Buffers and Queues

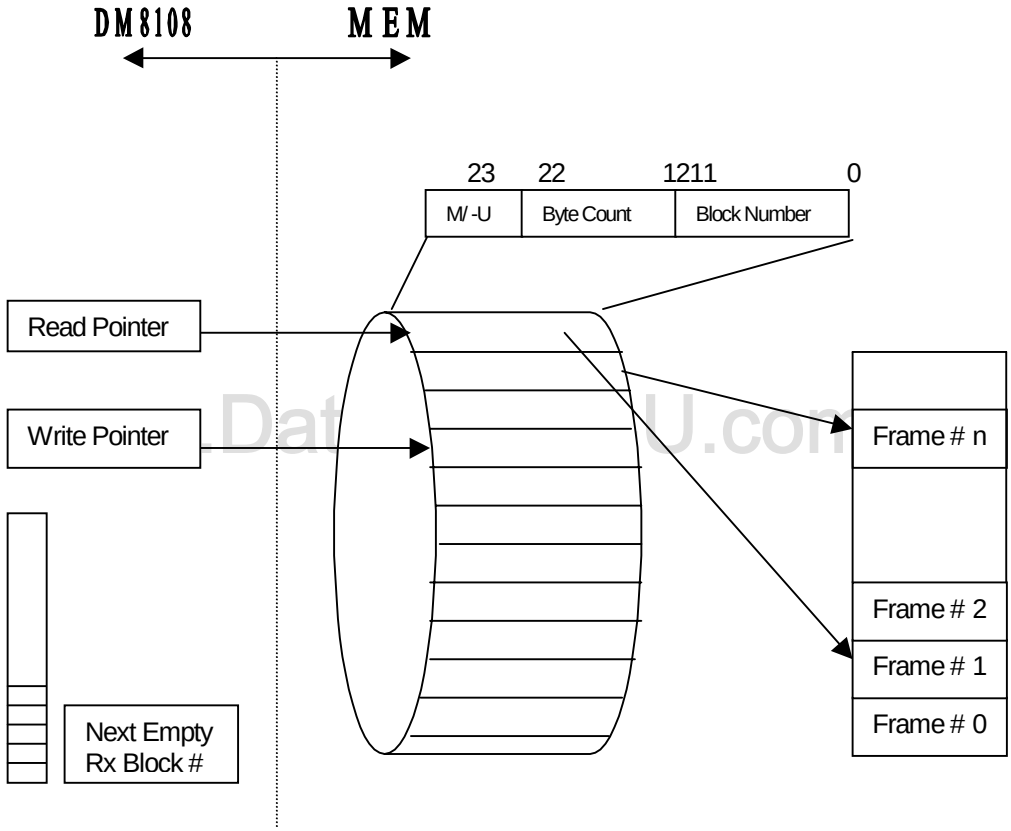
The DM8108 incorporates 3 transmit queues and one common receive buffer area for the two Fast Ethernet ports and the Expansion Port, The queues and buffers are located in the DRAM along with Address Table. The

DM8108 data structure components are the following:

- Receiving Buffer – a common receive buffer is allocated for each Fast Ethernet Receiving Port and Expansion Bus Receiving Port. The size of the receiving buffer is defined as 642KB (448 blocks) or 1728KB (1152 blocks) (depending on the DRAM size) of 1.5K Bytes each. The DM8108 allocates the buffers to the 8 Ethernet ports and the Expansion port.

- Transmit Descriptors (TxDR) – A set of 9 transmit descriptor rings. Each ring contains 512 descriptors. The Descriptor's size is 32-bit and contains the Receiving Buffer's Block Number, the packet length and the packet type (Multicast or Uni-cast). The Transmit Descriptors reside in the DRAM.

- Read/Write Pointers – 9 pairs of pointers to the Transmit Descriptors.



Empty List Tx Descriptors: 1K x 3 Receive Buffer

DM8108 DRAM Address Mapping

Queue & Buffers	Description	Memory Size	
		1M Byte	2M Byte
Receive Buffer	864KB (576 blocks) 1872KB (1248blocks) + unused	028000 – 0FFFFF	028000 – 1FFFFF
ACC Count	8KB	026000 – 027FFF	027000 – 027FFF
Reserved	4KB	025000 – 025FFF	025000 – 025FFF
TDR queue	20KB	020000 – 024FFF	020000 – 024FFF
Address Table	128KB	000000 – 01FFFF	000000 – 01FFFF

Address Table

The Address Table structure occupies 128K bytes of memory and is controlled and initialized by the DM8108. Following RESET, the DM8108 initializes the Address Table by invalidating the Valid bit of all entries.

Field	Description
V	Valid – Indicates a valid entry; 0 – Not Valid, 1 – valid.
Address (47:0)	Source MAC address. Unicast address only
Port #	Port Number – indicates which of the 3-port in a DM8108 is associated with this source address. 0h – 1h: Port 0 –Port 1 (2 Ethernet ports); 2h: Expansion Port.
Reserved	
Device #	Device number—indicate which device in the switching system is associated with this source address
Time Stamp	4-bit Tag—used to identify the update sequence. If the entry-block(4-entry) pointed by a MAC address index are all occupied, the entry that has oldest time stamp will be replaced.

Packet Forwarding

The following sections describe the procedures for forwarding packets under different situations:

Forwarding a Uni-cast packet to a local Ethernet port

The incoming packet is fed to the Rx FIFO and is transferred to an empty block in the Receive Buffer area of DRAM. The switching engine will claim the block by setting the Empty List not empty. In case of collision or FIFO overflow, transfer error etc . , the engine has to reset the Empty List associated with the block.

In parallel, an address recognition cycle will be performed for both the destination and source address. The DM8108 will use SA to learn a new or changed address entry. The DA will point to an entry that specifies the local port's number.

At the end of reception of an error-free packet, the packet information is written to the appropriate port's transmit descriptor. This information includes the Byte Count, Receive block address which points to the Write Pointer, and the Priority indication.

The Write Pointer of the outgoing port's transmit descriptor is incremented. The target port prepare for transmission whenever the Write Pointer and the Read pointer are not equal.

The engine resolves the priority issue and fills the Tx FIFO before starting the transmission. If any Tx FIFO under run situation happens, the MAC has to force the packet "Bad" and inform the engine to retry.

At the end of the good transmit process, the target port increments the Read Pointer. The Engine clears the appropriate bit in the Empty List.

Forward a Multicast, Broadcast and "Unknown" packet

If the received packet's DA is not found in the Address Table, or the packet is a Multicast or Broadcast packet, it will be treated as a Multicast packet, the switching engine will perform most of the steps mentioned above and forwards the packet to all ports.

DRAM Controller

The DM8108 includes direct support for Synchronous DRAM. The DRAM interface is entirely glue-less. All the accesses are performed as 32-bit. The memory controller is designed targeting up to 90-MHz.

The DM8108 refreshes the DRAM automatically.

Following the RESET, the DRAM controller will perform DRAM testing by write/read several patterns and invalidate all the entries in the Address Table. The DRAM test result is sent out through the LED status outputs.

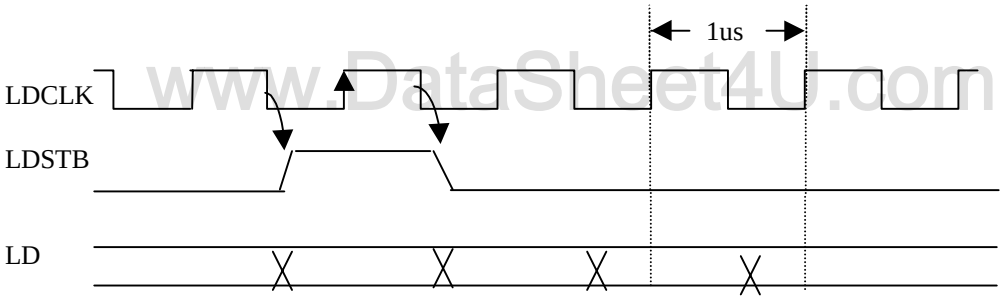
LED interface

The DM8108 provides LED data bus, address bus and strobe signals to:

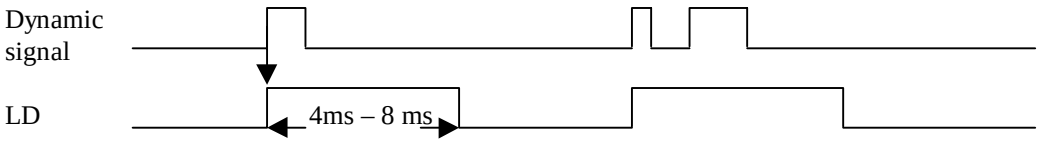
- Display the chip or ports' configuration and transfer status,
- Display the critical state signals for debug purpose.

LED signals definition

The following timing diagram shows the interface of LED bus while displaying LED signals.



For the LED signals having dynamic characteristics, the DM8108 will maintain the signal for a minimum of 4ms before sending to the LED bus if the state is triggered.



The following table shows the multiplexed LED signals.

Bit #	Signals	Bit #	Signals
1	Primary_port status 0 (link 0)	41	Transmit (4)
2	Primary_port status 1 (link 1)	42	Receiving (4)
3	Primary_port status 2 (link 2)	43	Collision (4)
4	Primary_port status 3 (link 3)	44	Rx buffer full (4)
5	Primary_port status 4 (link 4)	45	Reserved
6	Primary_port status 5 (link 5)	46	Reserved
7	Primary_port status 6 (link 6)	47	Full duplex (4)
8	Primary_port status 7 (link 7)	48	Port Speed (4)
9	Transmit (0)	49	Transmit (5)
10	Receiving (0)	50	Receiving (5)
11	Collision (0)	51	Collision (5)
12	Rx buffer full (0)	52	Rx buffer full (5)
13	Reserved	53	Reserved
14	Reserved	54	Reserved
15	Full duplex (0)	55	Full duplex (5)
16	Port Speed (0)	56	Port Speed (5)
17	Transmit (1)	57	Transmit (6)
18	Receiving (1)	58	Receiving (6)
19	Collision (1)	59	Collision (6)
20	Rx buffer full (1)	60	Rx buffer full (6)
21	Reserved	61	Reserved
22	Reserved	62	Reserved
23	Full duplex (1)	63	Full duplex (6)
24	Port Speed (1)	64	Port Speed (6)
25	Transmit (2)	65	Transmit (7)
26	Receiving (2)	66	Receiving (7)
27	Collision (2)	67	Collision (7)
28	Rx buffer full (2)	68	Rx buffer full (7)
29	Reserved	69	Reserved
30	Reserved	70	Reserved
31	Full duplex (2)	71	Full duplex (7)
32	Port Speed (2)	72	Port Speed (7)
33	Transmit (3)	73	Partition (0)
34	Receiving (3)	74	Partition (1)
35	Collision (3)	75	Partition (2)
36	Rx buffer full (3)	76	Partition (3)
37	Reserved	77	Partition (4)
38	Reserved	78	Partition (5)
39	Full duplex (3)	79	Partition (6)
40	Port Speed (3)	80	Partition (7)

81	Runt packet (0)	105	Link fail (0)
82	Runt packet (1)	106	Link fail (1)
83	Runt packet (2)	107	Link fail (2)
84	Runt packet (3)	108	Link fail (3)
85	Runt packet (4)	109	Link fail (4)
86	Runt packet (5)	110	Link fail (5)
87	Runt packet (6)	111	Link fail (6)
88	Runt packet (7)	112	Link fail (7)
89	Jab packet (0)	113	Pure_port_status(0)
90	Jab packet (1)	114	Pure_port_status(1)
91	Jab packet (2)	115	Pure_port_status(2)
92	Jab packet (3)	116	Pure_port_status(3)
93	Jab packet (4)	117	Pure_port_status(4)
94	Jab packet (5)	118	Pure_port_status(5)
95	Jab packet (6)	119	Pure_port_status(6)
96	Jab packet (7)	120	Pure_port_status(7)
97	Under_flow(0)	121	DRAM test status
98	Under_flow(1)	122	Internal SRAM test status
99	Under_flow(2)	123	Expansion Port RX buf. full
100	Under_flow(3)	124	Dynamic allocation buf. full
101	Under_flow(4)	125-128	Reserved
102	Under_flow(5)		
103	Under_flow(6)		
104	Under_flow(7)		

Strap Pins during Reset

The following table shows the strap pins during RESET.

Symbol	Description
LEDSTB	Strap pin during reset: 0= force link, 1= link detection through serial MII (default)
LEDD	Strap pin for TXENCLK frequency of expansion port: 0=fast, 1= slow (default)
TXD0[3:0]	TXD0[0]: Strap pin for the operating frequency 0=88Mhz; 1= 66Mhz (default) TXD0[1]: Strap pin to enable partition mode 0=enable; 1=disable (default) TXD0[2]: Strap pin to enable expansion port 0=enable; 1=disable (default) TXD0[3]: Strap pin to enable BIST 0=init only; 1=enable (default)
TXD1[3:0]	TXD1[2:0]: test function TXD1[3]: disable CRC checking 0= disable; 1=enable (default)
TXD2[3:0]	Strap pins during reset: TXD2[2:0] = device # setting TXD2[3] strapped for DRAM timing: 0=fast, 1= normal (default)
TXD3[3:0]	Strap pin during reset: TXD3[0] Max packet size selection: 0 = 1536 bytes, 1=1518 bytes (default) TXD3[1] Back pressure and flow control enable: 0 = enable, 1 = disable (default) TXD3[3:2] aging timing selection: 00 – 64sec. 01 –12 8 sec. 10 – 256 sec. 11 – disable (default)
TXD4[3:0]	Strap pin during reset: TXD4[0] port 0 trunking selection: 0 = enable, 1=disable (default) TXD4[1] port 1 trunking selection: 0 = enable, 1=disable (default) TXD4[2] port 2 trunking selection: 0 = enable, 1=disable (default) TXD4[3] port 3 trunking selection: 0 = enable, 1=disable (default)
TXD5[1:0]	Strap pin during reset: TXD5[1:0] broadcast filtering rate selection: 00 = 8k packets/sec. 01 = 16k packets/sec. 10 = 64k packets/sec. 11 = disable (default)
TXEN(7:0)	Strap pins during reset for ports' operating mode: 0= full duplex, 1=half duplex (default)
MA9	Strap pin during reset: 0= limit4 enabled, 1= disabled (default)
MA8	Strap pin during reset for memory size selection: 0= 2MB, 1= 1MB (default)
MA(7:0)	Strap pins during reset: MA7-0: Auto-negotiation enable for port0: 0= enabled (default), 1 = disabled

Absolute Maximum Ratings

Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
Vcc	Supply voltage	-0.3	3.6	V	
Vi	Input voltage	-0.3	5.25	V	
Vo	Output voltage	-0.3	Vcc + 0.3	V	
Io	Output Current	2	24	mA	
Iik	Input protection diode current			mA	
Iok	Output protection diode current			MA	
Tc	Operating temperature	0	70	C	
Tstg	Storage temperature	-40	125	C	
ESD	Static Discharge voltage	2000		V	

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
Vcc	Supply voltage	3.3	3.6	V	
Vi	Input voltage	0	Vcc	V	
Vo	Output voltage	0	Vcc	V	
Tc	Operating temperature	0	70	C	
Cin	Input Capacitance			pF	
Cout	Output Capacitance			pF	

Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (0°C<TA<70°C, 3.135<VCC<3.465, unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit	Conditions
Vih	Input high voltage	2.0		V	
Vil	Input low voltage		0.8	V	
Voh	Output high voltage	2.4	Vcc	V	
Vol	Output low voltage	0	0.4	V	
Iih	Input high current		±1	uA	
Iil	Input low current		±1	uA	
Ioz	Output high impedence current		±1	uA	
Icc	Operating Current		TBD	mA	

Thermal Information

Symbol	Parameter	Value
θja	Thermal resistance: junction to ambient; 0 ft/s airflow	42 °C/W
θjc	Thermal resistance: junction to case; 0ft/s airflow	TBD
Tj	Operating junction temperature	125 °C
Cin	Input Capacitance	

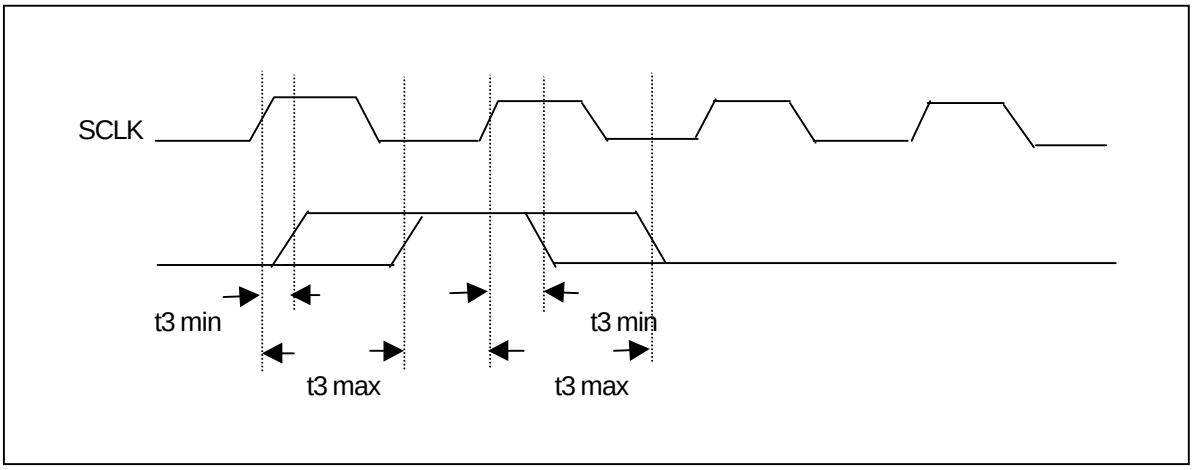
AC Electrical Characteristics & Timing Waveforms

(Tc = 0 – 70 °C; Vcc = 3.3V ± 5%)

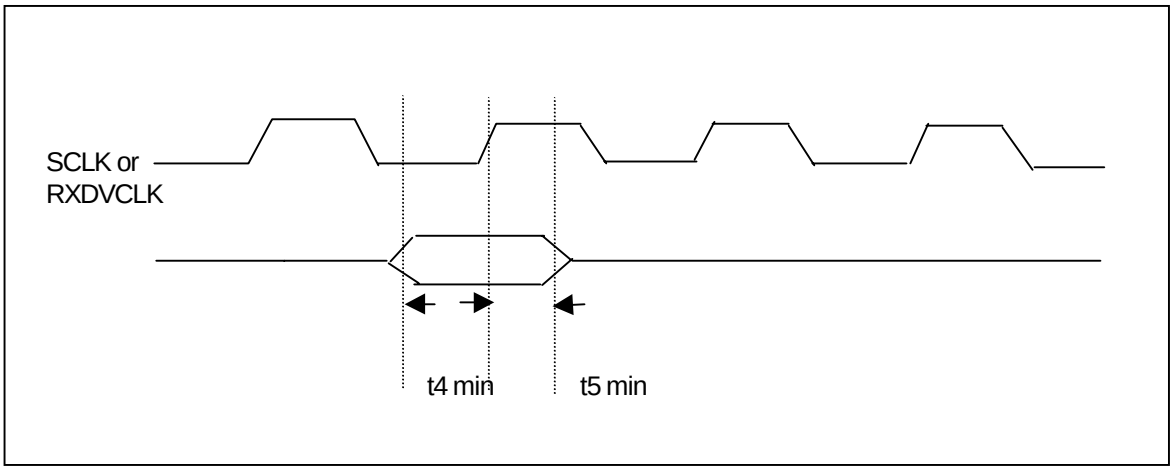
Symbol	Signals	Parameter	Min.	Max.	Unit	Conditions
	SCLK	System Clock frequency	66	90	MHz	
	SCLK	Rise/Fall time	1	4	ns	
	RST*	Reset pulse width	2		SCLK	
t3	MA, MD, CAS*, RAS*,DWE*, SDQM, SCS*,SRAS*, SCAS*	Delay from SCLK rising or falling edge	2	8	ns	
t4	MD, RXD8 (1)	Setup time	2		ns	
t5	MD, RXD8 (2)	Hold time	2		ns	
t6	MD	Float delay	2	8	ns	
t7	MD, TXD8 (3)	Drive delay	2	8	ns	

Notes:
1. MD is related to SCLK; RXD8 is related to RXDVCLK.
2. MD is related to SCLK; TXD8 is related to TXENCLK.
3. All Delays, Setup, and Hold times are referred to SCLK rising edge unless stated otherwise.
4. All outputs are specified for 25 pF load.
5. All inputs and outputs also refer to I/O signal behavior.

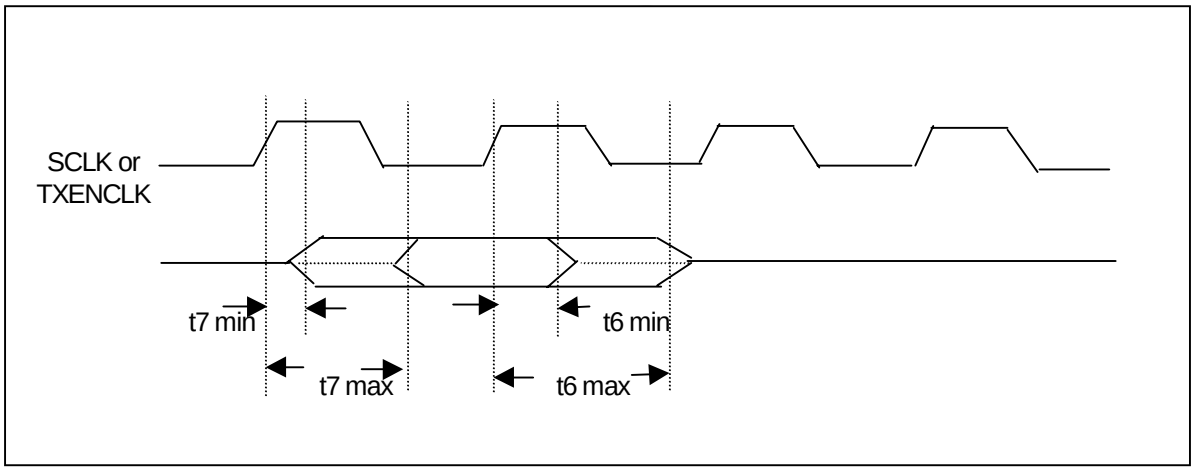
Output Delay from Rising Edge



Setup and Hold time from Rising Edge



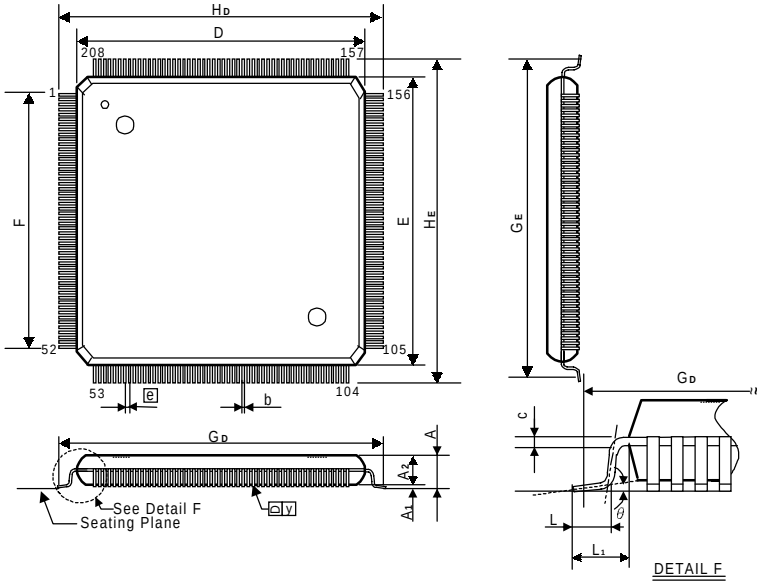
Drive or Float Delay from Rising Edge



Package Information

QFP 208L Outline Dimensions

unit: inches/mm

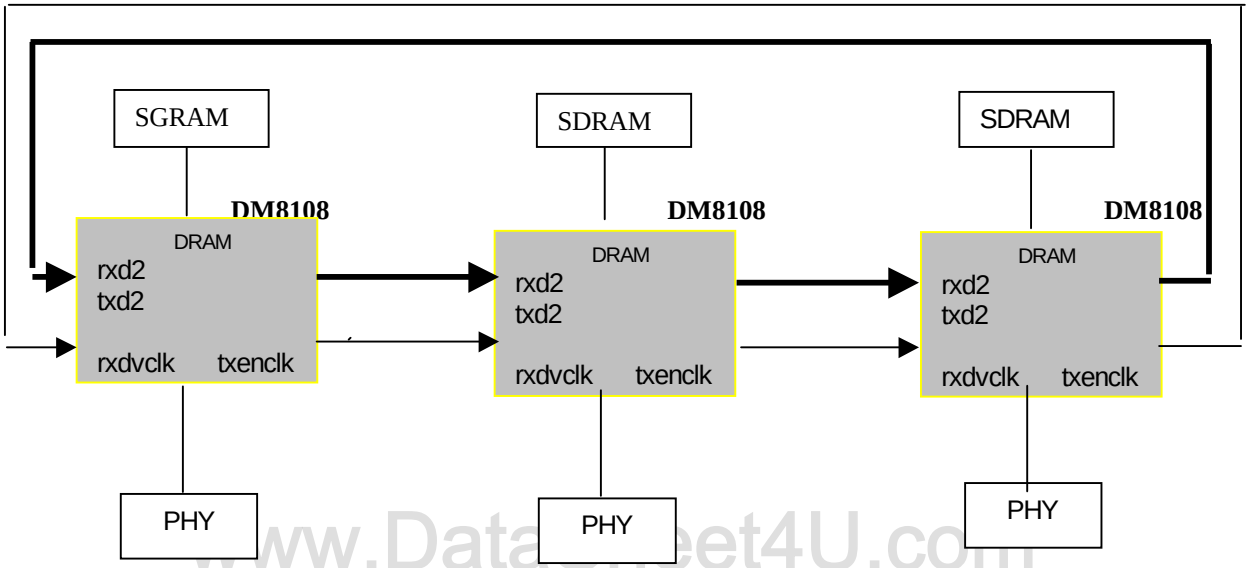


Symbol	Dimensions in inches	Dimensions in mm
A	0.145 Max.	3.68 Max.
A1	0.004 Min.	0.10 Min.
A2	0.127 ± 0.005	3.23 ± 0.13
b	0.008 +0.002 -0.002	0.20 +0.05 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	1.102 ± 0.005	28.00 ± 0.13
E	1.102 ± 0.005	28.00 ± 0.13
e	0.020 ± 0.004	0.50 ± 0.10
F	1.004 NOM.	25.5 NOM.
GD	1.185 NOM.	30.10 NOM.
GE	1.185 NOM.	30.10 NOM.
HD	1.205 ± 0.012	30.60 ± 0.30
HE	1.205 ± 0.012	30.60 ± 0.30
L	0.019 ± 0.008	0.50 ± 0.20
L1	0.051 ± 0.008	1.30 ± 0.20
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions F, GD, GE are for PC Board surface mount pad pitch design reference only.

Appendix: Cascade Three DM8108s to a 24-port Switch Illustration



Ordering Information

Part Number	Pin Count	Package
DM8108	208	QFP

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Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.