TRI-STATE® 8-Bit Latches

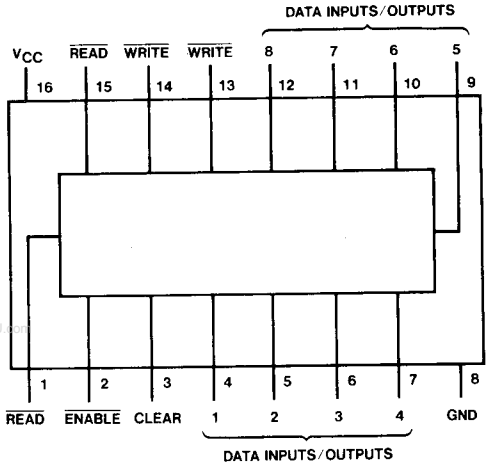
General Description

By utilizing TRI-STATE circuitry on the outputs, the inputs and outputs can be accessed on the same pins, and these circuits provide eight separate $\overline{R}$-$\overline{S}$ latches in the popular 16-pin package. While in the high-impedance state, the inputs and outputs are disabled and no information can be entered. When both $\overline{WRITE}$ inputs are brought to a low logic level, the outputs are disabled and new information may be entered at the inputs. When a low logic level is applied to both $\overline{READ}$ inputs, and a high logic level to both $\overline{WRITE}$ inputs, the inputs are rendered inactive and data may be read from the outputs.

Features

- TRI-STATE I/O pins
- 8 latches in popular 16-pin package
- Typical propagation delay—22 ns

Connection Diagram



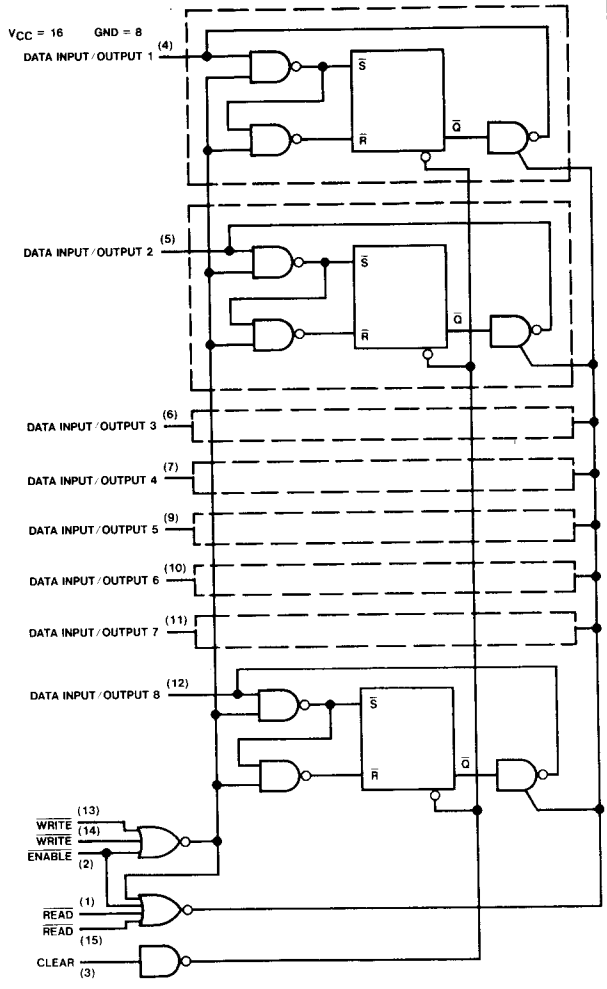
7553 (J,W); 8553 (N)

Truth Table

Clear	Enable	Read*	Write**	Operation	State of Bus
H	L	L	H	Enter L	L
H	L	L	L	Enter L	Hi-Z
L	X	H	H	Do Nothing	Hi-Z
L	H	X	X	Do Nothing	Hi-Z
L	L	X	L	Write	H or L ***
L	L	L	H	Read	H or L ***

*Both Read Inputs
**Both Write Inputs
***Depends on State of Latch

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	DM75 53 Min	DM75 53 Typ (1)	DM75 53 Max	DM85 53 Min	DM85 53 Typ (1)	DM85 53 Max	Units
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High Level Output Current				−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = Max	2.4			2.4			V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 0.4 V			−40			−40	μA
		V_{CC} = Max, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 2.4 V			40			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)	−28		−70	−28		−70	mA
I_{CC}	Supply Current	V_{CC} = Max		66	93		66	93	mA

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter			From (Input)	To (Output)	Conditions	DM75/85 53 Min	DM75/85 53 Typ	DM75/85 53 Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		Clear	Output	C_L = 50 pF, R_L = 400 Ω		21	32	ns
t_{ZH}	Output Enable Time to High Level		Enable	Output			22	33	ns
t_{ZL}	Output Enable Time to Low Level		Enable	Output			25	38	ns
t_{HZ}	Output Disable Time from High Level		Enable	Output	C_L = 5 pF, R_L = 400 Ω		7	12	ns
t_{LZ}	Output Disable Time from Low Level		Enable	Output			20	30	ns
t_W	Minimum Pulse Width	Clear				15	10		ns
		$\overline{\text{Write}}$				40	28		
t_{SETUP}	Minimum Data Setup Time	High Level				20	14		ns
		Low Level				36	26		
t_{HOLD}	Minimum Data Hold Time	High Level				−15	−26		ns
		Low Level				−8	−14		