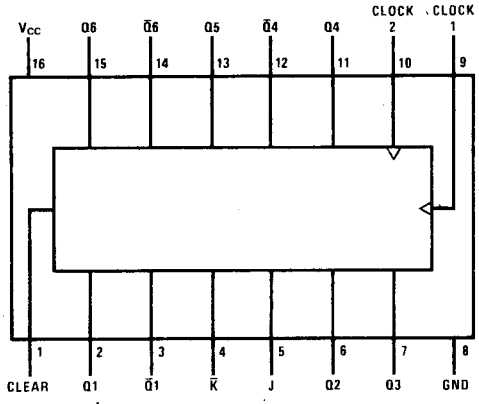
General Description

These 6-bit shift registers feature J-$\overline{K}$ serial inputs, parallel outputs, and a direct overriding clear. All inputs are buffered to lower the input drive requirements to one standard DM74S load. Furthermore, shifting is synchronous, and occurs on the positive-going edge of the clock pulse. These shift registers are particularly well-suited for very high speed data processing systems.

Connection Diagram

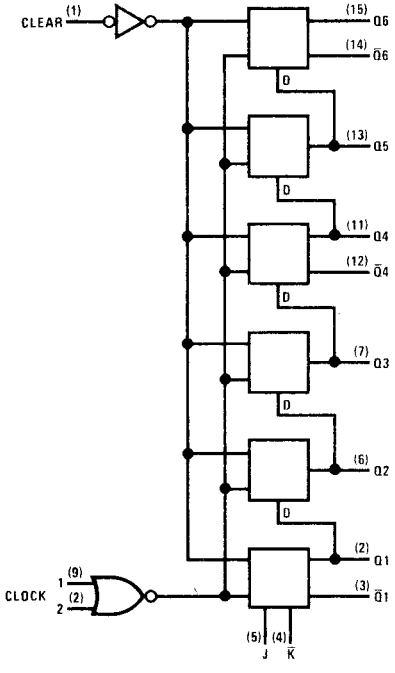


Truth Table

INPUTS					OUTPUTS					
CLEAR	CLOCKS 1	CLOCKS 2	J	$\overline{K}$	Q1	Q2	Q3	Q4	Q5	Q6
L	X	X	X	X	L	L	L	L	L	L
H	L	L	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	L	H	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	H	L	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	H	H	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	↑	L	L	L	L	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	L	L	H	$Q1_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	L	H	L	$\overline{Q1}_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	L	H	H	H	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	L	L	L	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	L	H	$Q1_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	H	L	$\overline{Q1}_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	H	H	H	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	H	X	X	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$	$Q6_N$
H	H	↑	X	X	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$	$Q6_N$

$Q1_0$, $Q2_0$, etc. = The level of Q1, Q2, etc. before the indicated steady-state input conditions were established.
$Q1_N$, $Q2_N$, etc. = The level of Q1, Q2, etc. before the most-recent ↑ transition of the clock; indicates a 1-bit shift.

Logic Diagram



To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM85S S50 MIN	DM85S S50 TYP(1)	DM85S S50 MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{OH}	High Level Output Current				−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	2.7	3.4		V
I_{OL}	Low Level Output Current				20	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max		90	150	mA

Notes
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM85S S50 MIN	DM85S S50 TYP	DM85S S50 MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 280Ω	75	110		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q or $\overline{Q}$			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Q or $\overline{Q}$			12	18	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clear	$\overline{Q}$			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q			13	20	ns