DAVICOM Semiconductor, Inc.

DM8606BF

6-Port Fast Ethernet
Single Chip Switch Controller

DATA SHEET

Preliminary
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Chapter 1 Product Overview

1.1 Overview

The DM8606BF is a high performance, low cost, highly integrated (Controller, PHY and Memory) four-port 10/100 Mbps TX/FX plus two 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex. The DM8606BF is intended for applications to stand alone bridge for low cost SOHO markets such as 5Port, Router applications. The 2nd MAC can be configured as PCS type MII with 10/100 PHY integrated.

DM8606BF provides the most advance functions such as: 802.1p(Q.O.S.), 802.1q(VLAN), Port MAC address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra MII port functions to meet customer requests on Switch demand.

The DM8606BF also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffers are full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the DM8606BF will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in SRAM used for the packet buffer and address learning table is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

DM8606BF also supports priority features by Port-Base, VLAN and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN are also supported.

An intelligent address recognition algorithm allows DM8606BF to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by DM8606BF to use on Building Internet access to prevent multiple users sharing one port traffic.

1.2 Features

- Supports five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces and one MII/GPSI/RMII port.
- Supports 2K MAC addresses table with 4-ways associative hash algorithm.
- Supports four queue for QoS
- Supports priority features by Port-Based, Application-Based, Diffserv, 802.1p VLAN, IP TOS of packets.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports per port Single/Dual color mode with Power On auto diagnostic. Collision/Duplex LED can be separate by register setting.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1518/1522 (Default)/1536/>1536 bytes.
- Scalable Per Port Bandwidth Control (Both Ingress and Egress) .(Step = 64K, up to 100M)
- Broadcast Storming Filter function.
- Supports 802.1Q VLAN. Up to 16 VLAN groups is implemented by full 12 bits VID matching.
- Support MAC clone function to enable multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Interrupt pin , Interrupt Register and Interrupt Mask Register. Programmable interrupt polarity (Default active low)
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count.
- Support 32 hardware IGMP Table (Multicast Table)
- MAC Address Table is Accessible.
- Support 802.1x.
- Support Spanning Tree Protocol
- Support internal counter/PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8V/3.3V power supply.
- 1.0w low power consumption.

1.3 Applications

DM8606BF in 128-pin PQFP: SOHO 5-port switch
5-port switch + Router with MII CPU interface.

1.4 Block Diagram

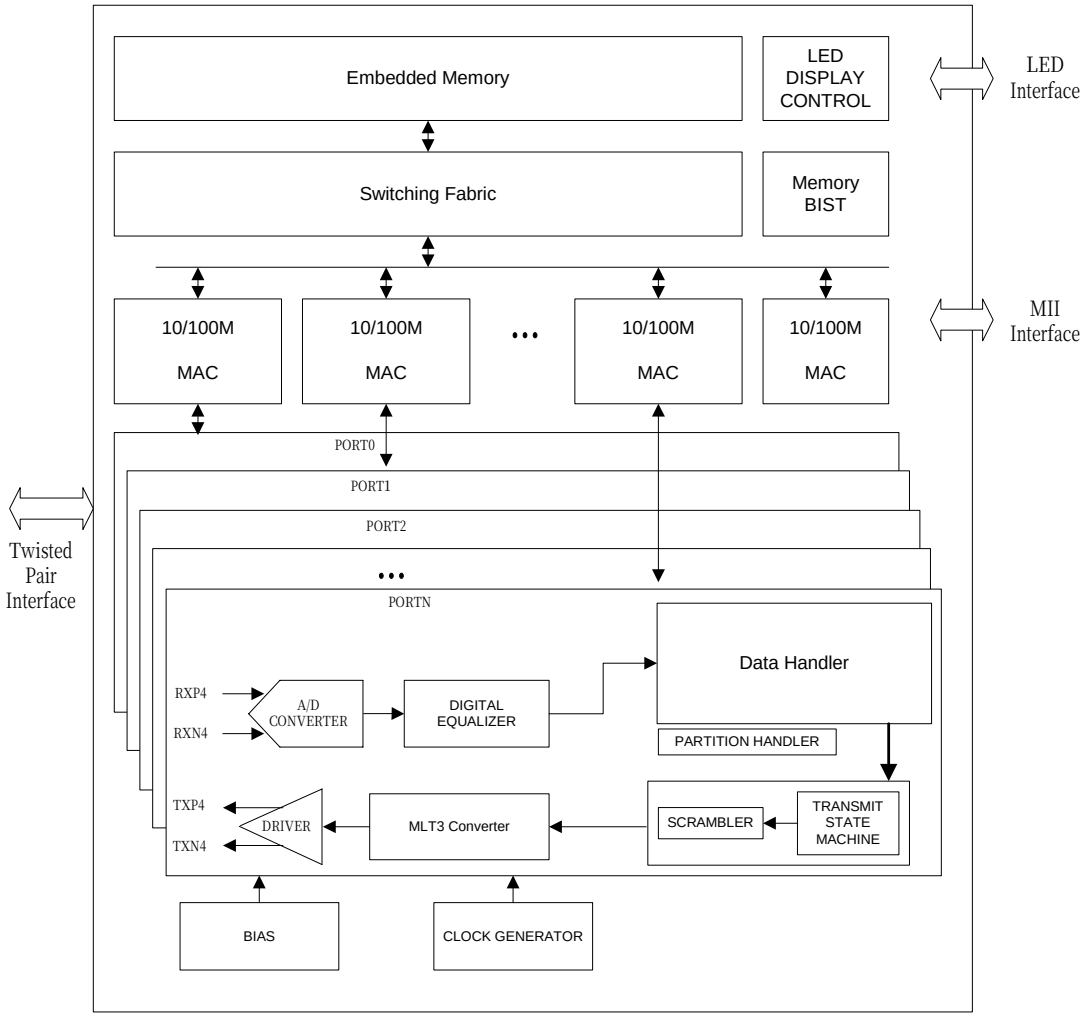


Figure 1-1 DM8606BF Block Diagram

1.5 Abbreviations

BER	Bit Error Rate
CFI	Canonical Format Indicator
COL	Collision
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CS	Chip Select
DA	Destination Address
DI	Data Input
DO	Data Output
EDI	EEPROM Data Input
EDO	EEPROM Data Output
EECS	EEPROM Chip Select
EESK	EEPROM Clock
ESD	End of Stream Delimiter
FEFI	Far End Fault Indication
FET	Field Effect Transistor
FLP	Fast Link Pulse
GND	Ground
GPSI	General Purpose Serial Interface
IPG	Inter-Packet Gap
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller
MDIX	MDI Crossover
MII	Media Independent Interface
NRZI	Non Return to Zero Inverter
NRZ	Non Return to Zero
PCS	Physical Coding Sub-layer
PHY	Physical Layer
PLL	Phase Lock Loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
QoS	Quality of Service
QFP	Quad Flat Package
RST	Reset
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Errors
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
SA	Source Address
SOHO	Small Office Home Office
SSD	Start of Stream Delimiter

SQE	Signal Quality Error
TOS	Type of Service
TP	Twisted Pair
TTL	Transistor Transistor Logic
TXCLK	Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXN	Transmission Negative
TXP	Transmission Positive

1.6 Conventions

1.6.1 Data Lengths

qword	64-bits
dword	32-bits
word	16-bits
byte	8 bits
nibble	4 bits

1.6.2 Pin Types

Pin Type	**Description**
I	Input
O	Output
I/O	Bi-directional
OD	Open drain
SCHE	Schmitt Trigger
PD	internal pull-down
PU	internal pull-up

1.6.3 Register Types

Register Type	**Description**
RO	Read-only
WO	Write-only
RW	Read/Write

Chapter 2 Interface Description

2.1 Pin Diagram

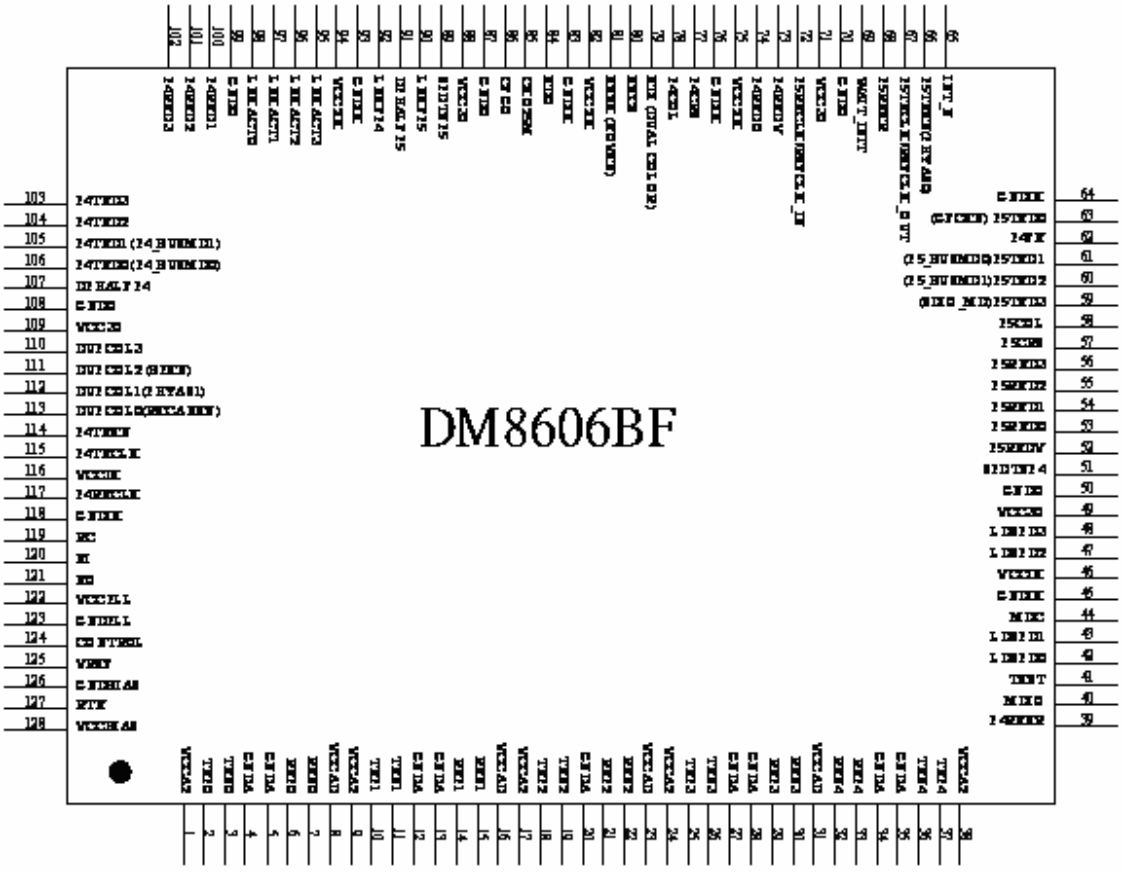


Figure 2-1 4 TP/FX PORT + 2 MII PORT 128 Pin Diagram

2.2 Pin Description by Function

DM8606BF pins are categorized into one of the following groups:

- Section 2.2.1 Network Media Connection
- Section 2.2.2 Port 4 MII Interface
- Section 2.2.3 Port 5 MII Interface
- Section 2.2.4 LED Interface
- Section 2.2.5 EEPROM Interface
- Section 2.2.6 Power/Ground, 48 pins
- Section 2.2.7 Miscellaneous

Note:
"Section 1.6.2 Pin Types" can be used for reference.

2.2.1 Network Media Connection

Pad Name	Pad#	Type	Descriptions
RXP[4:0] RXN[4:0]	6, 14, 21, 29, 33 7, 15, 22, 30, 32	IO ANA IO ANA	Receive Pair. Differential data is received on this pin.
TXP[4:0] TXN[4:0]	2, 10, 18, 25, 37 3, 11, 19, 26, 36	IO ANA IO ANA	Transmit Pair. Differential data is transmitted on this pin.

2.2.2 Port 4 MII Interface

Pad Name	Pad#	Type	Descriptions
MMII_P4RXD0	74	I, LVTTL	Port 4 MII Port Receive Data bit 0. In MAC MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MMII_P4RXCLK.
HDLC_P4RXD			HDLC Receive Data. When port 4 is operating in HDLC mode, this pin is acts as Receive Data Input and synchronous to the rising edge of HDLC_P4RXCLK.
PMII_P4RXD0		O, 8mA	Port 4 MII Port Receive Data bit 0. When port 4 is operating in PCS MII mode, the bit is the LSB of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.

Pad Name	Pad#	Type	Descriptions
MMII_P4RXD[3:1]	102,101,100	I, LVTTL	Port 4 MII Port Receive Data bit 3 ~ 1. In MAC MII mode, these pins are bit[3:1] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
PMII_P4RXD[3:1]		O, 8mA	Port 4 MII Port Receive Data bit 3 ~ 1. When port 4 is operating in PCS MII mode, these pins are bit[3:1] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
MMII_P4RXDV	73	I, LVTTL	Port 4 MII Port Receive Data Valid. Active high to indicate that the data on MMII_P4RXD[3:0] is valid. Synchronous to the rising edge of MMII_P4RXCLK.
PMII_P4RXDV		O, 8mA	Port 4 MII Port Receive Data Valid. When port 4 is operating in PCS MII mode, this pin is an active high output signal to indicate PMII_P4RXD[3:0] is valid. Synchronous to the rising edge of PMII_P4RXCLK.
MII_P4RXER	39	I, LVTTL	Port 4 MII Receive Error. Active high to indicate that there is error on the MII_P4RXD[3:0]. Upon receiving this signal, DM8606BF will send Error Symbol onto the medium. Only valid in 100M operation.
MMII_P4CRS	77	I, LVTTL	Port 4 MII Port Carrier Sense. In full duplex mode, CRS_P4 reflects the receive carrier sense situation on medium only; In Half Duplex, CRS will be high both in receive and transmit condition.
PMII_P4CRS		O, 8mA	Port 4 MII Port Carrier Sense. When port 4 is operating in PCS MII mode, this pin is used to output Carrier Sense status.
MMII_P4COL	78	I, LVTTL	Port 4 MII Port Collision input. Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
PMII_P4COL		O, 8mA	Port 4 MII Port Collision input. When port 4 is operating in PCS MII mode, this pin is used to output collision status.
Power On Setting P4_BUSMD0	106	I,PD, LVTTL	Port 4 Bus Type Configuration 0. Value on this pin will be latched by DM8606BF at the rising edge of RESETL for Port 4 Configuration Bit 0. Combined with CFG and P4_BUSMD1, DM8606BF provides 4 bus type for port 4. See CFG pin description for more detail.
MMII_P4TXD0		O, 8mA	Port 4 MII Transmit Data bit 0. The LSB bit of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
HDLC_P4TXD			Port 4 HDLC Transmit Data. When port 4 is operating in HDLC mode, this pin acts as HDLC Transmit Data. Synchronous to the rising edge of HDLC_P4TXCLK.
PMII_P4TXD0		I,PD, LVTTL	Port 4 MII Transmit Data bit 0. When port 4 is operating in PCS MII mode, this pin is the LSB of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.

Pad Name	Pad#	Type	Descriptions
Power On Setting P4_BUSMD1	105	I,PD, LVTTL	Port 4 Bus Type Configuration 1. Value on this pin will be latched by DM8606BF at the rising edge of RESETL for Port 4 Configuration Bit 1. Combined with CFG and P4_BUSMD0, DM8606BF provides 4 bus type for port 4, See CFG for more detail
MMII_P4TXD1		O, 8mA	Port 4 MII Transmit Data bit 1. The second bit of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
PMII_P4TXD1		I,PD, LVTTL	Port 4 MII Transmit Data bit 1. When port 4 is operating in PCS MII mode, this pin is second bit of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
MMII_P4TXD[3:2]	103,104	O, 8mA	Port 4 MII Transmit Data bit 3 ~ 2. The bit [3:2] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
PMII_P4TXD[3:2]		I, LVTTL	Port 4 MII Transmit Data bit 3 ~ 2. When port 4 is operating in PCS MII mode, these pins are bit[3:2] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
MMII_P4TXEN	114	O, 8mA	Port 4 MII Transmit Enable. Output by DM8606BF at the rising edge of MMII_P4TXCLK when DM8606BF is programmed to MAC Type MII;
PMII_P4TXEN		I, LVTTL	Port 4 MII Transmit Enable. It is input to DM8606BF when programmed to PCS Type MII.
MMII_P4RXCLK	117	I, LVTTL	Port 4 MII Port Receive Clock. 25M Free Running clock in 100M Mode and 2.5M free running clock in 10M Mode. MMII_P4RXDV and MMII_P4RXD[3:0] should synchronous to the rising edge of this clock
HDLC_P4RXCLK			Port 4 MII Port/HDLC Receive Clock Input.
PMII_P4RXCLK		O, 8mA	Port 4 MII Port Receive Clock. 25M Free Running clock in 100M Mode and 2.5M free running clock in 10M Mode. PMII_P4RXDV and PMII_P4RXD[3:0] should synchronous to the rising edge of this clock
MMII_P4TXCLK	115	I, LVTTL	Port 4 MII Port Receive Clock. 25M Free Running clock in 100M Mode and 2.5M free running clock in 10M Mode. MMII_P4TXEN and MMII_P4TXD[3:0] should synchronous to the rising edge of this clock
HDLC_P4TXCLK			Port 4 HDLC Transmit clock Input.
PMII_P4TXCLK		O, 8mA	Port 4 MII Port Receive Clock. 25M Free Running clock in 100M Mode and 2.5M free running clock in 10M Mode. PMII_P4TXEN and PMII_P4TXD[3:0] should synchronous to the rising edge of this clock
SPDTNP4	51	I,PD, LVTTL	Port 4 Speed Input: 0 : 100M 1 : 10M

Pad Name	Pad#	Type	Descriptions
LNKFP4	92	I,PD, LVTTL	Port 4 Link Fail Status Input. 0 : Link Up 1 : Link Failed
DPHALFP4	107	I,PD, LVTTL	Port 4 Duplex status Input. 0 : Full Duplex 1 : Half Duplex
P4FX	62	I,PD, LVTTL	Port 4 Fiber Selection. During power on reset, value will be latched by DM8606BF at the rising edge of RESETL as P4 Fiber select. 0 : Twisted Pair Mode 1 : Fiber Mode

2.2.3 Port 5 MII Interface

Pad Name	Pad#	Type	Descriptions
Power On Setting GFCEN	63	I,PU, LVTTL	Global Flow Control Enable. Value on this pin will be latched by DM8606BF at the rising edge of RESETL as Flow control enable. 0 : Flow Control Capability is depended upon the register setting in corresponding EEPROM register 1 : All ports flow control capability is enabled.
MII_P5TXD0		O, 4mA	Port 5 MII Transmit Data bit 0. The LSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
GPSI_P5TXD		O, 4mA	In GPSI Mode, Transmit Data.. When port 5 is operating in GPSI mode, this pin acts as GPSI Transmit Data. Synchronous to the rising edge of GPSI_P5TXCLK.
RMII_P5TXD0		O, 4mA	Port 5 RMII Transmit Data bit 0.. When port 5 is operating in RMII mode, this pin acts as RMII Transmit Data Bit [0]. Synchronous to the rising edge of REFCLK_IN.
Power On Setting P5_BUSMD[0]	61	I,PD, LVTTL	Port 5 bus mode selection bit 0. Value on this pin will be latched by DM8606BF at the rising edge of RESETL as port 5 bus mode selection bit 0. P5_BUSMD[1:0] Interface 00 MII 01 GPSI 10 RMII 11 Reserved and Not Allowed.
MII_P5TXD1		O, 4mA	Port 5 MII Transmit Data bit 1. The Second bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
RMII_P5TXD1		O, 4mA	Port 5 RMII Transmit Data bit 1. The Second bit of RMII Transmit data of port 5. Synchronous to the rising edge of REFCLK_IN.

Pad Name	Pad#	Type	Descriptions
Power On Setting P5_BUSMD[1]	60	I,PD, LVTTL	Port 5 bus mode selection bit 1. Value on this pin will be latched by DM8606BF at the rising edge of RESETL as port 5 bus mode selection bit 1.
MII_P5TXD2		O, 4mA	Port 5 MII Transmit Data bit 2. The Third bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
Power On Setting SDIO_MD	59	I,PD, LVTTL	SDC/SDIO mode selection. Value on this pin will be latched by DM8606BF at the rising edge of RESETL as SDC/SDIO control signal which is used to select 16 bits or 32 bits mode. 0 : 32 bits mode 1 :.16 bits mode
MII_P5TXD3		O, 4mA	Port 5 MII Transmit Data bit 3. The MSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
Power On Setting PHYAS0	66	I,PD, LVTTL	PHY Address MSB bit 0. During power on reset, value will be latched by DM8606BF at the rising edge of RESETL as PHY start address select. PHYAD E2PRM Master
MII_P5TXEN		O, 8mA	Port 5 MII Transmit Enable TXEN. Active high to indicate that the data on MII_P5TXD[3:0] is valid. Synchronous to the rising edge of MII_P5TXCLK.
GPSI_P5TXEN		O, 8mA	Port 5 GPSI Transmit Enable TXEN. Active high to indicate that the data on GPSI_P5TXD is valid. Synchronous to the rising edge of GPSI_P5TXCLK.
RMII_P5TXEN		O, 8mA	Port 5 RMII Transmit Enable TXEN. Active high to indicate that the data on RMII_P5TXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
MII_P5RXD0	53	I, LVTTL	Port 5 MII Receive Data bit 0. In MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
GPSI_P5RXD			Port 5 GPSI Receive Data. In GPSI Mode, this acts as Receive Data Input, synchronous to the rising edge of GPSI_P5RXCLK.
RMII_P5RXD0			Port 5 RMII Receive Data bit 0. In RMII mode, the bit is the LSB of RMII receive data, synchronous to the rising edge of REFCLK_IN.
MII_P5RXD1	54	I, LVTTL	Port 5 MII Port Receive Data bit 1. In MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
RMII_P5RXD1			Port 5 RMII eceive Data bit 1. In RMII mode, the bit is the MSB of RMII receive data, synchronous to the rising edge of REFCLK_IN.

Pad Name	Pad#	Type	Descriptions
MII_P5RXD[3:2]	56,55	I, LVTTL	Port 5 MII Receive Data bit 2 ~ 1. Combined with MII_P5RXD[1:0] to form MII Receive Data. Synchronous to the rising edge of MII_P5RXCLK.
MII_P5RXDV RMII_P5CRSDV	52	I, LVTTL	Port 5 MII receive Data Valid. Active high to indicate that the data on MII_P5RXD[3:0] is valid. Synchronous to the rising edge of MII_P5RXCLK. Port 5 RMII Carrier Sense and Receive Data Valid. Active high to indicate that the data on RMII_P5RXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
MII_P5RXER RMII_P5RXER	68	I, LVTTL	Port 5 MII Receive Error. Active high to indicate that there is error on the MII_P5RXD[3:0]. Upon receiving this signal, DM8606BF will send Error Symbol onto the medium. Only valid in 100M operation. Port 5 RMII Receive Error. Active high to indicate that there is error on the RMII_P5RXD[1:0]. Upon receiving this signal, DM8606BF will send Error Symbol onto the medium. Only valid in 100M operation.
MII_P5CRS GPSI_P5CRS	57	I, LVTTL	Port 5 MII Carrier Sense. In full duplex mode, MII_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, MII_P5CRS will be high both in receive and transmit condition. Port 5 GPSI Carrier Sense. In full duplex mode, GPSI_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, GPSI_P5CRS will be high both in receive and transmit condition.
MII_P5COL GPSI_P5COL	58	I, LVTTL	Port 5 MII Collision input. Active high to indicate that there is collision on the medium. Stay low in full duplex operation. Port 5 GPSI Collision input. Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
MII_P5RXCLK GPSI_P5RXCLK REFCLK_IN	72	I, LVTTL	Port 5 MII Port Receive Clock Input. MII_P5RXDV and MII_P5RXD[3:0] are synchronous to the rising edge of this clock. It is free running 25M clock in 100M mode and 2.5M clock in 10M mode. Port 5 GPSI Port Receive Clock Input. GPSI_P5RXD are synchronous to the rising edge of this clock. It is non-continuous 10M Clock input. 50M Reference Clock Input. RMII_P5RXD[1:0], RMII_P5TXD[1:0], RMII_P5TXEN and RMII_P5CRSDV are synchronous to the rising edge of this clock.

Pad Name	Pad#	Type	Descriptions
MII_P5TXCLK	67	I, LVTTL	Port 5 MII Port Transmit clock Input. MII_P5TXEN and MII_P5TXD[3:0] are output at the rising edge of this clock. It is free running 25M clock in 100M mode and 2.5M clock in 10M mode.
GPSI_P5TXCLK			Port 5 GPSI Port Transmit Clock Input. GPSI_P5TXEN and GPSI_P5TXD are synchronous to the rising edge of this clock. It is continuous 10M Clock input.
RMII_REFCLK_OUT		O, 8mA	50M Reference Clock Output.
SPDTNP5	89	I,PD, LVTTL	Port 5 Speed Input: 0 : 100M 1 : 10M
LNKFP5	90	I,PD, LVTTL	Port 5 Link Fail Status Input. 0 : Link Up 1 : Link Failed
DPHALFP5	91	I,PD, LVTTL	Port 5 Duplex status Input. 0 : Full Duplex 1 : Half Duplex

2.2.4 LED Interface

Pad Name	Pad#	Type	Descriptions
DUPCOL3	110	O,PD, 8mA	Port 3 Duplex/Collision LED. In Full duplex mode, this pin acts as DUPLEX LED for port 3, respectively; in half duplex mode, it is collision LED for each port. See Table 3 for mode detail. Note that DUPLEX and Collision can be separated by the register definition in PHY register.
Power On Setting BPEN	111	I,PU, LVTTL	Recommend Back-Pressure in half-duplex. Value on this pin will be latched by DM8606BF during power on reset as the beck-pressure enable in half-duplex mode. 0 : Disable Back-Pressure. 1 : Enable Back-Pressure
DUPCOL2		O 8mA	Port 2 Duplex-collision LED. In Full duplex mode, this pin acts as port 2 DUPLEX LED; in half duplex mode, it is collision LED for port 2. See Table 3 for mode detail.
Power On Setting PHYAS1	112	I,PD, LVTTL	Recommend PHY Address Bit 1. Value on this pin will be latched by DM8606BF during power on reset as the PHY address recommend value bit 1. See PHYAS0 description for more detail.
DUPCOL1		O 8mA	Port 1 Duplex-collision LED. In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for port 1. See Table 3 for mode detail.

Pad Name	Pad#	Type	Descriptions
Power On Setting RECANEN	113	I,PU, LVTTL	Recommend Auto Negotiation Enable. Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. 0 : Disable all TP port auto negotiation capability 1 : Enable all TP port auto negotiation capability
DUPCOL0		O, 8mA	Port 0 Duplex-collision LED. In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for port 1. See Table 3 for mode detail.
LNKACT[3:0]	95,96,97,98	O,PD, 8mA	LINK/Activity LED of port 3 to 0. When Link is stable, LNKACT will be low in 100M mode and high in 10M mode for the relevant port. When receiving data, LNKACT of the relevant port will be off for 100ms and on for 100ms.
LDSPD[3:0]	48,47,43,42	O,PD, 8mA	Port 3 to port 0 Speed LED. Used to indicate corresponding port's speed status, see Table 2 for more detail.

2.2.5 EEPROM Interface

Pad Name	Pad#	Type	Descriptions
EEDO	84	I,PU, LVTTL	EEPROM Data Output. This pin is used to input EEPROM data when reading EEPROM. During DM8606BF initialize itself, DM8606BF will drive EEPROM interface signal to read settings from EEPROM. Any other devices attach to EEPROM interface SHOULD drive Hi-Z or keep tri-state during this period. The initialization process needs about 500ms to complete.
IFSEL	80	I,PD, LVTTL	Interface selection. After DM8606BF initialization process is done, this pin is used to select using EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface 0 SDC/SDIO interface 1 EEPROM interface
EECS		O, 4mA	EEPROM Chip Select. During DM8606BF initialize itself, this pin is used as EEPROM chip select signal. During DM8606BF initialize itself, DM8606BF will drive EEPROM interface signal to read settings from EEPROM. Any other devices attach to EEPROM interface SHOULD drive Hi-Z or keep tri-state during this period. The initialization process needs about 500ms to complete.

Pad Name	Pad#	Type	Descriptions
Power On Setting XOVEN	81	I,PD, LVTTL,	Cross Over Enable. Value on this pin (active low) will be latched by DM8606BF at the rising edge of RESETL for port 4~0 crossover auto detect (Only available in TP interface) 1 : Enable 0 : Disable
EESK		I/O, 4mA	EEPROM Serial Clock. During DM8606BF initialize itself, this pin is used to output clock to EEPROM. After DM8606BF initialization process is done, this pin is used as EEPROM interface clock input if IFSEL = 1.
SDC		I,PD, LVTTL	Serial management interface clock input. If IFSEL = 0, this pin is used as serial management interface clock input.
Power On Setting LED_MODE	79	I,PD, LVTTL	Enable Mac to choose LED Display Mode. DM8606BF at the rising edge of RESETL as recommend operation described in EEPROM Reg0X11 with Bit[14].
EDI		I/O, 8mA	EEPROM Serial Data Input. During DM8606BF initialize itself, this pin is used to output address and command to access EEPROM. After the initialization process is done, this pin becomes an input pin to monitor EEPROM data if IFSEL = 1.
MDIO		I/O, 8mA	Serial management interface data input/output. If IFSEL = 0, this pin is used as data input/output pin of serial management interface

2.2.6 Power/Ground, 48 pins

Pad Name	Pad#	Type	Descriptions
GNDA	4,5,12, 13, 20, 27, 28, 34, 35	I	Ground Used by AD Block.
VCCA2	1, 9, 17, 24, 38	I	1.8V, Power Used by TX Line Driver.
VCCAD	8, 16, 23, 31	I	3.3V, Power Used by AD Block.
GNDBIAS	126	I	Ground Used by Bias Block
VCCBIAS	128	I	3.3V, Power Used by Bias Block.
GNDPLL	123	I	Ground used by PLL
VCCPLL	122	I	1.8V, Power used by PLL
GNDIK	45, 64, 76, 83, 93, 118	I	Ground Used by Digital Core
VCCIK	46, 75, 82, 94, 116	I	1.8V, Power Used by Digital Core
GNDO	50, 70, 87, 99, 108	I	Ground Used by Digital Pad
VCC3O	49, 71, 88, 109	I	3.3V, Power Used by Digital Pad.

2.2.7 Miscellaneous

Pad Name	Pad#	Type	Descriptions
TEST	41	I,PD, LVTTL	Test Mode. Reserved and should keep 0 when normal operation.

Pad Name	Pad#	Type	Descriptions
CFG0	86	I,PU, LVTTL	Configuration 0. Reserved and should keep 0 when normal operation.
WAIT_INIT	69	I,PU, LVTTL	Wait Initialization. This pin will be used to pause all activities after power up until loading EEPROM successful and done or CPU initialization done. 0 : pause until loading EEPROM done. 1 : pause until loading EEPROM successful and done or CPU initialization done
INT_N	65	O,OD, 8mA	Interrupt. Active low interrupt signal to indicate the status change in the interrupt status register. Interrupt signal will keep active until host read the status of ISR register. 1 : Not interrupt 0 : Interrupt
MDIO	40	I/O, 8mA PU	Management Data. MDIO transfers management data in and out of the device synchronous to MDC.
MDC	44	I,PD, SCHE	Management Data Reference Clock. A non-continuous clock input for management usage. DM8606BF will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.
CKO25M	85	O, 8mA	25M Clock Output. Free Running 25M Clock output (Even during power on reset)
RC	119	I, SCHE	RC Input For Power On reset. Active low signal to reset DM8606BF. Minimum during is 200 ms.
XI	120	I, Analog	25M Crystal/Oscillator Input. 25M Crystal or Oscillator Input. Variation is limited to +/- 50ppm.
XO	121	O, Analog	25M Crystal Output. When connected to oscillator, this pin should left unconnected.
RTX	127	I Analog	Constant Voltage Reference. External 1.1kΩ1% resistor connection to ground.
VREF	125	I Analog	Analog Reference Voltage. Used by Internal Bias Circuit for voltage reference.
CONTROL	124	I/O, Analog	FET Control Signal. The pin is used to control FET for 3.3V to 1.8V regulator.

Chapter 3 Function Description

3.1 Switch Functional Description

The DM8606BF uses a "store & forward" switching approach for the following reasons:
Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffers, especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.
Store & forward switches improve overall network performance by acting as a "network cache".
Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port

3.1.1 Basic Operation

The DM8606BF receives incoming packets from one of its ports, uses the source address (SA) and FID to update the address table, and then forwards the packet to the output ports determined by the destination address (DA) and FID.
If the DA and FID are not found in the address table, the DM8606BF treats the packet as a broadcast packet and forwards the packet to the other ports within the same group.
The DM8606BF could automatically learn the port number of attached network devices together with the SA and FID of all the incoming packets. If the SA and FID are not found in the address table, the DM8606BF adds it to the table.

3.1.2 Buffers and Queues

The DM8606BF incorporates 6 transmit queues and receive buffer area for the 6 Ethernet ports. The receive buffers as well as the transmit queues are located within theDM8606BF along with the switch fabric. The buffers are divided into 192 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.
Input buffers and output queues are maintained through proprietary patent pending UNIQUE (Universal Queue management) scheme.

3.1.3 Full Duplex Flow Control

When full duplex port runs out of its receive buffers, a PAUSE command will be issued by DM8606BF to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. When flow control hardware pin (GFCEN) is set to high during power on reset and per port PAUSE is enabled, DM8606BF will output and accept 802.3x flow control packet.

3.1.4 Half Duplex Flow Control

Back-pressure is supported for half-duplex operation. When the DM8606BF cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision.

3.1.5 Back-Off Algorithm

The DM8606BF implements the truncated exponential back off algorithm compliant to the 802.3 standard. DM8606BF will restart the back off algorithm by choosing 0-9 collision count. After 16 consecutive retransmit trials, the DM8606BF resets the collision counter. Users could set Back Off (see 0x0010) to disable this function.

3.1.6 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value is 9.6us for 10Mbps ETHERNET and 960ns for 100Mbps fast Ethernet. For the receive end, DM8606BF is designed to be able

to tolerate IPG gap greater than 64 bits. For the transmit end, DM8606BF will always transmit packets with the minimum IPG gap equal to 96-bits time. If users want to shorten the transmission IPG gap, they can enable the Short IPG function (see 0x000bh). Then DM8606BF will instruct its output MAC to transmit packets with IPG equal to 88-bits and 96-bits in order.

3.1.7 Trunking Function

DM8606BF supports only one trunking port. If Port 3 and Port 4 Trunk (see 0x000bh) function is enabled, DM8606BF will see Port 3 and Port 4 as the same port to make the bandwidth equal to 200M. When any of these two ports link fail, the DM8606BF will automatically change the transmit path from the failed link. Output port based load balancing is implemented in DM8606BF, so users don't set anything.

3.1.8 Illegal Frames

The DM8606BF will discard all illegal packets. These packets are
1. Undersize packets. The packets received with a length of less than 64 bytes are discarded.
2. Oversize packets. The packets received with a length of more than "MAXPKTLEN" bytes are discarded. See 0x0011h to see how to decide the MAXPKTLEN value.
3. CRC packets. The packets received with a wrong FCS value are discarded.
4. Symbol error packets. The packets received with symbol error are discarded.
5. Source violation packets. The packets received with a source violation could be discarded in some cases. See Source Violation Description.
6. VLAN violation packets. The frames received with a VLAN violation could be discarded in some cases. See VLAN violation Description.

3.1.9 Broadcast Storm

DM8606BF allows users to limit the traffic of the broadcast address (DA = 48'hffffffffffff) to prevent them from blocking the switch bandwidth. If users also want to limit the multicast packets(DA[40] = 1'b1), they could set the Multicast Packet Counted into Storming Counter (see 0x0010) function. Two thresholds and storm enable bits (see 0x003bh and 0x003ch) are used to control the broadcast storm.
1. Time Scale. DM8606BF uses 50ms as a scale to meter the storm packets.

	Rising Threshold	Falling Threshold
All link ports are 100M	100M Threshold (See 0x003bh)	1/2 100M Threshold
All link ports are not all 100M	10M Threshold (See 0x003ch)	1/2 10M Threshold

2. Storm keeps on at least 1.6 seconds if any of the ports meets the rising threshold in the 4 consecutive 50ms intervals. In these 1.6 seconds, the ports meeting the rising threshold will start to discard the broadcast or multicast packets until the 50ms interval expires. Users could also disable Input Filter (see 0x000b) function to forward above packets to the un-congested port instead of discarding directly.
Note that if the packet received is a management packet, it will not be discarded even in the above case.
3. Storm finishes. After the 1.6-second storm period, DM8606BF will check the port that makes the storm on. If all of these ports meet the falling threshold in the 2 consecutive 50ms intervals and no other ports satisfy the rising threshold at the same time, the storm will finish.

3.1.10 Bandwidth Control

DM8606BF supports hardware-based bandwidth control for both ingress and egress traffic. Ingress and egress rate could be limited independently on a per port base. The DM8606BF uses 8ms as the scale, and the minimum bandwidth control unit is 64kbps so users could configure the rate equal to K * 64kbps, 1<=K<=2048. DM8606BF maintains two counters (input and output) for each port. For example, if users want to limit rate equal to 64Kbps, they should configure the bandwidth control threshold equal to 1. At each time unit, DM8606BF will add 64 to the counter and decrease the byte length when receiving a packet in this period. When the counter is decreased to zero, we can divide the control behavior into two parts: For the ingress control, the ingress port will not receive packets any more. If flow control is enabled, Pause packets will be transmitted, if Back Pressure is enabled, Jam packet will be transmitted, and if the above functions are not enabled, the packet will be discarded.

For the egress control, the egress port will not transmit any packets, so the egress bandwidth is controlled. DM8606BF allows users to control the ingress and egress bandwidth at the same time (see 0x0033h).

3.1.11 Smart Discard

The DM8606BF supports a smart mechanism to discard packets early according to their priority to prevent the resource blocked by the low priority. The discard ratio is as follows:

Discard Mode / Utilization	00	01	10	11
00	0%	0%	0%	0%
01	0%	0%	25%	50%
11	0%	25%	50%	75%

3.1.12 LED Display

Three LEDs per port are provided by DM8606BF: Link/Act, Duplex/Col and Speed. The dual-color LED mode is also supported by DM8606BF. For easy production purpose, the test signal is sent to each LED at power on reset stage. The LED display mode is controlled by:
1. DUAL-COLOE-EE: It is an EEPROM register to control the dual or single color mode. See 0x0012h. It is useless when the value (wait_init) on the pin WAIT_INIT is low.
2. DUAL-COLOR-HW: It is the value latched on the EDI pin during the power on reset. It's also used to control the dual or single color mode and is useless when the value wait_init is high.
3. LED Enable (see 0x0012h): When CPU is attached and this CPU has no ability to pull the EDI to high or low, users could set the wait_init to high to delay the led test, write the correct value to the DUAL-COLOR_EE, write 1'b1 into LED Enable register, and then the LED test starts.
4. Duplex and Col Separate (see 0x0012h): Dupcol LEDs indicate the duplex status only.
5. COL_LED (See 0x0030h): When enabled, pin DUPCOL0 shows col_10m status and pin DUPCOL1 shows col_100m status. These two LEDs are necessary in the dual-speed hub.

3.1.12.1 Single Color LED Display

Pin Name	Status
LNKACT4/LNKACT3/ LNKACDM8606BF/L NKACT1/ LNKACT0	These pins have no power on reset values on them, and DM8606BF uses active low value to drive the led. So the output values of these pins after the power on reset are shown as follows: 1. First Period: This period lasts 1.28s for LED on test. DM8606BF drives value 0 to open the LED. 2. Second Period: This period lasts 0.48s for LED off test. DM8606BF drives value 1 to close the LED. 3. Normal Period: This period indicates the link status. 0 = Port links up and LED is ON. 1 = Port links down and LED is OFF. 0/1= Port links up and is transmitting or receiving. The LED flashes at 10hz.
LDSPD4/LDSPD3/ LDSPD2/LDSPD1/ LDSPD0	The behavior of these pins is the same as the LNKACT, except the normal period. Normal Period: This period indicates the speed status. 0 = Port links up and its speed is 100M. LED is ON. 1 = Port links down or its speed is 10M. LED is OFF.
DUPCOL2/DUPCOL1/ DUPCOL0	These 3 pins have power on reset values on them. DM8606BF needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows: 1. First Period: This period lasts 1.28s for LED on test. DM8606BF drives ~value_power_on to open the LED. 2. Second Period: This period lasts 0.48s for LED off test. DM8606BF drives value_power_on to close the LED. 3. Normal Period: This period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED is OFF.

Pin Name	Status
	0/1 = Port links up and collision is detected. LED flashes at 10hz. If Duplex and Col Separate is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1 = This value is cancelled. LED doesn't blink. If COL_LED is enabled, the display in the normal period is as follows: DUPCOL0: 10m collision indicator. 0/1 = One of the ports links up in 10M half-duplex mode and detects a collision event. LED flashes at 20hz. value_power_on = When the above event is not satisfied, the LED is OFF. DUPCOL1: 100m collision indicator. 0/1 = One of the ports links up in 100M half-duplex mode and detects a collision event. LED flashes at 20hz. Value_power_on = The above event is not satisfied. LED is OFF.
DUPCOL4/DUPCOL3	The behavior of these pins is the same as the LNKACT, except the normal period. Normal Period: This period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED is OFF. 0/1 = Port links up and collision is detected. LED flashes at 10hz. If Duplex and Col Separate is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1 = This value is cancelled. LED doesn't blink.

3.1.12.2 Dual Color LED Display

Users should be careful that DUPCOL LED only supports the single color mode. The only difference between single and dual color for DUPCOL LED is the self-test time.

Pin Name	Status
(LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3) (LNKACDM8606BF, LDSPD2) (LNKACT1, LDSPD1) (LNKACT0, LDSPD0)	First Period: Test LED on with green color. It lasts 1.28s. 0, 1 = LED is on with green color. Second Period: Test LED on with yellow color. It lasts 1.28s. 1, 0 = LED is on with yellow color. Third Period: Test LED off. 0, 0 = LED is off. Normal Period: This period shows the status of the link and speed at the same time. 0, 0 = Port links down. LED is off. 1, 1 = Port links down. LED is off. 0, 1 = Port Links up in 100M. LED glows green. 1, 0 = Port Links up in 10M. LED glows yellow. 0/1, 1 = Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10hz. 0/1, 0 = Port links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10hz.
DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1 DUPCOL0	The behavior of these pins is the same as the single mode, except the self-test period. The LED on test period is 2.56s instead of 1.28s.

3.1.12.3 Circuit for Single LED Mode

Figure 3-1 Circuit for single color LED mode

3.1.12.4 Circuit for Dual Led Mode

Figure 3-2 Circuit for dual color LED mode

3.1.13 Packet Identification

Packets are classified to determine if they should be passed to the CPU port or another entity for special handling.

Packets Identified by DM8606BF		Comments
BPDU		The Ethernet destination address is 01-80-C2-00-00-00.
PAUSE		The Ethernet destination address is 01-80-C2-00-00-01. Ether-Type field is 8808. OPCODE is 0001.
SLOW		The Ethernet destination address is 01-80-C2-00-00-02.
PAE		The Ethernet destination address is 01-80-C2-00-00-03.
RESER_R0		The Ethernet destination address ranges between 01-80-C2-00-00-04 and 01-80-C2-00-00-0F.
RESER_R1		The Ethernet destination address ranges between 01-80-C2-00-00-10 and 01-80-C2-00-00-1F.
GXRP		The Ethernet destination address ranges between 01-80-C2-00-00-20 and 01-80-C2-00-00-22.
RESER_R2		The Ethernet destination address ranges between 01-80-C2-00-00-23 and 01-80-C2-00-00-2F.
RESER_R3		The Ethernet destination address ranges between 01-80-C2-00-00-30 and 01-80-C2-00-00-FF
RARP		The Ethernet destination address is FF-FF-FF-FF-FF-FF and the Ether-Type field is 0x8035h.
ARP		The Ethernet destination address is FF-FF-FF-FF-FF-FF and the Ether-Type field is 0x0806h.
IGMP_IP		The Ethernet destination address is 01-00-5E-XX-XX-XX. Ether-Type field is 0x0800h (IP). IP Version is 4 and the Protocol field is 02 (IGMP).
MLD_IP		Ethernet destination address is 33-33-XX-XX-XX-XX. The Ether-Type field is 0x0800h (IP). IP Version is 6 and the Protocol field is 0x3ah (ICMP).
MLD_IPV6		Ethernet destination address is 33-33-XX-XX-XX-XX. The Ether-Type field is 0x86ddh (IP). IP Version is 6 and the Protocol field is 0x3ah (ICMP).
Others	TYPE	The Ether-Type field matches one of the type filters.
	PROTOCOL	The Protocol field matches one of the protocol filters.

	TCPUDP	The TCP/UDP port number matches one of the TCP/UDP filters.
	MAC_CTRL	The Ether-Type field is 0x8808h, but OPCODE is not 0x0001h.

For learning purpose, DM8606BF sometimes divide Ethernet address into three groups.

Packets Identified by DM8606BF	Comments
MULTICAST	The first bit of the Ethernet destination address is 1, but not all 1.
BROADCAST	The Ethernet destination address is FF-FF-FF-FF-FF-FF.
UNICAST	The first bit of the Ethernet destination address is 0.

3.1.13.1 Span Packet

The span packet is defined in DM8606BF to support spanning tree protocol.

Packet Type	Description
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit defined in the learning table when there is a match for DA+FID. 3. Span bit defined in the control table when there is a match for DA. 4. Span bit in register 0x003eh.
ARP/RARP	The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit in register 0x000dh.
IGMP_IP/MLD_IP/ MLD_IPV6	The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit in register 0x000ch.
Others	The span packet is determined in priority order by: 1. Span bit defined in the Special TAG, when Span_Valid is set. 2. Span bit defined in the learning table when there is a match for DA+FID. If the first and second conditions are not satisfied, the frame is classified as non-span packets.

3.1.13.2 Management Packet

DM8606BF reserves some buffers for these packets, so they are not dropped because of traffic congestion. Management packets are never limited by the bandwidth control, stormed by the storming control, or dropped due to smart discard function.

Packet Type	Description
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	The management packet is determined in priority order by: 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit defined in the learning table when there is a match for DA+FID. 3. Management bit defined in the control table when there is a match for DA. 4. Management bit in register 0x003eh.
ARP/RARP	The management packet is determined in priority order by: 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit in register 0x000dh.
IGMP_IP/MLD_IP/ MLD_IPV6	The management packet is determined in priority order by: 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit in register 0x000ch.
Others	The management packet is determined in priority order by: 1. Management bit defined in the Special TAG, when Management_Valid is set. 2. Management bit defined in the learning table when there is a match for DA+FID. If the first and second conditions are not satisfied, the frame is classified as non-management packets.

3.1.13.3 Cross_VLAN Packet

Cross-VLAN packets are defined to cross VLAN boundary or bypass the VLAN violation.

Packet Type	Description
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	The cross-VLAN packet is determined in priority order by: 1. Cross_VALN bit defined in the Special TAG, when Cross_VLAN_Valid is set. . 2. Cross_VLAN bit defined in the learning table when there is a match for DA+FID. 3. Cross_VLAN bit defined in the control table when there is a match for DA. 4. Cross_VLAN bit in register 0x003eh.
ARP/RARP	The cross_VLAN packet is determined in priority order by: 1. Cross_VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross-VLAN bit in register 0x000dh.
IGMP_IP/MLD_IP/ MLD_IPV6	The cross_VLAN packet is determined in priority order by: 1. Cross-VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross-VLAN bit in register 0x000ch.
Others	The Cross_VLAN packet is determined in priority order by: 1. Cross_VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set.. 2. Cross_VLAN bit defined in the learning table when there is a match for DA+FID. If the first and second conditions are not satisfied, the frame is classified as non-cross_VLAN packets.

3.1.14 Tagged VLAN or Port VLAN

The difference between two VLAN rules is the way to search the VLAN boundary. Users could enable "TAG Base VLAN" (see 0x0011h) bit to instruct DM8606BF to operate in the Tagged VLAN mode.

3.1.14.1 VLAN Filters

DM8606BF supports 16 VLAN filters, each specifying a Valid bit, a TAG PRI, a VID, a FID, a Tagged Member, and a Member.

	VLAN_Valid	VLAN_PRI[2:0]	VID[11:0]	FID[3:0]	Tagged Member[5:0]	Member[5:0]
VLAN Filter 0						
~						
VLAN Filter 15						

3.1.14.2 Port VLAN

Port VLANs are created by grouping individual physical ports together. In this mode, only 6 VLAN filters (VLAN filter 0 ~5) are used. By the time examining the received frame, the source port is used as an index to search the VLAN filter. If the source port is port 0, then Member in the filter 0 is the VLAN group that port 0 joins.

3.1.14.3 Tagged VLAN

Tagged VLAN is created with the aids of the VID in the packet or VID assigned by the source port. This VID is compared with 16 VIDs in the VLAN filters to check if any match exists. The Member in this matched filter is the VLAN boundary for the packet.

3.1.14.4 VID for Comparison and Carried through DM8606BF

VID for comparison and carried through DM8606BF (as egress VID) depends on the VLAN configuration.
VID0 The incoming packet is tagged with VID = 12'h0. Enable "Replace VID0" (see 0x000ah) to replace the Null VID with PVID (see basic control registers) if necessary.
VID1 The incoming packet is tagged with VID = 12'h1. Enable "Replace VID1" (see 0x000ah) to replace VID1 with PVID (see basic control registers) if necessary.
VIDFFF The incoming packet is tagged with VID = 12'hfff. Enable "Replace VIDFFF" (see 0x000ah) to replace VIDFFF with PVID (see basic control registers) if necessary.
VLAN Security DM8606BF ignores packet's VID and always uses PVID to see if there is a match and transfers it to the output ports. Disable the "VLAN Security Disable" (See0x0022h) to achieve this goal.
Input Force No Tag When enabled (see 0x0020h), DM8606BF assumes all the packets are untagged and PVID is used. Input Force No Tag and VLAN Security are different in some situations.

	Tagged Frame with VID = 12'hfff	Packet Transmitted Tagged

VLAN Security	The frame is recorded as a VLAN violation and discarded if VIDFFF is not replaced.	Output packets have only one VLAN tag.
Input Force No Tag	The frame is recognized as an untagged frame. PVID is carried with this packet to the output port.	Output packets may have double tags, because the packet is transmitted with an additional tag with PVID.

3.1.14.5 Admit Only VLAN-Tagged Packets

DM8606BF supports a function to check if the packet is VLAN-Tagged, and any packets received on that port that carries no VID (untagged packets or packets with VID = 0) are discarded and recorded as a VLAN violation. This feature is implemented by programming the "Admit Only VLAN-Tagged" (see 0x0027). DM8606BF assumes all the packets are untagged in the "Input Force No Tag" mode and users should care that in this situation, "Admit Only VLAN Tagged" is of no effect.

3.1.14.6 VID Check

In Tagged VLAN, the VID for comparison must be contained in the VLAN filters, or the packet received on the port will be dropped and recorded as a VLAN violation. This feature is disabled by programming the "VID CHECK" bit to 0 (see 0x0026h) to forward these packets instead of dropping them.

3.1.14.7 FID and VLAN Boundary

In DM8606BF, every incoming packet is associated with a FID group. DM8606BF searches the learning table for the FID + DA, FID + SA. VLAN boundary restricts the allowable destination ports.

FID Search Algorithm			
Port VLAN	The source port number is the VLAN filter index. We can find FID in this filter.		
Tagged VLAN	VID match	Fid is contained in the matched filter. We can find FID in this filter.	
	VID un-match	VID check	The frame is dropped.
		VID uncheck	Default FID is the FID (see 0x000ah). If users configure DM8606BF to back to port VLAN (see 0x0027), we can find the FID in the same way as the Port VLAN. When this feature is enabled, VLAN filter 0 ~ 5 are for Port VLAN purpose and VLAN filter 6 ~15 are for VID comparison.

VLAN Boundary Search Algorithm			
Port VLAN	The source port number is the VLAN filter index. We can find the boundary in this filter.		
Tagged VLAN	VID match	Member is contained in the matched filter. We can find the boundary in this filter	
	VID un-match	VID check	The frame is dropped.
		VID uncheck	DM8606BF uses Default VLAN Portmap as the boundary (see 0x003ah). If users configure DM8606BF to "Back to Port VLAN" (see 0x0027), we can back to find the boundary in the same way as the Port VLAN. When this feature is enabled, VLAN filter 0 ~ 5 are for Port VLAN purpose and VLAN filter 6 ~15 are for VID comparison.

3.1.14.8 Ingress Filter

If the source port is not contained in the VLAN boundary associated with the incoming packet, then this frame is dropped and recorded as a VLAN violation. This feature is disabled by setting the "Ingress Filter" (see 0x0021h) bit to 1'b0.

3.1.14.9 VLAN Violation

When packets are recoded as a VLAN violation packet, DM8606BF will drop them. The only way to ignore these violations is to classify these packets as cross_VLAN packets.

3.1.14.10 TXTAG Carried through DM8606BF

Each packet during receive is assigned 2-bit TXTAG value. This value is carried by DM8606BF to the output ports to help to determine if egress tagged is necessary.

Packet Type	Description

BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTXG in the learning table when there is a match for DA+FID in the learning table. 3. TXTXG in the control table when there is a match for DA in the control table. 4. TXTAG defined in register 0x003eh.
ARP/RARP	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG is defined in 0x000dh.
IGMP_IP/MLD_IP/ MLD_IPV6	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG is defined in 0x000ch.
Other	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. The DA + FID matches an entry in the learning table with TXTXG defined. If the first and second conditions are not satisfied, TXTAG is 2'b00.

3.1.14.11 Tagged Member Carried through DM8606BF

If the output port is a tagged port is determined by the port or the VID. Ports in the tagged members should egress packets tagged.

First way: New Transmit Tag Disable (see 0x000ah)			
The "Output Packet Tagging" bit in the basic control registers determines the tagged members.			
Second way: New Transmit Tag Enable (see 0x000ah)			
Port VLAN	The source port number is the VLAN filter index. We can find the tagged member in this filter.		
Tagged VLAN	VID match	Tagged members are contained in the matched VLAN filter. We can find the tagged members in this filter	
	VID un-match	VID check	The frame is dropped.
		VID uncheck	DM8606BF uses the first way to determine the tagged members. If users configure DM8606BF to "Back to Port VLAN" (see 0x0027), we can back to find the tagged members in the same way as the Port VLAN.

Users should note that when the Special Tag with Tagged Member Valid = 1'b1 is incoming, the DM8606BF always uses Tagged Member in the Special Tag as the Tagged Member.

3.1.14.12 Egress Tag Rule

The tagged member is transferred from the source to the destination port where the decision whether the transmitted frame is tagged is made.

Egress Tag Result		
Untagged packets are received (If Input Force No Tag is enabled, DM8606BF assumes all the received packets are untagged.)	Output port is in the tagged members carried with the packet.	TXTAG Description 00 = System Default Tag. Packets are transmitted tagged. 01 = Unmodified. Packets are transmitted untagged. 10 = Always Tagged. Packets are transmitted tagged. 11 = Always Untagged. Packets are transmitted untagged.

	Output port is not in the tagged members carried with the packet.	TXTAG Description 00 = System Default Tag. Packets are transmitted untagged. 01 = Unmodified. Packets are transmitted untagged. 10 = Always Tagged. Packets are transmitted tagged. 11 = Always Untagged. Packets are transmitted untagged.
	Output port is configured to operate in the bypass mode. See 0x002ah.	TXTAG Description 00 = System Default Tag. Packets are transmitted untagged. 01 = Unmodified. Packets are transmitted untagged. 10 = Always Tagged. Packets are transmitted tagged. 11 = Always Untagged. Packets are transmitted untagged.
Tagged packets are received.	Output port is in the tagged members carried with the packet.	TXTAG Description 00 = System Default Tag. Packets are transmitted tagged. 01 = Unmodified. Packets are transmitted tagged. 10 = Always Tagged. Packets are transmitted tagged. 11 = Always Untagged. Packets are transmitted untagged.
	Output port is not in the tagged members carried with the packet.	TXTAG Description 00 = System Default Tag. Packets are transmitted untagged. 01 = Unmodified. Packets are transmitted tagged. 10 = Always Tagged. Packets are transmitted tagged. 11 = Always Untagged. Packets are transmitted untagged.
	Output port is configured to operate in the bypass mode. See 0x002ah.	TXTAG Description 00 = System Default Tag. Packets are transmitted tagged. 01 = Unmodified. Packets are transmitted tagged. 10 = Always Tagged. Packets are transmitted tagged. 11 = Always Untagged. Packets are transmitted untagged.

3.1.14.13: Tagged PRI Carried through DM8606BF

Tagged PRI Carried		
Untagged packets are received (If Input Force No Tag is enabled, DM8606BF assumes all the received packets are untagged.)	Port VLAN	Change Priority Enable (see 0x000a) Change Rule 0 = VLAN_PRI field in the matched VLAN filter. 1 = Reverse PRI Change Priority Disable Reverse PRI

	Tagged VLAN	VID unmatch	Reverse PRI
		VID match	Change Priority Enable (see 0x000a) Change Rule 0 = VLAN_PRI field in the matched VLAN filter. 1 = Reverse PRI Change Priority Disable Reverse PRI
Tagged packets are received.	Port VLAN	Change Priority Enable (see 0x000a) Change Rule 0 = VLAN_PRI field in the matched VLAN filter. 1 = Reverse PRI Change Priority Disable Tagged PRI = The 3-bit user priority in the tag header.	
	Tagged VLAN	VID un-match	Change Priority Enable (see 0x000a) Reverse PRI Change Priority Disable Tagged PRI = The 3-bit user priority in the tag header.
		VID match	Change Priority Enable (see 0x000a) Change Rule 0 = VLAN_PRI field in the matched VLAN filter. 1 = Reverse PRI Change Priority Disable Tagged PRI = The 3-bit user priority in the tag header.
Reserve PRI is reversed from the priority queue the packet is switched through. Compare = {queue, queue, queue, queue, queue, queue, queue, queue} XOR VLAN Priority MAP in 0x000eh. Then we get Tagged PRI. Compare Tagged PRI xxxx_xxx0 = 3'b000 xxxx_xx01 = 3'b001 xxxx_x011 = 3'b010 xxxx_0111 = 3'b011 xxx0_1111 = 3'b100 xx01_1111 = 3'b101 x011_1111 = 3'b110 0111_1111 = 3'b111 1111_1111 = 3'b000			

3.1.14.14: CFI Carried through DM8606BF

CFI Carried	
Untagged frames received (If Input Force No Tag is enabled, DM8606BF assumes all the received packets are untagged.)	CFI Carried = 1'b0
Tagged frame received	CFI Carried = Original CFI in the tag header.

3.1.14.15 Egress TAG

Egress tag contains Egress PRI, Egress CFI, and Egress VID. When packets are transmitted tagged, this egress tag associated with Ethernet-Type = 0x8100h is inserted following the Ethernet source address.
Egress PRI: Egress PRI is Tagged PRI carried through DM8606BF from the source port.
Egress CFI: Egress CFI is CFI carried through DM8606BF from the source port.
Egress VID: Egress VID is VID carried through DM8606BF from the source port.

3.1.15 Priority Queue

DM8606BF supports 4 priority queues and each is assigned a weight.

Queue	Weight
Queue 0	Weight = 1.
Queue 1	Weight = "Queue 1 Weight" bits in 0x0025h.
Queue 2	Weight = "Queue 2 Weight" bits in 0x0026h.
Queue 3	Weight = "Queue 3 Weight" bits in 0x0027h.

3.1.15.1 System PRI

The system PRI is determined in the order as follows:
1. (DA+FID) was found in the learning table, then LRN_PRI field (when LRN_PRIEN is set) in this entry indicates the priority queue.
2. Port PRI in basic control register indicates the priority queue, when Port_PRIEN is enabled on that port.
3. The user priority field in the tag header is used for a tagged packet ("Input Force No Tag" doesn't effect DM8606BF to extract the PRI in the tag header), when "VLAN Priority" is enabled. The user priority in the tag header is a 3-bits field, DM8606BF uses "VLAN Priority MAP" to map the priority queue.
4. For IP packets with no tag header, IP PRI is used when "Service Priority" (see 0x001fh) is enabled. Even for a tagged packet with IP header, we can set "IP over VLAN" (see basic control registers) bit to 1 to force using IP PRI. Three kinds of IP PRI are available.
(1) For IPV6 packets with IP Version = 4'h6, the most significant 6-bits of the traffic class in the IPV6 header is used to map the priority queue by the service mapping registers.
(2) For IPV4 packets with IP Version = 4'h4, the most significant 3-bits of the TOS field in the IPV4 header is used to map the priority queue by the TOS Priority Map register.
(3) If "TOS Using" (see 0x000ah) is disabled, even for IPV4 packets, DM8606BF uses the most significant 6-bits of the TOS field to map the priority queue by the service mapping registers.
5. If the packet matches the TCP/UDP filters, the PRI associated with this filter indicates the priority queue when "TCP/UDP PRIEN" is set to 1 (see 0x0098h). Users could enable "TCPUDP over IP" to force using the TCPUDP PRI when there is a match.

3.1.15.2 Queue Assigned

Packets Identified by DM8606BF	The Order of Priority Assigned
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. If (DA+FID) matches an entry in the learning table, then LRN_PRI field with LRN_PRIEN enabled in this entry indicates the priority queue. 3. Use PRI in 0x003dh to indicate the queue the frame was switched.
ARP/RARP	1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. Use PRI in 0x000dh to indicate the priority queue when enabled. 3. Use System PRI.
IGMP_IP/MLD_IP/ MLD_IPV6	1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. Use PRI in 0x000ch to indicate the priority queue when enabled. 3. Use System PRI.
Others	1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue. 2. Use System PRI.

3.1.16 Address Learning

DM8606BF provides two ways to create the entry in the address table: dynamic learning and manual learning. A four-way hash algorithm is implemented to allow the maximum of 4 different addresses with the same hash key to be stored at the same time. Up to 2k entries can be created and all entries are stored in the internal SSRAM. DM8606BF searches the learning table for the SA+FID of the incoming packet or the instruction from CPU. When both fields (a single SA may exist in different FID) are matched, there is a match.

3.1.16.1 Dynamic Learning

The DM8606BF searches for SA and FID of an incoming packet in the address table and takes dynamic learning action as follows:
1. If (SA+FID) was not found in the learning table, create a new entry with SA, FID, and the incoming port.
2. If (SA+FID) was found in the learning table, and the incoming port and the Portmap don't match, create a new entry with SA, FID, and the incoming port.

Dynamic learning will be disabled in the following condition:
1. Security violation exists on the port.
2. VLAN violation exists on the port.
3. The packet is a PAUSE packet.
4. The number of the addresses that port has learned has reached its maximum.
5. The port disables its learning function (see extended control registers).
6. The packet is an illegal packet (too long, too short or FCS error).
7. A packet with Special Tag is received and the LRN bit is 0 and LRN_Valid = 1'b1.
8. The port is in the Disabled state in the Spanning Tree Protocol.
10. The port is in the Blocking/Listening state in the Spanning Tree Protocol.
11. All the four entries in the same hash address are occupied and all of them are static addresses.

3.1.16.2 Manual Learning

The DM8606BF implements the manual learning through the CPU's help. The CPU can create or remove any entry in the address table. Each entry could be static or not. "Static" means the entry will not be aged forever. When the entry is static, then the definition in some fields is modified to make DM8606BF work more flexibly.

3.1.16.3 Learning Table

3.1.16.3.1 Entry Format in the Learning Table

69	68	67	66 58	57 52	51 48	47 0
Bad	Info_Type	Occupy	Info_Ctrl/Age Timer	Portmap	FID	Address

Field	Description	
Bad	The entry is marked to show if it is failed during the learning table memory bist time. 0 = Doesn't fail. 1 = Fail.	
Info_Type	Static Address. 0 = The entry is not static. 1 = The entry is static.	
Occupy	The entry is marked to show the status if the entry is occupied. 0 = Don't occupy. 1 = Occupy.	
Info_Ctrl/ Age Timer	Info_Ctrl is used when the entry is static.	
	Bit	Description
	8	Source Intrusion. 0 = It isn't a violated source address. 1 = It is a violated source address.
	7	Span. 0 = Not span packet. 1 = A span packet.
	6	Management. 0 = Not a management packet. 1 = A management packet.
	5	Cross_VLAN. 0 = Not a cross_VLAN packet. 1 = A cross_VLAN packet.
	4:3	TXTXG. It is used as an option for inserting Tag on the transmission port. 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged. 11 = Always Untagged.
	2	LRN_PRIEN. 0 = LRN_PRI is not used. 1 = LRN_PRI is used.

	1:0	LRN_PRI. It identified the address priority. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.
	Age Timer is used when the entry is not static.	
	Bit	Description
	8:0	Age Timer. This timer is used to control the ageing time.
Portmap	The field is used as the output ports associated with the FID+MAC Address.	
FID	The field is used as the FID group associated with the MAC address.	
Address	The MAC Address in the learning table.	

3.1.16.3.2 The Registers Accessing the Learning Table

12 registers are provided by DM8606BF to support the customer to access the address table. These 12 registers are Address Table Control Register 0 ~ 5 and Address Table Status Register 0 ~ 5 in 0x011ah ~ 0x0125h.

Control Register Description						
Command	Access Control	Info_Type	Info_Ctrl/ Age Timer	Portmap	FID	Address
Control 5 [6:4]	Control 5 [3:0]	Control 4[12]	Control 4 [8:0]	Control 3 [9:4]	Control 3 [3:0]	{Control 2, Control 1, Control 0}

The Address, FID, Portmap, Info_Ctrl/Age Timer and Info_Type in the Control Register have the same meaning as those in the entry format. The Command and Access Control is described as follows:

Description for Command and Access Control.		
Command	Access Control	Description
3'b000	4'b0111	Create a new address
3'b000	4'b1111	Overwrite an existed address
3'b001	4'b1111	Erase an existed address

Status Register Description								
Busy	Result	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Status 5 [31]	Status 5 [30:28]	Status 5 [2]	Status 5[1]	Status 5[0]	Status 4 [8:0]	Status 3 [9:4]	Status 3 [3:0]	{Status 2, Status 1, Status 0}

Description for the Status Register	
Result	This field tells us the status for not only the search operation but also the creating operation. 000 = Command OK 001 = All Entry Used. This result happens only for the create operation. DM8606BF uses the 4-way address lookup engine so it allows 4 different addresses stored at each hash location. If these 4 entries are all static, then CPU will not successfully create 5th different address hashed to the same location and 001 will be returned. The only way to create 5th different address is to remove one of early addresses. 101 = Command Error.
Busy	This bit indicates if the table engine for access is available. 1 = The engine is busy and it will not accept the command from the CPU. 0 = The engine is available.

3.1.16.3.3 Rules to Access the Learning Table

(1) Check the Busy Bit in the status register to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.

(2) Write the MAC address[15:0] into the control register 0.
(3) Write the MAC address[31:16] into the control register 1.
(4) Write the MAC address[47:32] into the control register 2.
(5) Write the Portmap and FID into the control register 3.
(6) Write the Info_Ctrl/Age Timer and Info_Type into the control register 4.
(7) Write the Access Control and Command into the control register 5 to define the operation.
(8) Wait for the engine to complete (Check the Busy Bit).
(9) Read the desired result returned in the status register.

3.1.16.3.4 Example

Example	Rule
The user needs DM8606BF to forward the specified unicast packet (DA = 48'h0012-3456-789A and FID = 2) to port 3 forever.	(1) Check the Busy bit. If Busy = 1'b0, go to the next step. If Busy = 1'b1, wait. (2) Write 16'h789A into control register 0. (3) Write 16'h3456 into control register 1 (4) Write 16'h0012 into control register 2. (5) Write 16'h0082 into control register 3. (6) Write 16'h1000 into control register 4. (7) Write 16'h0007 into control register 5. (8) Read the status register 5 to check the busy bit. If Busy = 1'b0, check the Command Result to see if the create operation is successful. If Busy = 1'b1, wait
The user needs DM8606BF to forward the specified multicast packet (DA = 48'h0123-4567-89AB and FID = 3) to port 0, and port 1 both. This address could be aged.	(1) Check the Busy bit. If Busy = 1'b0, go to the next step. If Busy = 1'b1, wait. (2) Write 16'h89AB into control register 0. (3) Write 16'h4567 into control register 1 (4) Write 16'h0123 into control register 2. (5) Write 16'h0033 into control register 3. (6) Write 16'h0000 into control register 4. (7) Write 16'h0007 into control register 5. (8) Read the status register 5 to check the busy bit. If Busy = 1'b0, check the Command Result to see if the create operation is successful. If Busy = 1'b1, wait

3.1.17 Address Aging

DM8606BF maintains an age timer for each address. The aging timer is reset to 0 when the packet is received. When aging time counts up to 300 seconds, it means that this station didn't transmit packets for this period and the address can be removed from the table. This could help to prevent a station leaves the network and occupies a table space for a long time. Aging function can be disabled from the EEPROM (see extend control registers). If the address is static, DM8606BF doesn't age it out also. The default aging timer is 300 seconds. User could change Aging Timer Select (0x0011h) to shorten the aging time.

3.1.18 Hardware based IGMP Snooping

DM8606BF support IGMP v1/v2 Snooping without any software effort. DM8606BF will monitor the IGMP traffic and update its embedded IGMP membership table if hardware based IGMP snooping function enabled. IP multicast frames can be forwarded according to the Port-Map information of the membership table. The data of the membership can also be accessed by CPU via SDC/SDIO interface. The following registers could be used to configure the IGMP Snooping behavior.

1. EEPROM register 0x00b bit [13:12] , Additional Snooping Control register.
2. EEPROM register 0x00b bit [2], Source Violation Over Snooping.
3. EEPROM register 0x00b bit [1], Source Violation Over Default.
4. EEPROM register 0x00c bit [13:6], various Snooping Control registers.
5. EEPROM register 0x00c bit [2], Hardware IGMP Packet Ignore CPU Port.
6. EEPROM register 0x00c bit [1], Hardware IGMP Snooping Enable.
7. EEPROM register 0x00c bit [0], Hardware IGMP Default Router Enable.
8. EEPROM register 0x00d bit [14], IP Multicast Packet Treated as Cross VLAN packet.

9. EEPROM register 0x01b bit [14:9], Multicast Port-Map.
10. EEPROM register 0x03f bit [15:8], Query Interval.
11. EEPROM register 0x03f bit [7:6], Robust Variable.
12. EEPROM register 0x03f bit [5:0], Default Router Port-Map.

3.1.18.1 Entry Format of IGMP membership Table

57	56	55 48	47 42	41 30	29	28 23	22 0
Bad	Occupy	Response Timer	Response Flag	No Response Counter	Report Mask	Port-Map	Group ID

Field	Description
Bad	The entry is marked to show if it is failed during the learning table memory bist time. 0 = Doesn't fail. 1 = Fail.
Occupy	The entry is marked to show the status if the entry is occupied. 0 = Don't occupy. 1 = Occupy.
Response Timer	Response Timer The timer will be set according to maximum response time field in General Query frame or Group Specific Query frame and count down every 100ms.
Response Flag	A flag is used to record any IGMP REPORT frame is received for each port before Response Timer count to 0. 0 : No IGMP REPORT frame is received. 1. : IGMP REPORT frame is received
No Response Counter	A counter for each port is used to count the consecutive occurrence times of no IGMP REPORT frame received before Response Timer count to 0.
Report Mask	A flag is used to record any IGMP REPORT frame of this Group is received before Response Timer count to 0. 0 : No IGMP REPORT frame of this Group is received. 1 : IGMP REPORT frame is received.
Port-Map	A flag is used to denote weather the port is the member of this Group or not. 0 : The port is not the member of this Group. 1 : The port is the member of this Group.
Group ID	IP Multicast Group ID

3.1.18.2 The Registers Accessing the IGMP membership table

The registers for accessing the IGMP membership table are the same with accessing MAC address filtering table, but the data format are re-defined as below.

Control Register Description		
Command	Entry Address	Entry Data
Control5[6:4]	Control4[4:0]	{Control3[9:0], Control2, Control1, Control0}

The Command used to access IGMP membership table is defined as below.:

Description for Command	
Command	Description
3'b100	write data into internal IGMP table
3'b101	Read data from internal IGMP table

Status Register Description			
Busy	Result	Entry Address	Entry Data
Status5[15]	Status5[14:12]	Status4[4:0]	{Status3[9:0], Status2, Status1, Status0}

3.1.19 Source Violation

Source violation is defined in DM8606BF to support flexible security modes. See Security Option in the EEPROM Basic Register and the Src_Violation bit in the Learning Table.

Security Mode	Description
First Lock	DM8606BF locks the first SA+FID of packets received on the port. After the first (SA+FID) was locked, DM8606BF starts to check packets with different (SA+FID). 1. If the packets are not assigned as management, drop it (modify the forwarding algorithm) and record as a source violation. 2. If the packets are management packets, and Source Violation (see 0x000bh) is configured to 1'b1 for different kinds of packets, then DM8606BF modifies the forwarding algorithm to drop these packets. They are also recorded as a source violation. 3. If the packets are management packets and Source Violation is configured to 1'b0, then DM8606BF doesn't modify the forwarding algorithm. In this situation, we don't record this case as a source violation.
First Link Lock	The first received packets will be locked as First Lock. The difference is that the receiving port will not receive and learn packets any more after the port links down even if it links up again. A source violation is recorded as the First Lock. If DM8606BF modifies the forwarding algorithm is still as the First Lock.
Assign Lock	DM8606BF allows users to assign the locked SA+FID through CPU's help instead of the first SA+FID. A source violation is recorded as the First Lock. If DM8606BF modifies the forwarding algorithm is still as the First Lock.
Assign Link Lock	DM8606BF allows users to assign the locked SA+FID through CPU's help instead of the first SA+FID. The others are the same as First Link Lock.
Discard Unknown	The "unknown source address" means that (SA+FID) is not found in the learning table or even is found but Portmap doesn't match the incoming port. If "unknown" packets are received, DM8606BF records the source violation as the First Lock. The rule to modify the forwarding algorithm is still as the First Lock.
Unknown to CPU	This option is the same as "Discard Unknown" except that if DM8606BF decides to modify the forwarding algorithm, it will forward the packets to the CPU port instead of dropping them.
Source Intrusion	If the incoming port receives the packets with SA is marked as Source Intrusion, we handle these packets in the following rule: 1. Enable Source Intrusion Must (see 0x000bh) to instruct DM8606BF to modify the forwarding algorithm and record the source violation always. 2. If Source Intrusion Must is not enabled, DM8606BF also modifies the forwarding algorithm and records the source violation when any non-management packets are received. 3. If Source Intrusion Must is not enabled, DM8606BF also modifies the forwarding algorithm and records the source violation when amanagement packets are received but Source Violation is configured to 1'b1. 4. If Source Intrusion Must is not enabled, DM8606BF doesn't modify the forwarding algorithm and records the source violation when management packets are received and Source Violation is configured to 1'b0. DM8606BF allows the users to redirect the packets to the CPU port instead of dropping it when they violate the source intrusion (see Source Intrusion Action in 0x000bh).

DM8606BF supports stricter security protection. The port is disabled when there is a source violation. Enable Security Option[3] to enable this feature.

3.1.20 Packet Forwarding

DM8606BF identifies packet headers and transfers it from the incoming port to the destination ports.

3.1.20.1 Control Table

DM8606BF provides a control table for user to control the forwarding algorithm of the DA = 01-80-C2-00-00-00 ~ DA = 01-80-C2-00-00-2f easily. This control table is defined in 0x0074h ~0x008bh.

3.1.20.2 Default Output Ports

The default output ports that a packet is transferred to are determined in the following order.

1. The Portmap in the Special Tag with Portmap_Valid = 1 is used as the output ports.
2. The Portmap in the learning table is used as the output ports, when (DA+FID) matches an entry in the learning table.
3. The Portmap in the hardware IGMP table is used as the output ports, when DA matches an entry in the hardware IGMP table and "Hardware IGMP Snooping" (see 0x000bh) is enabled.
4. "Broadcast Portmap" (see 0x001ah) is used as the output ports, when the incoming packet is a broadcast packet.
5, "Multicast Portmap" (see 0x001bh) is used as the output ports, when the incoming packet is a multicast packet.
6. "Unicast Portmap" (see 0x0019h) is used as the output ports, when the incoming packet is a unicast packet.

3.1.20.3 Forwarding Algorithm

Packets Identified by DM8606BF	Algorithm
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Seacial Tag as the output ports. ELSE IF ((DA+FID) matches an entry in the learning table)), THEN use the Portmap in the learning table as the output ports. ELSE IF (DA matches an entry in the control table), THEN the output ports are the Portmap in the table. ELSE the output ports are the intersection of the Pass Portmap (see 0x003dh and 0x003eh) and the "Reserve Portmap" in the EEPROM (see 0x001c)
ARP/RARP	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF (ARP/RARP is trapped), THEN use ARP/RARP Portmap as the output ports. ELSE use "Default Output Ports" as the output ports.

IGMP_IP/MLD_IP/ MLD_IPV6	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports.
	ELSE IF (Hardware IGMP Snooping is enabled),
	IF (Hardware IGMP Packet Ignore CPU Port is enabled),
	THEN forwards packets to Multicast Portmap but doesn't forward to the CPU port.
	Else forwards packets to Multicast Portmap.
	ELSE IF (IGMP_IP/MLD_IP/MLD_IPV6 is trapped), THEN use IGMP/IGMP_IP/MLD_IP/MLD_IPV6 Portmap as the output ports.
	ELSE use "Default Output Ports" as the output ports.

TYPE	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use Type Portmap as the output ports.
PROTOCOL	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use Protocol Portmap as the output ports.
TCPUDP	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE use TCPUDP Portmap as the output ports.
MAC_CTRL	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the

	Special Tag as the output ports. ELSE use MAC CTRL Portmap as the output ports.
Others	Use "Default Output Ports" as the output ports

3.1.21 Special TAG

Special Tag is inserted after the Ethernet SA field to allow the CPU to tell the switch how to handle the packets it sends or to know the source port when the CPU receives a packet.

8 Bytes	Preamble
6 Bytes	DA
6 Bytes	SA
Byte 0	Special Tag 0
Byte 1	Special Tag 1
Byte 2	Special Tag 2
Byte 3	Special Tag 3
Byte 4	Special Tag 4
Byte 5	Special Tag 5
4 Bytes	VLAN Tag
6 Bytes	SNAP
2 Bytes	Type/Length
	Data
4 Bytes	CRC

3.1.21.1 Special Tag for the Receive

Users are allowed to enable Special TAG Receive (0x0011h) function to instruct DM8606BF to check the Special Tag to see if this field contains any commands when packets are received on the CPU port.

Special TAG	Description
Byte 0	DM Prefix 0.
Byte 1	DM Prefix 1. When Special TAG Receive is enabled, DM8606BF will compare {DM Prefix -, DM Prefix 1} with DM TAG Ether Type (see 0x002eh). If they are different, Special Tag is ignored. If they are the same, DM8606BF uses the Special Tag to make switching decisions.
Byte 2	Bit [7]: Don't care. Bit [6]: Portmap_Valid. 1 = Vaild. 0 = Not Valid. Bit [5:0]: Portmap in the Special Tag.
Byte 3	Bit [7]: Span_Valid. 1 = Valid. 0 = Not Valid. Bit [6]: Span. 1 = Span packet. 0 = Not span packet. Bit [5]: Management_Valid. 1 = Valid. 0 = Not Valid. Bit [4]: Management. 1 = Management packet. 0 = Not management packet. Bit [3]: Cross_VLAN_Valid. 1 = Valid. 0 = Not Valid. Bit [2]: Cross_VLAN. 1 = Cross_Vlan packet. 0 = Not Cross_VLAN packet. Bit [1]: LRN_Valid. 1 = Valid. 0 = Not Valid. Bit [0]: LRN. 1 = Learn. 0 = Not Learn,
Byte 4	Bit[7]: Ignore. Bit[6]: PRI_Valid. 1= Valid. 0 = Not Valid. Bit[5:4]: PRI. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3. Bit [3]: Ignore. Bit [2]: TXTAG_Valid. 1 = Valid. 0 = Not Valid. Bit [1:0]: TXTAG.
Byte 5	Bit [6]: Tagged Member Valid. 1 = Valid. 0 = Not Valid. Bit [5:0]: Tagged Member. Bit[X] = 1: Port is in the tagged member.

3.1.21.2 Special Tag for the Transmit

Users are allowed to enable Special TAG Transmit (0x0011h) function to instruct DM8606BF to insert the Special Tag followed SA in the packets transmitted from the CPU port. DM8606BF also allows users to choose what kinds of packets they don't want to insert this Special Tag even when Special TAG Transmit (0x0011h) function is enabled.

Packets Identified by DM8606BF	Condition	Result
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXRP/ RESER_R2/ RESER_R3	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert Reserve} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Reserve} = 2'b11.	Insert Special Tag on the CPU port.
ARP/RARP	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert ARP/RARP} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert ARP/RARP} = 2'b11.	Insert Special Tag on the CPU port.
IGMP_IP/MLD_IP/ MLD_IPV6	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert Snoop} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Snoop} = 2'b11.	Insert Special Tag on the CPU port.
TYPE	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert Type} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Type} = 2'b11.	Insert Special Tag on the CPU port.
PROTOCOL	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert Protocol} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Protocol} = 2'b11.	Insert Special Tag on the CPU port.
TCPUDP	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert TCP/UDP} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert TCP/UDP} = 2'b11.	Insert Special Tag on the CPU port.
MAC_CTRL	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert MAC CTRL} = 2'b10.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert MAC CTRL} = 2'b11.	Insert Special Tag on the CPU port.
Others	Special TAG Transmit = 1'b0. or {Special TAG Transmit, Insert Default, Source Violation} = 2'b100.	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Default, Source Violation} = 2'b110. or {Special TAG Transmit, Insert Default, Source Violation} = 2'b101. {Special TAG Transmit, Insert Default, Source Violation} = 2'b111.	Insert Special Tag

Special TAG	Description
Byte 0	DM Prefix 0.
Byte 1	DM Prefix 1.
Byte 2	Bit [7]: Source Violation. 1 = This packet is a source violated packet and it was modified its forwarding algorithm to the CPU port. 0 = This packet is not a source violated packet. Bit [6]: Mirror. 1 = This is a mirrored packet. 0 = This is not a mirrored packet. Bit [5]: Span. 1 = This is a span packet. 0 = This is not a span packet. Bit [4]: Management. 1 = This is a management packet. 0 = This is not a management packet. Bit [3]: Ignore. Bit [2:0]: Source Port. 000 = Port 0. 001 = Port 1. 010 = Port 2. 011 = Port 3. 100 = Port 4. 101 = Port 5.
Byte 3	Egress TAG[15:8].
Byte 4	Egress TAG[7:0].
Byte 5	Ignore.

3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:
100Base-X physical coding sub-layer (PCS)
100Base-X physical medium attachment (PMA)
100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:
10Base-T physical layer signaling (PLS)
10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:
Clock synthesizer module
MII Registers
IEEE 802.3u auto negotiation

The interfaces used for communication between PHY block and switch core is MII interface.

Auto MDIX function is supported. This function can be Enable/Disable by the hardware pin.
Digital approach for the integrated PHY of DM8606BF has been adopted.

3.2.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The DM8606BF supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the DM8606BF can be controlled either by internal register access or by the use of configuration pins are sampled. If disabled, auto negotiation will not occur until software

enables bit 12 in MII register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the DM8606BF transmits the abilities programmed into the auto negotiation advertisement register at address 04h via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiation, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05h.

The contents of the "auto negotiation link partner ability register" are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation by comparing the contents of register 04h and 05h and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.
100Base-TX full duplex (highest priority)
100Base-TX half duplex
10Base-T full duplex
10Base-T half duplex (lowest priority)

The basic mode control register at address 0h provides control of enabling, disabling, and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto negotiation enable bit (bit 12) is set.

The basic mode status register at address 1h indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the DM8606BF. The BMSR also provides status on:
Whether auto negotiation is complete (bit 5)
Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4h indicates the auto negotiation abilities to be advertised by the DM8606BF. All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05h indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1h) is set.

3.2.2 Speed/Duplex Configuration

The twelve sets of four pins listed in Table 3-1 configure the speed/duplex capability of each channel of DM8606BF. The logic states of these pins are latched into the advertisement register (register address 4h) for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0h) according to Table 3-1.

In order to make these pins have the same Read/Write priority as software, they should be programmed to 11111111b in case user likes to update the advertisement register through software.

Auto Negotiation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
				100F	100H	10F	10H	100F	100H	10F	10H
1	1	1	1	1	1	1	1	0	1	0	1
1	1	0	1	0	1	0	1	0	1	0	1

Auto Negotiation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
				100F	100H	10F	10H	100F	100H	10F	10H
1	0	1	1	0	0	1	1	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	1
0	1	1	0	1	—	—	—	—	—	—	—
0	1	0	0	—	1	—	—	—	—	—	—
0	0	1	0	—	—	1	—	—	—	—	—
0	0	0	0	—	—	—	1	—	—	—	—

Table 3-1 Speed/Duplex Configuration

3.3 Hardware, EEPROM and SMI Interface for Configuration

Three ways are supported to configure the setting in the DM8606BF: (1) Hardware Setting (2) EERPROM Interface (3) SMI Interface. Users could use EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See the following figure as a description.

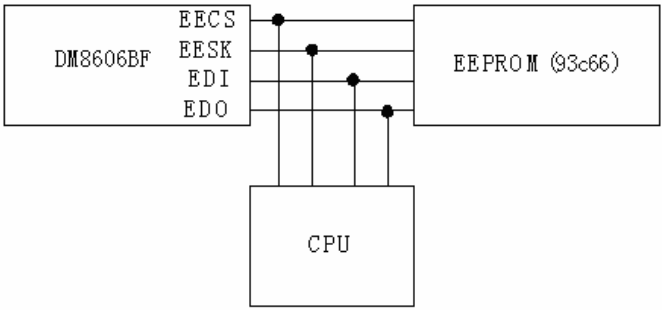


Figure 3-3 Interconnection between DM8606BF, EEPROM and CPU

3.3.1 Hardware Setting

The DM8606BF provides some hardware pins where values reside on during power on or reset will be strapped for the default setting.

Setting Name	Description
GFCEN	Global Flow Control Enable. 0 : Flow Control Capability is depended upon the register setting in corresponding EEPROM register 1 : All ports flow control capability is enabled.
SDIO_MD	SDC/SDIO mode selection. 0 : 32 bits mode 1 :.16 bits mode

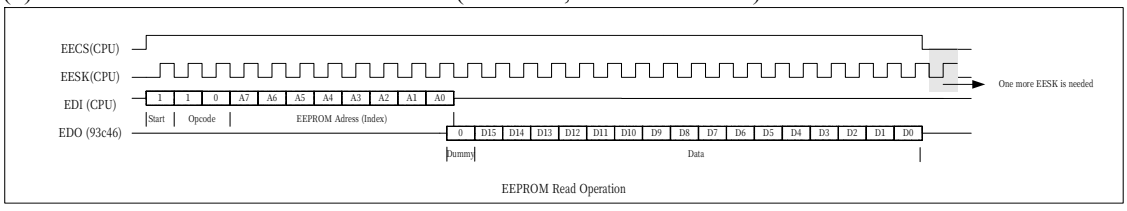
Setting Name	Description
P5_BUSMD[1:0]	Port 5 bus mode selection bit 0. P5_BUSMD[1:0] Interface 00 MII 01 GPSI 10 RMII 11 Reserved and Not Allowed.
BPEN	Recommend Back-Pressure in half-duplex. 0 : Disable Back-Pressure. 1 : Enable Back-Pressure
RECANEN	Recommend Auto Negotiation Enable. Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. 0 : Disable all TP port auto negotiation capability 1 : Enable all TP port auto negotiation capability
XOVEN	Cross Over Enable. Only available in TP interface. 1 : Enable 0 : Disable
LED_MODE	Enable Mac to choose LED Display Mode. 0 : Single color LED 1 : Dual color LED

3.3.2 EEPROM Interface

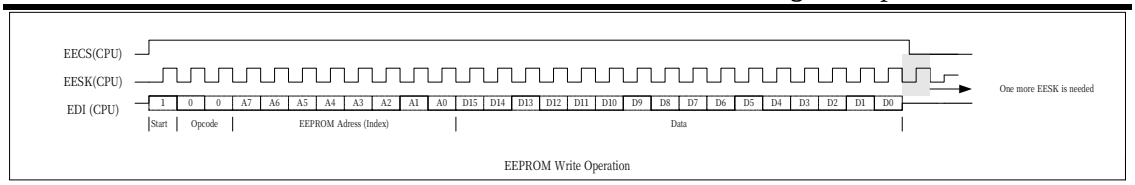
The EEPROM Interface is provided so the users could easily configure the setting without CPU's help. Because the EEPROM Interface is the same as the 93c66, it also allows the CPU to write the EEPROM register and renew the 93c66 at the same time. After the power up or reset (default value from the hardware pins fetched in this stage), the DM8606BF will automatically detect the presence of the EEPROM by reading the address 0 in the 96c66. If the value = 16'h4154, it will read all the data in the 93c66. If not, the DM8606BF will stop loading the 93c66. The user also could pull down the EDO to force the DM8606BF not to load the 93c66. The 93c66 loading time is around 30ms. Then CPU should give the high-z value in the EECS, EESK and EDI pins in this period if we really want to use CPU to read or write the registers in the DM8606BF.

The EEPROM Interface needs only one Write command to complete a writing operation. If updating the 93c66 at the same time is necessary, three commands Write Enable, Write, and Write Disable are needed to complete this job (See 93c66 Spec. for a reference). Users should note that the EERPOM interface only allows the CPU to write the EEPROM register in the DM8606BF and doesn't support the READ command. If CPU gives the Read Command, DM8606BF will not respond and 93c66 will respond with the value. Users should also note that one additional EESK cycle is needed between any continuous commands (Read or Write).

(1) Read 93c66 via the EEPROM Interface (Index = 2, Data = 16'h1111).



(2) Write EEPROM registers in the DM8606BF (Index = 2, Data =16'h2222).



3.3.3 SMI Interface

The SMI consists of two pins, management data clock (EESK) and management data input/output (EDI). The DM8606BF is designed to support an EESK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin may be needed (pulled to low) if EEPROM interface is also used.

The EDI pin requires a 1.5 KΩ pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. DM8606BF requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EESK. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to management register operation. The next field is management register address. It is 10 bits wide and the most significant bit is transferred first.

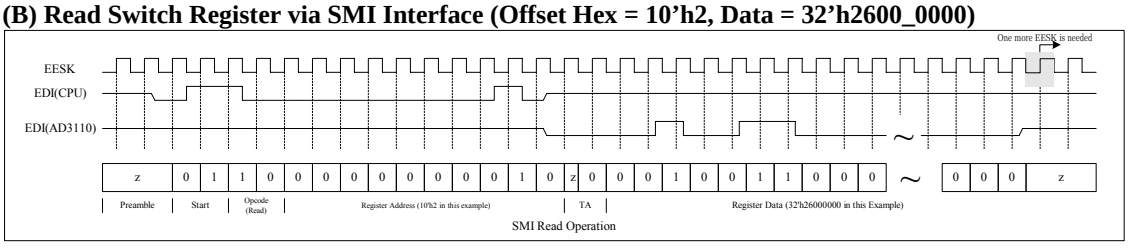
During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 32-bit data stream is read from or written into the management registers of the DM8606BF.

(A) Preamble Suppression

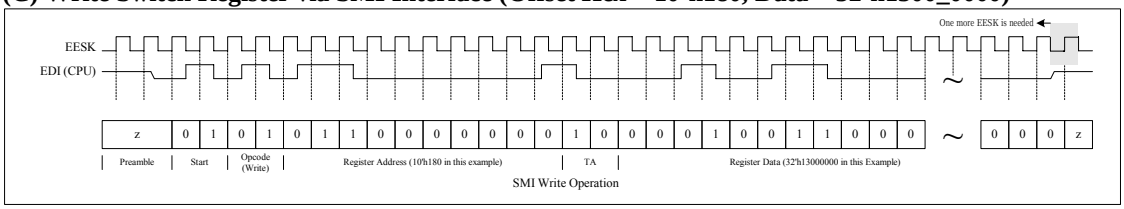
The SMI of DM8606BF supports a preamble suppression mode. The DM8606BF requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI While the DM8606BF will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When DM8606BF detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then DM8606BF will tri-state the EDI pin.

(B) Read Switch Register via SMI Interface (Offset Hex = 10'h2, Data = 32'h2600_0000)



(C) Write Switch Register via SMI Interface (Offset Hex = 10'h180, Data = 32'h1300_0000)



(D) The pin type of EECS, EESK, EDI and EDO during the operation.

Pin Name	Reset Operation	Load EEPROM	Write Operation	Read Operation
EECS	Input	Output	Input	Input
EESK	Input	Output	Input	Input
EDI	Input	Output	Input	Input/Output
EDO	Input	Input	Input	Input

Chapter 4 Register Description

4.1 EEPROM Content

EEPROM provides DM8606BF many options setting such as:

Port Configuration: Speed, Duplex, Flow Control Capability and Tag/ Untag.
VLAN & TOS Priority Mapping
Broadcast Storming rate and Trunk.
Fiber Select, Auto MDIX select
VLAN Mapping
Per Port Buffer number

4.1.1 Memory Map

Register	Definition
0x0000h~0x003fh	EEPROM BAISC Register Map
0x0040h~0x009bh	EEPROM Extended Register Map
0x00a0h~0x0143h	Counter and Switch Status Map
0x0200h~0x02ffh	PHY Register Map

4.2 EEPROM Basic Register Map

Register	Bit 15- 0			Default Value
0x00h	Signature Register			0x4154h
0x01h	P0 Basic Control Register			0x040fh
0x02h	P1 Extended Control Register		P0 Extended Control Register	0x0000h
0x03h	P1 Basic Control Register			0x040fh
0x04h	P3 Extended Control Register		P2 Extended Control Register	0x0000h
0x05h	P2 Basic Control Register			0x040fh
0x06h	P5 Extended Control Register		P4 Extended Control Register	0x0000h
0x07h	P3 Basic Control Register			0x040fh
0x08h	P4 Basic Control Register			0x040fh
0x09h	P5 Basic Control Register			0x040fh
0x0ah	System Control Register 0			0x5902h
0x0bh	System Control Register 1			0x8001h
0x0ch	Multicast Snooping Register			0x0000h
0x0dh	ARP/RARP Register			0x0000h
0x0eh	VLAN Priority Map			0xfa50h
0x0fh	TOS Priority Map			0xfa50h
0x10h	System Control Register 2			0x0040h
0x11h	System Control Register 3			0xe300h
0x12h	System Control Register 4			0x3600h
0x13h	P0 Security Option	STP P0	Forward Group 0 Port Map	0x01d5h
0x14h	P1 Security Option	STP P1	Forward Group 1 Port Map	0x01d5h
0x15h	P2 Security Option	STP P2	Forward Group 2 Port Map	0x01d5h
0x16h	P3 Security Option	STP P3	Forward Group 3 Port Map	0x01d5h
0x17h	P4 Security Option	STP P4	Forward Group 4 Port Map	0x01d5h
0x18h	P5 Security Option	STP P5	Forward Group 5 Port Map	0x01d5h
0x19h	Unicast Portmap		Forward Group 6 Port Map	0xffd5h
0x1ah	Broadcast Portmap		Forward Group 7 Port Map	0xffd5h

Register	Bit 15- 0			Default Value
0x1bh	Multicast Portmap	Forward Group 8 Port Map		0xffd5h
0x1ch	Reserve Portmap	Forward Group 9 Port Map		0xffd5h
0x1dh	Packet Identification Option	Forward Group 10 Port Map		0xffd5h
0x1eh	VLAN Priority Enable	Forward Group 11 Port Map		0xffd5h
0x1fh	Service Priority Enable	Forward Group 12 Port Map		0xffd5h
0x20h	Input Force No Tag	Forward Group 13 Port Map		0xffd5h
0x21h	Ingress Filter	Forward Group 14 Port Map		0xffd5h
0x22h	VLAN Security Disable	Forward Group 15 Port Map		0xffd5h
0x23h	Input Buffer Threshold Register 0			0x0000h
0x24h	Input Buffer Threshold Register 1			0x0000h
0x25h	Queue 1 Weight	IGMP/MPLD TRAP Enable	Input Jam Threshold	0x1000h
0x26h	Queue 2 Weight	VID Check	PPPOE Port Only	0x1000h
0x27h	Queue 3 Weight	Back to Port VLAN	Admit Only VLAN-Tagged	0x1000h
0x28h	Reserve		P0VID [11:4]	0x0000h
0x29h	Reserve		P1VID [11:4]	0x0000h
0x2ah	Output Tag Pass		P2VID [11:4]	0x3f00h
0x2bh	P4VID [11:4]		P3VID [11:4]	0x0000h
0x2ch	Reserved Address Control	TAG Shift	P5VID [11:4]	0xd000h
0x2dh	PHY Control Register			0x4442h
0x2eh	DM TAG Ether Type			0x0000h
0x2fh	PHY Restart Register			0x0000h
0x30h	Miscellaneous Register			0x0987h
0x31h	Basic Bandwidth Control Register			0x0000h
0x32h	Basic Bandwidth Control Register			0x0000h
0x33h	Bandwidth Control Enable Register			0x0000h
0x34h	Expansion Bandwidth Control Register 0			0x0000h
0x35h	Expansion Bandwidth Control Register 1			0x0000h
0x36h	Expansion Bandwidth Control Register 2			0x0000h
0x37h	Expansion Bandwidth Control Register 3			0x0000h
0x38h	Expansion Bandwidth Control Register 4			0x0000h
0x39h	Expansion Bandwidth Control Register 5			0x0000h
0x3ah	Default VLAN Member	Expansion Bandwidth Control Register 6		0x0fc0h
0x3bh	New Storm Register 0			0x0000h
0x3ch	New Storm Register 1			0x0000h
0x3dh	New Reserved Address Control Register 0			0x00fdh
0x3eh	New Reserved Address Control Register 1			0x0000h
0x3fh	Hardware IGMP Control Register			0x7c80h

4.2.1 Signature Register

offset: 0x00h

Bits	Type	Description	Initial value
15:0	RO	The value must be 16'h4154. DM8606BF uses this value to check if the EEPROM is attached. If the value in the EEPROM doesn't equal to 16'h4154h, DM8606BF will stop loading the EEPROM even if the EEPROM is attached. DM8606BF will use the default value in section 4.2 to initialize.	0x4154h

4.2.2 P0, P1, P2, P3, P4 and P5 Basic Control Registers

offset: 0x01h, 0x03h, 0x 05h, 0x07, 0x 08, 0x09h

Bits	Type	Description	Initial value

15	R/W	Crossover Auto Detect Enable (cross_ee). This bit is used together with the value (cross_hw) on the pin EESK/SDC during the power on reset and the value (wait_init) on the pin WAIT_INIT during the normal mode to decide if PHY enables this function. This bit is useless in Port 5. {wait_init, cross_hw, cross_ee} Description 1x1 = This port will enable Crossover Auto Detect Enable function. 1x0 = This port will disable Crossover Auto Detect Enable function. 01x = This port will enable Crossover Auto Detect Enable function. 000 = This port will disable Crossover Auto Detect Enable function. 001 = This port will enable Crossover Auto Detect Enable function.	1'b0
14	R/W	Select FX (selfx_ee). This bit is used together with the value (p4fx_hw) on the pin P4FX during the power on reset to decide if the PHY operates on the fiber mode. This bit is useless in Port 5. Port 0, 1, 2, 3: selfx_ee Description 0 = Port will operate in the Twisted Pair Mode. 1 = Port will operate in the Fiber Mode. Port 4: {p4fx_hw, selfx_ee} Description 1x = Port 4 will operate in the fiber mode. 00 = Port 4 will operate in the twisted mode. 01 = Port 4 will operate in the fiber mode.	1'b0
13:10	R/W	PVID[3:0]. See 0x0028h ~ 0x002ch to find the other PVID [11:4]	4'b1
9:8	R/W	Port Priority. 00 = Assign packets to Queue 0. 01 = Assign packets to Queue 1. 10 = Assign packets to Queue 2. 11 = Assign packets to Queue 3.	2'b0
7	R/W	Port Priority Enable 0 = The port priority is disabled. 1 = The port priority is enabled.	1'b0
6	R/W	IP over VLAN PRI. 0 = Use the priority bits in the tag header to assign the priority queue. 1 = Use the IP PRI to assign the priority queue.	1'b0
5	R/W	Port Disable. Port 0, 1, 2, 3, 4: 0 = PHY works normally. 1 = PHY is disabled. Port 5: 0 = Port 5 works normally. 1 = Port 5 is forced to link down.	1'b0
4	R/W	Output Packet Tagging Enable. 0 = Untagged packets are transmitted. 1 = Tagged packets are transmitted.	1'b0
3	R/W	Duplex Ability. It is useless in Port 5. 0 = Recommend PHY to work in the half duplex mode. 1 = Recommend PHY to work in the full duplex mode.	1'b1
2	R/W	Speed Ability. 0 = Recommend PHY to work in the 10M mode. 1 = Recommend PHY to work in the 100M mode.	1'b1
1	R/W	Auto Negotiation Enable. 0 = Recommend PHY to work without Auto Negotiation. 1 = Recommend PHY to work with Auto Negotiation, when the value on the pin DUPCOL0 during the power on reset is 1.	1'b1

0	R/W	Flow Control Enable. 0 = Recommend MAC to work without Pause or Back Pressure. 1 = In full duplex, recommend MAC to work with Pause when the value on the TXD0 during the power on reset is 1. In half duplex, recommend MAC to work with Back Pressure when the value on the DUPCOL2 during the power on reset is 1.	1'b1

4.2.3 P0, P1, P2, P3, P4, P5 Extended Control Registers

offset: 0x02h, 0x04h, 0x06h

Bits	Type	Description	Initial value
15	R	Reserve	1'b0
14	R/W	Aging Disable (P1, P3, and P5). 0 = Aging function is enabled. 1 = Aging function is disabled.	1'b0
13	R/W	Learning Disable (P1, P3, and P5). 0 = Learning function is enabled. 1 = Learning function is disabled.	1'b0
12:8	R/W	The maximum number of addresses learned from the port (P1, P3, and P5). 00000 = Don't constrain the number of addresses learned. others = Constrain the number of addresses learned to this value.	5'b0
7	R	Reserve	1'b0
6	R/W	Aging Disable (P0, P2, and P4). 0 = Aging function is enabled. 1 = Aging function is disabled.	1'b0
5	R/W	Learning Disable (P0, P2, and P4). 0 = Learning function is enabled. 1 = Learning function is disabled.	1'b0
4:0	R/W	The maximum number of addresses learned from the port (P0, P2, and P4). 00000 = Don't constrain the number of addresses learned. others = Constrain the number of addresses learned to this value.	5'b0

4.2.4 System Control Register 0

offset: 0x0ah

Bits	Type	Description	
15:12	R/W	ERCMPTH. It means the earlier cycles for transmission used in DM8606BF. It is for the engineer debug purpose.	4'h5
11	R/W	Priority Change Rule 0 = Use VLAN_PRI field in the matched VLAN filter. 1 = Reverse PRI in the same way as untagged packet.	1'b1
10	R/W	Priority Change Enable. 0 = Don't change the priority in the tag header. 1 = Change the priority field in the tag header.	1'b0
9	R/W	Replace VID0. 0 = Don't replace. 1 = Replace.	1'b0
8	R/W	Replace VID1. 0 = Don't replace. 1 = Replace.	1'b1
7	R/W	Replace VIDFFF. 0 = Don't replace. 1 = Replace.	1'b0
6:3	R/W	Default FID. See 3.1.14.7.	4'b0
2	R/W	New Transmit Tag Enable. 0 = Use old. 1 = Use new.	1'b0
1	R/W	TOS Using.	1'b1

		0 = Use the most significant 6-bits of the TOS field in the IPV4 header to map the priority queue. 1 = Use the most significant 3-bits of the TOS field in the IPV4 header to map the priority queue	
0	R/W	PPPOE Manage. When the port is configured a PPPOE Only, the port will only transmit the PPPOE packets. But when the packet is a management one, users could configure PPPOE Manage to 1'b1 to transmit this packet on the PPPOE Only port even if it is not a PPPOE packet. DM8606BF identifies packets with Ether-Type = 16'h8863 or 16'h8864 as the PPPOE packet.	1'b0

4.2.5 System Control Register 1

offset: 0x0bh

Bits	Type	Description	Initial value
15	R/W	Disable Far-End-Fault detection. 0 = Far-End-Fault detection is enabled. 1 = Far-End-Fault detection is disabled	1'b1
14	R/W	Input Filter. 0 = Discard packets directly when storming or the lack of input buffers. 1 = Forward packets to the un-congested port when storming or the lack of input buffers.	1'b0
13:12	R/W	Additional Snooping Control. These bits are used when the packets on the incoming port with the Ethernet destination address = 01-00-5E-XX-XX-XX/33-33-XX-XX-XX are not IGMP_IP/ MLD_IPV/MLD_IPV6 packets and not found in the learning table or the hardware IGMP table. 00 = As normal multicast packets. 01 = Drop. 10 = Send to CPU if the receiving port is non-CPU port or send to Multicast Portmap if the receiving is the CPU port. 11 = Reserve.	2'b0
11	R/W	Source Intrusion Condition. 0 = Learning table source violation doesn't consider the port match. 1 = Learning table source violation takes the port match into consideration.	1'b0
10	R/W	Source Intrusion Must. 0 = Learning table source violation will be effective in the following conditions. 1. The packets are not the management packets. 2. The packets are the management packets but Source Violation Over Reserve is 1'b1. 1 = Must follow the learning table source violation rules.	1'b0
9	R/W	Source Intrusion Action. 0 = Discard. 1 = Send to the CPU port.	1'b0
8	R/W	Carrier Mask Select. 0 = Mask CRS of 4 Cycles. 1 = Mask CRS of 5 Cycles.	1'b0
7	R/W	Port 3 and Port 4 Trunk Enable. 0 = No trunk is enabled. 1 = Port 3 and Port 4 are trunked.	1'b0
6	R/W	Transmit Short IPG Enable. 0 = 96-bits time is used. 1 = 88/96-bits time is used.	1'b0
5	R/W	CPU Port doesn't check CRC for packets with Special Tag. 0 = Check. 1 = Don't Check.	1'b0
4	R/W	Source Violation Over Reserve. This bit is used when the management packet with DA =	1'b0

		01-80-C2-00-00-XX violates the source rule. 0 = Source violation doesn't change the forwarding algorithm. 1 = Source violation will change the forwarding algorithm.	
3	R/W	Source Violation Over ARP/RARP. This bit is used when the ARP/RARP packet classified as management violates the source rule. 0 = Source violation doesn't change the forwarding algorithm. 1 = Source violation will change the forwarding algorithm.	1'b0
2	R/W	Source Violation Over Snooping. This bit is used when the MLD_IPV6/MLD_IP/IGMP/IP packet classified as management violates the source rule. 0 = Source violation doesn't change the forwarding algorithm. 1 = Source violation will change the forwarding algorithm.	1'b0
1	R/W	Source Violation Over Default. This bit is used when the packet that is not the same as the above and is classified as management violates the source rule. 0 = Source violation doesn't change the forwarding algorithm. 1 = Source violation will change the forwarding algorithm.	1'b0
0	R/W	New EEPROM. 0 = Use old EEPROM functions. 1 = New EEPROM function is enabled.	1'b1

4.2.6 Multicast Snooping Register

offset: 0x0ch

Bits	Type	Description	Initial value
15:14	R/W	Snooping Control Packet Action. 00 = IGMP Portmap is 6'b0. 01 = IGMP Portmap is the Multicast Portmap. 10 = If the incoming port is not the CPU port, then the IGMP Portmap is the CPU port. If the incoming port is the CPU port, then the IGMP Portmap is the Multicast Portmap except the CPU port. 11 = If the incoming port is not the CPU port, then the Multicast Portmap is the CPU port. If the incoming port is the CPU port, then the Multicast Portmap is the default output ports except the CPU port.	2'b0
13	R/W	Snooping Control Packet Priority Enable 0 = Disable. 1 = Enable.	1'b0
12:11	R/W	Snooping Control Packet Priority. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	2'b0
10:9	R/W	Snooping Control Packet Transmission Tag Handle. 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged. 11 = Always Untagged.	2'b0
8	R/W	Snooping Control Packet Treated as Cross_VLAN Packet. 0 = Don't identify. 1 = Identify as the cross_VLAN packet.	1'b0
7	R/W	Snooping Control Packet Treated as Management Packet. 0 = Don't identify. 1 = Identify as the management packet.	1'b0
6	R/W	Snooping Control Packet Treated as Span Packet. 0 = Don't identify. 1 = Identify as the span packet.	1'b0

5	R/W	Trap MLD_IPV6 Packet. 0 = Don't trap. 1 = Trap.	1'b0
4	R/W	Trap MLD_IP Packet. 0 = Don't trap. 1 = Trap.	1'b0
3	R/W	Trap IGMP_IP Packet. 0 = Don't Trap. 1 = Trap.	1'b0
2	R/W	Hardware IGMP Packet Ignore CPU Port 0 = IGMP packet forwards to CPU also when Hardware IGMP Snooping is enabled. 1= IGMP packet doesn't forward to CPU when Hardware IGMP Snooping is enabled.	1'b0
1	R/W	Hardware IGMP Snooping Enable. 0 = Disable Hardware IGMP Snooping. 1 = Enable Hardware IGMP Snooping.	1'b0
0	R/W	Hardware IGMP Default Router Enable. 0 = Disable. 1 = Enable.	1'b0

4.2.7 ARP/RARP Register

offset: 0x0dh

Bits	Type	Description	Initial value
15	R	Reserve	1'b0
14	R/W	IP Multicast Packet Treated as Cross_VLAN packet. 0 = Don't identify. 1 = Identify as the cross_VLAN packet.	1'b0
13	R/W	Unicast packet Treated as Cross_VLAN packet. 0 = Don't identify. 1 = Identify as the cross_VLAN packet when there is a match in the learning table.	1'b0
12	R/W	RARP Packet Treated as Cross_VLAN Packet. 0 = Don't identify. 1 = Identify as the cross_VLAN packet.	1'b0
11:10	R/W	RARP/ARP Packet Action. 00 = ARP/RARP Portmap is 6'b0. 01 = ARP/RARP Portmap is the Broadcast Portmap. 10 = If the incoming port is not the CPU port, then the ARP/RARP Portmap is the CPU port. If the incoming port is the CPU port, then the ARP/RARP Portmap is the Broadcast Portmap except the CPU port. 11 = If the incoming port is not the CPU port, then the ARP/RARP Portmap is the CPU port. If the incoming port is the CPU port, then the ARP/RARP Portmap is the default output ports except the CPU port.	2'b0
9	R/W	RARP/ARP Packet Priority Enable. 0 = Disable. 1 = Enable.	1'b0
8:7	R/W	RARP/ARP Packet Priority. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	2'b0
6:5	R/W	RARP/ARP Packet Output Tag Handle. 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged.	2'b0

		11 = Always Untagged.	
4	R/W	ARP Packet Treated as Cross_VLAN Packet. 0 = Don't identify. 1 = Identify as the cross_VLAN packet.	1'b0
3	R/W	RARP/ARP Packet Treated as Management Packet. 0 = Don't identify. 1 = Identify as the management packet.	1'b0
2	R/W	RARP/ARP Packet Treated as Span Packet. 0 = Don't identify. 1 = Identify as the span packet.	1'b0
1	R/W	Trap ARP Packet. 0 = Don't Trap. 1 = Trap.	1'b0
0	R/W	Trap RARP Packet. 0 = Don't Trap. 1 = Trap.	1'b0

4.2.8 VLAN Priority Map Register

offset: 0x0eh

Bits	Type	Description	Initial value
15:14	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b111 are received on the port. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	2'b11
13:12	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b110 are received on the port.	2'b11
11:10	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b101 are received on the port.	2'b10
9:8	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b100 are received on the port.	2'b10
7:6	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b011 are received on the port.	2'b01
5:4	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b010 are received on the port.	2'b01
3:2	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b001 are received on the port.	2'b00
1:0	R/W	These 2 bits are used as the priority queue when the tagged packets with the user priority = 3'b000 are received on the port.	2'b00

4.2.9 TOS Priority Map Register

offset: 0x0fh

Bits	Type	Description	Initial value
15:14	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b111. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	2'b11
13:12	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b110.	2'b11

Bits	Type	Description	Initial value
11:10	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b101.	2'b10
9:8	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b100.	2'b10
7:6	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b011.	2'b01
5:4	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b010.	2'b01
3:2	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b001.	2'b00
1:0	R/W	These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 3'b000.	2'b00

4.2.10 System Control Register 2

offset: 0x10h

Bits	Type	Description	Initial value
15:14	R/W	Discard Mode (Drop scheme for Packets Classified as Q3). See Smart Discard.	2'b0
13:12	R/W	Discard Mode (Drop scheme for Packets Classified as Q2). See Smart Discard.	2'b0
11:10	R/W	Discard Mode (Drop scheme for Packets Classified as Q1). See Smart Discard.	2'b0
9:8	R/W	Discard Mode (Drop scheme for Packets Classified as Q0). See Smart Discard.	2'b0
7	R/W	Aging Disable. (Useless in DM8606BF) 0 = Age enable. 1 = Age disable.	1'b0
6	R/W	Rx Clock Change to Tx Clock for GPSI Interface. 0 = DM8606BF doesn't use Tx clock to replace Rx clock when Rx clock stops. 1 = DM8606BF uses Tx clock to replace Rx clock when Rx clock stops	1'b1
5	R/W	Multicast Packet Counted into the Storm Counter. 0 = Only broadcast packets are counted into the storming counter. 1 = Multicast and broadcast packets are counted into the storming counter.	1'b0
4	R/W	CRC Check Disable. 0 = Check CRC. 1 = Don't check CRC.	1'b0
3	R/W	Back Off Disable. 0 = Back-off is enabled. 1 = Back-off is disabled.	1'b0
2	R/W	Storming Enable. It is used in old storm control. 0 = Enable. 1 = Discard.	1'b0
1:0	R/W	Storming Threshold[1:0]. It is used in old storm control.	1'b0

4.2.11 System Control Register 3

offset: 0x11h

Bits	Type	Description	Initial value
15:13	R/W	CPU Port Number. 000 = The CPU is attached to Port 0. 001 = The CPU is attached to Port 1. 010 = The CPU is attached to Port 2. 011 = The CPU is attached to Port 3. 100 = The CPU is attached to Port 4. 101 = The CPU is attached to Port 5. 110 or 111 = No CPU exists.	3'b111

Bits	Type	Description	Initial value
12	R/W	Special TAG Receive Enable. 0 = DM8606BF doesn't identify the Special TAG for the incoming packets. 1 = DM8606BF identifies the Special TAG for the incoming packets.	1'b0
11	R/W	Special TAG Transmit Enable. 0 = DM8606BF doesn't insert Special TAG for the packets transmitted to the CPU port. 1 = DM8606BF inserts Special TAG for the packets transmitted to the CPU port.	1'b0
10	R/W	Pause also adds Special Tag when Special TAG Transmit is enabled. 0 = Don't add Special Tag on the PAUSE packets. 1 = Add Special Tag in the PAUSE packets.	1'b0
9:7	R/W	Max Packet Length (MAXPKTLEN) 110 = 1522 bytes. 000 = 1518 bytes. 001 = 1536 bytes. 010 = 1664 bytes other = 1784 bytes.	3'b110
6	R/W	New Storming Enable. 0 = Use the DM8606F storming control. 1 = Use the DM8606BF storming control.	1'b0
5	R/W	Tag Base VLAN. 0 = Port VLAN 1 = Tagged VLAN.	1'b0
4	R/W	MAC Clone Enable. 0 = Mac Clone is disabled. 1 = Mac Clone is enabled.	1'b0
3	R/W	Queue Option. It's the test for the designer in the queue control.	1'b0
2	R /W	Interrupt Polarity Inverter. 0 = The interrupt signal is active pull low. 1 = The interrupt signal is active pull high.	1'b0
1:0	R/W	Aging Timer Select. 00 = 300 Seconds. 01 = 75 Seconds. 10 = 18 Seconds. 11 = 1 Seconds	2'b0

4.2.12 System Control Register 4

offset: 0x12h

Bits	Type	Description	Initial value
15	R/W	Drop Packet When Excessive Collision Happen. 0 = Don't drop. 1 = Drop.	1'b0
14	R/W	Duplex and Col Separate. 0 = Indicate the duplex and collision status at the same time. 1 = Indicate the duplex status only.	1'b0
13:12	R/W	Power Saving Select. 11	2'b11
11	R/W	Ten Limit Enable. This function works only when Full Flow Control/Half Back Pressure is enabled. 1 = The switch will forward packets with Multicast, Broadcast, or Unicast but not learned DA addresses from 100Mbps only to 100Mbps ports and ignore the 10M paths when the ten limit reaches. This function allows the switch to balance the high and the low speed. 0 = The switch will not ignore 10Mbps paths even when the ten limit reaches.	1'b0
10	R/W	Enable Transmit Power Saving. 1	1'b1

Bits	Type	Description	Initial value
		0 = Disable 1 = Enable	
9	R/W	Enable DRV62MA. 1 0 = Disable 1 = Enable	1'b1
8	R/W	OLD P5 First Lock. 0 = First Lock is disabled. 1 = First Lock is enabled.	0x0h
7	R/W	OLD P4 First Lock. 0 = First Lock is disabled. 1 = First Lock is enabled.	0x0h
6	R/W	OLD P3 First Lock.. 0 = First Lock is disabled. 1 = First Lock is enabled.	0x0h
5	R/W	Pause Ignore. 0 = Don't ignore Pause packets. 1 = Ignore Pause packets in half duplex or in full duplex when flow control is not enabled.	0x0h
4	R/W	OLD P2 First Lock. 0 = First Lock is disabled. 1 = First Lock is enabled.	0x0h
3	R/W	Dual Color in SDC/SDIO with CPU. See 3.1.12 LED Display 1 = Dual Color. 0 = Single Color.	0x0h
2	R/W	OLD P1 First Lock. 0 = First Lock is disabled. 1 = First Lock is enabled.	0x0h
1	R/W	LED Enable. 0 = Disable. 1 = Enable	0x0h
0	R/W	OLD P0 First Lock. 0 = First Lock is disabled. 1 = First Lock is enabled.	0x0h

4.2.13 Port Security Option, Port Spanning Tree State and Forward Group Port Map

offset: 0x13h ~ 0x18h

Bits	Type	Description	Initial value
15	R	Reserve	1'b0
14	R/W	Close Port. 0 = Don't close the port. 1 = When port security exists, the port is closed automatically.	1'b0
13:11	R/W	Port Security Option. 011 = First Lock 100 = First Link Lock 101 = Assign Lock 110 = Assign Link Lock 010 = Discard Unknown 001 = Unknown to CPU	3'000
10:9	R/W	Spanning Tree Port Status. The DM8606BF supports 4 port status to support Spanning Tree Protocol. 00 = Forwarding State. The port acts as the normal mode. 01 = Disabled State. The port entity will not transmit and receive any packets. Learning	1'b0

		is disabled in this state. 10 = Learning State. The port entity will only transmit and receive span packets. All other packets are discarded. Learning is enabled for all good frames. 11 = Blocking/Listening. Only the span packets defined by DM8606BF will be received and transmitted. All other packets are discarded by the port entity. Learning is disabled in this state.	
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b1
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b1
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b1
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.14 Unicast Portmap and Forward Group Port Map

offset: 0x19h

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Unicast Portmap. See 3.1.19.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member.	1'b1

		1 = Port 0 is a member.	

4.2.15 Broadcast Portmap and Forward Group Port Map

offset: 0x1ah

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Broadcast Portmap. See 3.1.19.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.16 Multicast Portmap and Forward Group Port Map

offset: 0x1bh

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Multicast Portmap See 3.1.19.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0

0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.17 Reserve Portmap and Forward Group Port Map

offset: 0x1ch

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Reserve Portmap See 3.1.19.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.18 Packet Identification Option, Forward Group Port Map

offset: 0x1dh

Bits	Type	Description	Initial value
15	R/W	MLD Snooping Protocol Header. 0 = Protocol Header is 8'h01. 1 = Protocol Header is 8'h3a.	1'b1
14	R/W	Don't identify VLAN after SNAP. 0 = Identify. 1 = Don't identify.	1'b1
13	R/W	Don't identify IPV6 in PPPOE. 0 = Identify. 1 = Don't identify.	1'b1
12	R/W	Don't identify IP in PPPOE after SNAP. 0 = Identify. 1 = Don't identify.	1'b1
11	R/W	Don't identify Ether-Type = 16'h0800, IP VER = 6 as IPV6 packets. 0 = Identify. 1 = Don't identify.	1'b1
10	R/W	Don't identify IP in PPPOE. 0 = Identify. 1 = Don't identify.	1'b1

9	R/W	Don't Identify SNAP. 0 = Identify. 1 = Don't Identidy.	1'b1
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.19 VLAN Priority Enable and Forward Group Port Map

offset: 0x1eh

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	VLAN Priority Enable. 0 = Don't care the PRI in the tag header 1 = PRI in the tag header will be taken into priority determination consideration.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.20 Service Priority Enable and Forward Group Port Map

offset: 0x1fh

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Service Priority Enable. 0 = Don't care IPV4 TOS/IPV6 Traffic Class. 1 = Care IPV4 TOS/IPV6 Traffic for priority decision.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.21 Input Force No Tag and Forward Group Port Map

offset: 0x20h

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Input Force No TAG Enable. 0 = Disabled. 1 = Enabled.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member.	1'b1

		1 = Port 1 is a member.	
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.22 Ingress Filter and Forward Group Port Map

offset: 0x21h

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	Ingress Filter Enable. 0 = Don't filter. 1 = Filter.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0
4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.23 VLAN Security Disable and Forward Group Port Map

offset: 0x22h

Bits	Type	Description	Initial value
15	R	Reserve	1'b1
14:9	R/W	VLAN Security Disable. 0 = Don't disable. 1 = Disable.	6'b111111
8	R/W	Port 5 is a member of the Forwarding Group 0 = Port 5 is not a member. 1 = Port 5 is a member.	1'b1
7	R/W	Port 4 is a member of the Forwarding Group. 0 = Port 4 is not a member. 1 = Port 4 is a member.	1'b1
6	R/W	Port 3 is a member of the Forwarding Group. 0 = Port 3 is not a member. 1 = Port 3 is a member.	1'b1
5	R	Reserve	1'b0

4	R/W	Port 2 is a member of the Forwarding Group 0 = Port 2 is not a member. 1 = Port 2 is a member.	1'b1
3	R	Reserve	1'b0
2	R/W	Port 1 is a member of the Forwarding Group. 0 = Port 1 is not a member. 1 = Port 1 is a member.	1'b1
1	R	Reserve	1'b0
0	R/W	Port 0 is a member of the Forwarding Group. 0 = Port 0 is not a member. 1 = Port 0 is a member.	1'b1

4.2.24 Buffer Threshold Register 0

offset: 0x23h

Bits	Type	Description	Initial value
15:14	R/W	Port Unfull Offset 3	2'b0
13:12	R/W	Port Unfull Offset 2	2'b0
11:10	R/W	Port Unfull Offset 1	2'b0
9:8	R/W	Port Unfull Offset 0	2'b0
7:6	R/W	Port Full Offset 3	2'b0
5:4	R/W	Port Full Offset 2	2'b0
3:2	R/W	Port Full Offset 1	2'b0
1:0	R/W	Port Full Offset 0	2'b0

4.2.25 Buffer Threshold Register 1

offset: 0x24h

Bits	Type	Description	Initial value
15:14	R	Reserve	2'b0
13	R/W	Total Low Add	1'b0
12	R/W	Total High Add	1'b0
11:10	R/W	Total Low Offset	2'b0
9:8	R/W	Total High Offset	2'b0
7:4	R/W	Port Unfull Add	2'b0
3:0	R/W	Port Full Add	2'b0

4.2.26 IGMP/MLD TRAP Enable, and Input Jam Threshold Register

offset: 0x25h

Bits	Type	Description	Initial value
15:12	R/W	Queue 1 Weight. See 3.1.15.	4'b0001
11:6	R/W	IGMP/MLD Trap Enable. It is a per port function. 0 = The port doesn't enable its multicast snooping function. Trap MLD_IPV6, MLD_IP and IGMP_IP are useless in this port. 1 = The port enables its multicast snooping function. Trap MLD_IPV6, MLD_IP and IGMP_IP are useful in this port.	6'b0
5:0	R/W	Input Jam Threshold.	6'b0

4.2.27 Queue 2 Weight, VID Exist Check, and PPPOE Port Only

offset: 0x26h

Bits	Type	Description	Initial value
15:12	R/W	Queue 2 Weight. See 3.1.15.	4'b0001

11:6	R/W	VID Check. 0 = Don't check. 1 = check. 0 = Don't Check. It is a per port function.	6'b000000
5:0	R/W	PPPOE Port Only. It's a per port function. 0 = The port is not a PPPOE Only port. 1 = The port is a PPPOE Only port.	6'b000000

4.2.28 Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged

offset: 0x27h

Bits	Type	Description	Initial value
15:12	R/W	Queue 3 Weight. See 3.1.15.	4'b0001
11:6	R/W	Back To Port VLAN. It is a per port function. 0 = Don't back to Port VLAN. 1 = Back to Port VLAN.	6'b000000
5:0	R/W	Admit Only VLAN_Tagged Packet. It is a per port function. 0 = The port don't check if the packets are VLAN-Tagged. 1 = The port drops the packets that carry no VID. (That is Untagged Packets or Priority-Tagged Packets.)	6'b000000

4.2.29 Input Double Tag Enable, and P0VID[11:4]

offset: 0x28h

Bits	Type	Description	Initial value
15:14	R/W	Reserve	2'00
13:8	R/W	Input Double Tag Enable. (Reserve)	6'b0
7:0	R/W	P0VID[11:4]	8'b0

4.2.30 Output Double Tag Enable, and P1VID[11:4]

offset: 0x29h

Bits	Type	Description	Initial value
15:14	R/W	REC_SELAB for Port1, Port2 and Port3. REC_SELAB = 2'b10	2'b0
13:12	R/W	REC_SELAB for Port0 and Port4. REC_SELAB = 2'b01	2'b0
11:8	R/W	Output Double Tag Enable. (Reserve)	4'b0
7:0	R/W	P1VID[11:4]	8'b0

4.2.31 Output Tag Bypass, and P2VID[11:4]

offset, 0x2ah

Bits	Type	Description	Initial value
15:14	R/W	REC_IBSL_SEL REC_IBSL_SEL = 2'b01	2'b0
13:8	R/W	Output Tag Bypass Enable. It's a per port function. See 3.1.14.2.	6'b11_1111
7:0	R/W	P2VID[11:4]	8'b0

4.2.32 P3VID[11:4], and P4VID[11:4]

offset: 0x2bh

Bits	Type	Description	Initial value
15:8	R/W	P4VID[11:4]	8'b0
7:0	R/W	P3VID[11:4]	8'b0

4.2.33 Reserved Address Control, and P5VID[11:4]

offset: 0x2ch

Bits	Type	Description	Initial value
15	R/W	The Action of MAC Address = 0180c2000010~ff	1'b1
14	R/W	The Action of MAC Address = 0180c2000002~0f	1'b1
13	R/W	The Action of MAC Address = 0180c2000001	1'b0
12	R/W	The Action of MAC Address = 0180c2000000	1'b1
11:8	R/W	Tag Shift	4'b0
7:0	R/W	P5VID[11:4]	8'b0

4.2.34 PHY Control Register

offset: 0x2dh

Bits	Type	Description	Initial value
15	R/W	Chip ID Check Disable. 0 = Check CHIP ID in 32 bit SDC/SDO. 1 = Don't check CHIP ID in 32 bit SDC/SDIO.	1'b0
14	R/W	REC_CBDETEN. 1 = Enable 0 = Disable	1'b1
13	R/W	REC_MCC_AVERAGE. 0 = Enable 1 = Disable	1'b0
12:11	R/W	LFAILTM.	2'b0
10	R/W	INTCHKEN.	1'b1
9	R/W	FGDLINK.	1'b0
8	R/W	NTH.	1'b0
7	R/W	DISJAB.	1'b0
6	R/W	ENRJAB.	1'b1
5	R/W	APOLDIS.	1'b0
4	R/W	IINSEL.	1'b0
3:2	R/W	ISHSEL.	2'b0
1:0	R/W	FILTSEL.	2'b10

4.2.35 DM TAG Ether Type

offset: 0x2eh

Bits	Type	Description	Initial value
15:0	R/W	DM TAG Ether Type. This value is used by the user to define their Ether-Type. When Special Tag Receive is enabled, DM8606BF checks the packets on the CPU port to see if the two bytes following the SA are the same as DM TAG Ether Type. If they are different, DM8606BF bypasses the Special Tag. If the same, DM8606BF will use the value in the Special Tag to do switching decisions.	16'b0

4.2.36 PHY Restart Register

offset: 0x2fh

Bits	Type	Description	Initial value
15:0	R/W	Restart. DM8606BF writes this register to restart all the PHYs in the switch. The value written is not important.	16'b0

4.2.37 Miscellaneous Register

offset: 0x30h

Bits	Type	Description	Initial value
15	R/W	REC_10MHIGHV. 0	1'b0

Bits	Type	Description	Initial value
14	R/W	REC_SEL09CURRENT.	1'b0
13	R/W	REC_SEL5MA.	1'b0
12	R/W	Port 4 LED Mode.	1'b0
11	R/W	Reserved	1'b1
10	R/W	Reserved	1'b0
9	R/W	Dual Speed Hub COL_LED Enable.	1'b0
8	R/W	Drop packets when the link partner doesn't follow the PAUSE protocol.	1'b1
7	R/W	BYPASS	1'b1
6	R/W	Reserved	1'b0
5	R/W	MAC Clone Enable Bit[1].	1'b0
4	R/W	HOL Congestion Threshold.	1'b0
3	R/W	VOLDM8606BF3_100M. 1	1'b0
2	R/W	Old Interface. 1 = 32 bit interface is the same as DM8606F when SDC/SDIO access speed is not an issue. 0 = 32 bit interface is different from DM8606F when reading eeprom register 0x0012 ~0x0023.	1'b1
1	R/W	VOLDM8606BF3_10M.	1'b1
0	R/W	ROM_CODE25.	1'b1

4.2.38 Basic Bandwidth Control Register 0

offset: 0x31h

Bits	Type	Description	Initial value
15	R/W	Port 3 Receive Bandwidth Maximum[3] (r3bw_th1).	1'b0
14:12	R/W	Port 3 Receive Bandwidth Configuration Port 3 Receive Bandwidth Maximum[2:0] (r3bw_th0).	2'b0
11	R/W	Port 2 Receive Bandwidth Maximum[3] (r2bw_th1).	1'b0
10:8	R/W	Port 2 Receive Bandwidth Configuration Port 2 Receive Bandwidth Maximum[2:0] (r2bw_th0).	2'b0
7	R/W	Port 1 Receive Bandwidth Maximum[3] (r1bw_th1).	1'b0
6:4	R/W	Port 1 Receive Bandwidth Configuration Port 1 Receive Bandwidth Maximum[2:0] (r1bw_th0).	2'b0
3	R/W	Port 0 Receive Bandwidth Maximum[3] (r0bw_th1).	1'b0
2:0	R/W	Port 0 Receive Bandwidth Configuration Port 0 Receive Bandwidth Maximum[2:0] (r0bw_th0).	2'b0

4.2.39 Basic Bandwidth Control Register 1

offset: 0x32h

Bits	Type	Description	Initial value
15	R/W	Port 1 Transmit Bandwidth Maximum[3] (t1bw_th1).	1'b0
14:12	R/W	Port 1 Transmit Bandwidth Maximum[2:0] (t1bw_th0)	2'b0
11	R/W	Port 0 Transmit Bandwidth Maximum[3] (t0bw_th1).	1'b0
10:8	R/W	Port 0 Transmit Bandwidth Maximum[2:0] (t0bw_th0).	1'b0
7	R/W	Port 5 Receive Bandwidth Maximum[3] (r5bw_th1).	1'b0
6:4	R/W	Port 5 Receive Bandwidth Configuration Port 5 Receive Bandwidth Maximum[2:0] (r5bw_th0).	2'b0
3	R/W	Port 4 Receive Bandwidth Maximum[3] (r4bw_th1).	1'b0
2:0	R/W	Port 4 Receive Bandwidth Configuration Port 4 Receive Bandwidth Maximum[2:0] (r4bw_th0).	2'b0

4.2.40 Bandwidth Control Enable Register

offset: 0x33h

Bits	Type	Description	Initial value
15	R/W	Invert P4 Clock in PCS. 0 : Disable 1 : Enable	1'b0
14	R/W	Check the length of CRS 0 : Enable 1 : Disable	1'b0
13	R/W	Reserved.	1'b0
12	R/W	DM8606BF New Bandwidth Control Enable. 0 = Disable. 1 = Enable.	1'b0
11	R/W	Port 5 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t5bw_th3, t5bw_th2, t5bw_th1, t5bw_th0, 6'b0} Kbps. K = 1000.	1'b0
10	R/W	Port 4 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t4bw_th3, t4bw_th2, t4bw_th1, t4bw_th0, 6'b0} Kbps. K = 1000.	1'b0
9	R/W	Port 3 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t3bw_th3, t3bw_th2, t3bw_th1, t3bw_th0, 6'b0} Kbps. K = 1000.	1'b0
8	R/W	Port 5 Receive Bandwidth Control Enable. 0 = Disable. 1 = Enable. The receive bandwidth is {r5bw_th3, r5bw_th2, r5bw_th1, r5bw_th0, 6'b0} Kbps. K = 1000.	1'b0
7	R/W	Port 4 Receive Bandwidth Control Enable. 0 = Disable. 1 = Enable. The receive bandwidth is {r4bw_th3, r4bw_th2, r4bw_th1, r4bw_th0, 6'b0} Kbps. K = 1000.	1'b0
6	R/W	Port 3 Receive Bandwidth Control Enable. 0 = Disable. 1 = Enable. The receive bandwidth is {r3bw_th3, r3bw_th2, r3bw_th1, r3bw_th0, 6'b0} Kbps. K = 1000.	1'b0
5	R/W	Port 2 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t2bw_th3, t2bw_th2, t2bw_th1, t2bw_th0, 6'b0} Kbps. K = 1000.	1'b0
4	R/W	Port 2 Receive Bandwidth Control Enable. 0 = Disable. 1 = Enable. The receive bandwidth is {r2bw_th3, r2bw_th2, r2bw_th1, r2bw_th0, 6'b0} Kbps. K = 1000.	1'b0
3	R/W	Port 1 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t1bw_th3, t1bw_th2, t1bw_th1, t1bw_th0, 6'b0} Kbps. K = 1000.	1'b0
2	R/W	Port 1 Receive Bandwidth Control Enable. 0 = Disable. 1 = Enable. The receive bandwidth is {r1bw_th3, r1bw_th2, r1bw_th1, r1bw_th0, 6'b0} Kbps. K = 1000.	1'b0

Bits	Type	Description	Initial value
1	R/W	Port 0 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t0bw_th3, t0bw_th2, t0bw_th1, t0bw_th0, 6'b0} Kbps. K = 1000.	1'b0
0	R/W	Port 0 Receive Bandwidth Control Enable. 0 = Disable. 1 = Enable. The receive bandwidth is {r0bw_th3, r0bw_th2, r0bw_th1, r0bw_th0, 6'b0} Kbps. K = 1000.	1'b0

4.2.41 Extended Bandwidth Control Register 0

offset: 0x34h

Bits	Type	Description	Initial value
15	R/W	Port 5 Transmit Bandwidth Maximum[3] (t5bw_th1).	1'b0
14:12	R/W	Port 5 Transmit Bandwidth Maximum[2:0] (t5bw_th0).	2'b0
11	R/W	Port 4 Transmit Bandwidth Maximum[3] (t4bw_th1).	1'b0
10:8	R/W	Port 4 Transmit Bandwidth Maximum[2:0] (t4bw_th0).	2'b0
7	R/W	Port 3 Transmit Bandwidth Maximum[3] (t3bw_th1).	1'b0
6:4	R/W	Port 3 Transmit Bandwidth Maximum[2:0] (t3bw_th0).	2'b0
3	R/W	Port 2 Transmit Bandwidth Maximum[3] (t2bw_th1).	1'b0
2:0	R/W	Port 2 Transmit Bandwidth Maximum[2:0] (t2bw_th0).	2'b0

4.2.42 Extended Bandwidth Control Register 1

offset: 0x35h

Bits	Type	Description	Initial value
15:12	R/W	Port 3 Receive Bandwidth Maximum[7:4] (r3bw_th2).	4'b0
11:8	R/W	Port 2 Receive Bandwidth Maximum[7:4] (r2bw_th2).	4'b0
7:4	R/W	Port 1 Receive Bandwidth Maximum[7:4] (r1bw_th2).	4'b0
3:0	R/W	Port 0 Receive Bandwidth Maximum[7:4] (r0bw_th2).	4'b0

4.2.43 Extended Bandwidth Control Register 2

offset: 0x36h

Bits	Type	Description	Initial value
15:10	R/W	Port 1 Transmit Bandwidth Maximum[7:4] (t1bw_th2).	4'b0
11:8	R/W	Port 0 Transmit Bandwidth Maximum[7:4] (t0bw_th2).	4'b0
7:4	R/W	Port 5 Receive Bandwidth Maximum[7:4] (r5bw_th2).	4'b0
3:0	R/W	Port 4 Receive Bandwidth Maximum[7:4] (r4bw_th2).	4'b0

4.2.44 Extended Bandwidth Control Register 3

offset: 0x37h

Bits	Type	Description	Initial value
15:12	R/W	Port 5 Transmit Bandwidth Maximum[7:4] (t5bw_th2)	4'b0
11:8	R/W	Port 4 Transmit Bandwidth Maximum[7:4] (t4bw_th2)	4'b0
7:4	R/W	Port 3 Transmit Bandwidth Maximum[7:4] (t3bw_th2)	4'b0
3:0	R/W	Port 2 Transmit Bandwidth Maximum[7:4] (t2bw_th2).	4'b0

4.2.45 Extended Bandwidth Control Register 4

offset: 0x38h

Bits	Type	Description	Initial value
15	R/W	Port 0 MDIX Control. It is useful when Port 0 Crossover Auto Detect is disabled and 16	1'b0

Bits	Type	Description	Initial value
		bits management interface (SDC/SDIO) is used. 0 = Using MDI 1 = Using MDIX	
14:12	R/W	Port 4 Receive Bandwidth Maximum[10:8] (r4bw_th3).	3'b0
11:9	R/W	Port 3 Receive Bandwidth Maximum[10:8] (r3bw_th3).	3'b0
8:6	R/W	Port 2 Receive Bandwidth Maximum[10:8] (r2bw_th3).	3'b0
5:3	R/W	Port 1 Receive Bandwidth Maximum[10:8] (r1bw_th3).	3'b0
2:0	R/W	Port 0 Receive Bandwidth Maximum[10:8] (r0bw_th3).	3'b0

4.2.46 Extended Bandwidth Control Register 5

offset: 0x39h

Bits	Type	Description	Initial value
15	R/W	Port 1 MDIX Control. It is useful when Port 1 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 = Using MDI 1 = Using MDIX	1'b0
14:12	R/W	Port 3 Transmit Bandwidth Maximum[10:8] (t3bw_th3).	3'b0
11:9	R/W	Port 2 Transmit Bandwidth Maximum[10:8] (t2bw_th3).	3'b0
8:6	R/W	Port 1 Transmit Bandwidth Maximum[10:8] (t1bw_th3).	3'b0
5:3	R/W	Port 0 Transmit Bandwidth Maximum[10:8] (t0bw_th3).	3'b0
2:0	R/W	Port 5 Receive Bandwidth Maximum[10:8] (r5bw_th3).	3'b0

4.2.47 Default VLAN Member and Extended Bandwidth Control Register 6

offset: 0x3ah

Bits	Type	Description	Initial value
15:12	R/W	Reserve	4'b0
11:6	R/W	Default VLAN Member.	6'b11_1111
5:3	R/W	Port 5 Transmit Bandwidth Maximum[10:8] (t5bw_th3).	3'b0
2:0	R/W	Port 4 Transmit Bandwidth Maximum[10:8] (t4bw_th3).	3'b0

4.2.48 New Storm Register 0

offset: 0x3bh

Bits	Type	Description	Initial value
15	R	Reserve	1'b0
14	R/W	Storm Drop Enable. 0 = Don't drop in the storming period. 1 = Drop in the storming period.	1'b0
13	R/W	Storm Enable. 0 = The storm threshold is of no effect. 1 = The storm threshold is in effect.	1'b0
12:0	R/W	100M Threshold. It is used when all ports link up in the 100M. The upper bound is reached when the number of the packets received during the 50ms is over 100M Threshold.	13'b0

4.2.49 New Storm Register 1

offset: 0x3ch

Bits	Type	Description	Initial value
15	R/W	Port 4 MDIX Control. It is useful when Port 4 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 = Using MDI	1'b0

Bits	Type	Description	Initial value
		1 = Using MDIX	
14	R/W	Port 3 MDIX Control. It is useful when Port 3 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 = Using MDI 1 = Using MDIX	1'b0
13	R/W	Port 2 MDIX Control. It is useful when Port 2 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 = Using MDI 1 = Using MDIX	1'b0
12:0	R/W	10M Threshold. See function description. It is used when one of ports link up in the 10M. The upper bound is reached when the number of the packets received during the 50ms is over 10M Threshold.	13'b0

4.2.50 New Reserve Address Control Register 0

offset: 0x3dh

Bits	Type	Description	Initial value
15:14	R/W	New Reserve TXTAG for BPDU. 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged. 11 = Always Untagged.	2'b0
13:12	R/W	PRI for GXRP. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	6'b0
11:10	R/W	PRI for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	2'b0
9:8	R/W	PRI for BPDU. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3.	2'b0
7	R/W	RESER_R3 Pass Portmap. 0 = RESER_R3 Pass Portmap is 6'b00_0000. 1 = RESER_R3 Pass Pormap is 6'b11_1111.	1'b1
6	R/W	RESER_R2 Pass Portmap. 0 = RESER_R2 Pass Portmap is 6'b00_0000. 1 = RESER_R2 Pass Pormap is 6'b11_1111.	1'b1
5	R/W	GXRP Pass Portmap. 0 = GXRP Pass Portmap is 6'b00_0000. 1 = GXRP Pass Pormpap is 6'b11_1111.	1'b1
4	R/W	RESER_R1 Pass Portmap. 0 = RESER_R1 Pass Portmap is 6'b00_0000. 1 = RESER_R1 Pass Portmap is 6'b11_1111.	1'b1
3	R/W	RESER_R0 Pass Portmap. 0 = RESER_R0Pass Portmap is 6'b00_0000. 1 = RESER_R0Pass Portmap is 6'b11_1111.	1'b1
2	R/W	PAE Pass Portmap.	1'b1

Bits	Type	Description	Initial value
		0 = PAE Pass Portmap is 6'b00_0000. 1 = PAE Pass Portpap is 6'b11_1111.	
1	R/W	Slow Pass Portmap. 0 = SLOW Pass Portmap is 6'b00_0000. 1 = SLOW Pass Portpap is 6'b11_1111.	1'b0
0	R/W	BPDU Pass Portmap. 0 = BPDU Pass Portmap is 6'b00_0000. 1 = BPDU Pass Portpap is 6'b11_1111.	1'b1

4.2.51 New Reserve Address Control Register 1

offset: 0x3eh

Bits	Type	Description	Initial value
15	R/W	Mac Control Action for OPCODE = 8'h01. 0 = The same as Mac Control Action for OPCODE != 8'h01. 1 = Discard.	1'b0
14:13	R/W	Mac Control Action for OPCODE != 8'h01. 00 = Default Output Ports. 01 = Discard. 10 = If the receiving port is the CPU port, forward it to the default output ports. If the receiving port is not the CPU port, forward it to the CPU port. 11 = Forward to the default output ports except the CPU port.	2'b0
12	R/W	New Reserve Management for GXRP. 0 = Don't identify as management packets. 1 = Identify as management packets.	1'b0
11	R/W	New Reserve Management for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3. 0 = Don't identify as management packets. 1 = Identify as management packets.	1'b0
10	R/W	New Reserve Management for BPDU. 0 = Don't identify as management packets. 1 = Identify as management packets.	1'b0
9	R/W	New Reserve Span.for GXRP. 0 = Don't identify as management packets. 1 = Identify as management packets.	1'b0
8	R/W	New Reserve Span for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3. 0 = Don't identify as span packets. 1 = Identify as span packets.	1'b0
7	R/W	New Reserve SPAN for BPDU. 0 = Don't identify as span packets. 1 = Identify as span packets.	1'b0
6	R/W	New Reserve Cross_VLAN for GXRP. 0 = Follow VLAN 1 = Cross VLAN.	1'b0
5	R/W	New Reserve Cross_VLAN.for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3. 0 = Follow VLAN 1 = Cross VLAN.	1'b0
4	R/W	New Reserve Cross_VLAN for BPDU. 0 = Follow VLAN 1 = Cross VLAN.	1'b0
3:2	R/W	New Reserve TXTAG for GXRP. 00 = System Default Tag.	2'b0

Bits	Type	Description	Initial value
		01 = Unmodified. 10 = Always Tagged. 11 = Always Untagged.	
1:0	R/W	New Reserve TXTAG for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged. 11 = Always Untagged.	2'b0

4.2.52 Hardware IGMP Control Register

offset: 0x3fh

Bits	Type	Description	Initial value
15:8	R/W	Query Interval	8'h7c
7:6	R/W	Robust Variable.	2'h2
5:0	R/W	Default Router Portmap	6'h0

4.3 EEPROM Extended Register Map

Register	Bit 15- 0	Default Value
0x040h	VLAN Filter 0 Low	16'h003f
0x041h	VLAN Filter 0 High	16'h8001
0x042h	VLAN Filter 1 Low	16'h003f
0x043h	VLAN Filter 1 High	16'h8001
0x044h	VLAN Filter 2 Low	16'h003f
0x045h	VLAN Filter 2 High	16'h8001
0x046h	VLAN Filter 3 Low	16'h003f
0x047h	VLAN Filter 3 High	16'h8001
0x048h	VLAN Filter 4 Low	16'h003f
0x049h	VLAN Filter 4 High	16'h8001
0x04ah	VLAN Filter 5 Low	16'h003f
0x04bh	VLAN Filter 5 High	16'h8001
0x04ch	VLAN Filter 6 Low	16'h003f
0x04dh	VLAN Filter 6 High	16'h8001
0x04eh	VLAN Filter 7 Low	16'h003f
0x04fh	VLAN Filter 7 High	16'h8001
0x050h	VLAN Filter 8 Low	16'h003f
0x051h	VLAN Filter 8 High	16'h8001
0x052h	VLAN Filter 9 Low	16'h003f
0x053h	VLAN Filter 9 High	16'h8001
0x054h	VLAN Filter 10 Low	16'h003f
0x055h	VLAN Filter 10 High	16'h8001
0x056h	VLAN Filter 11 Low	16'h003f
0x057h	VLAN Filter 11 High	16'h8001
0x058h	VLAN Filter 12 Low	16'h003f
0x059h	VLAN Filter 12 High	16'h8001
0x05ah	VLAN Filter 13 Low	16'h003f
0x05bh	VLAN Filter 13 High	16'h8001
0x05ch	VLAN Filter 14 Low	16'h003f
0x05dh	VLAN Filter 14 High	16'h8001
0x05eh	VLAN Filter 15 Low	16'h003f

Register	Bit 15- 0		Default Value
0x05fh	VLAN Filter 15 High		16'h8001
0x060h	Type Filter 0		16'h0
0x061h	Type Filter 1		16'h0
0x062h	Type Filter 2		16'h0
0x063h	Type Filter 3		16'h0
0x064h	Type Filter 4		16'h0
0x065h	Type Filter 5		16'h0
0x066h	Type Filter 6		16'h0
0x067h	Type Filter 7		16'h0
0x068h	Protocol Filter 1	Protocol Filter 0	16'h0
0x069h	Protocol Filter 3	Protocol Filter 2	16'h0
0x06ah	Protocol Filter 5	Protocol Filter 4	16'h0
0x06bh	Protocol Filter 7	Protocol Filter 6	16'h0
0x06ch	Service Priority Mapping 0		16'b0
0x06dh	Service Priority Mapping 1		16'h0
0x06eh	Service Priority Mapping 2		16'h0
0x06fh	Service Priority Mapping 3		16'h0
0x070h	Service Priority Mapping 4		16'h0
0x071h	Service Priority Mapping 5		16'h0
0x072h	Service Priority Mapping 6		16'h0
0x073h	Service Priority Mapping 7		16'h0
0x074h	Reserve Action for 01-80-c2-00-00-01	Reserve Action for 01-80-c2-00-00-00	16'h0
0x075h	Reserve Action for 01-80-c2-00-00-03	Reserve Action for 01-80-c2-00-00-02	16'h0
0x076h	Reserve Action for 01-80-c2-00-00-05	Reserve Action for 01-80-c2-00-00-04	16'h0
0x077h	Reserve Action for 01-80-c2-00-00-07	Reserve Action for 01-80-c2-00-00-06	16'h0
0x078h	Reserve Action for 01-80-c2-00-00-09	Reserve Action for 01-80-c2-00-00-08	16'h0
0x079h	Reserve Action for 01-80-c2-00-00-0B	Reserve Action for 01-80-c2-00-00-0A	16'h0
0x07ah	Reserve Action for 01-80-c2-00-00-0D	Reserve Action for 01-80-c2-00-00-0C	16'h0
0x07bh	Reserve Action for 01-80-c2-00-00-0F	Reserve Action for 01-80-c2-00-00-0E	16'h0
0x07ch	Reserve Action for 01-80-c2-00-00-11	Reserve Action for 01-80-c2-00-00-10	16'h0
0x07dh	Reserve Action for 01-80-c2-00-00-13	Reserve Action for 01-80-c2-00-00-12	16'h0
0x07eh	Reserve Action for 01-80-c2-00-00-15	Reserve Action for 01-80-c2-00-00-14	16'h0
0x07fh	Reserve Action for 01-80-c2-00-00-17	Reserve Action for 01-80-c2-00-00-16	16'h0
0x080h	Reserve Action for 01-80-c2-00-00-19	Reserve Action for 01-80-c2-00-00-18	16'h0
0x081h	Reserve Action for 01-80-c2-00-00-1B	Reserve Action for 01-80-c2-00-00-1A	16'h0
0x082h	Reserve Action for 01-80-c2-00-00-1D	Reserve Action for 01-80-c2-00-00-1C	16'h0
0x083h	Reserve Action for 01-80-c2-00-00-1F	Reserve Action for 01-80-c2-00-00-1E	16'h0
0x084h	Reserve Action for 01-80-c2-00-00-21	Reserve Action for 01-80-c2-00-00-20	16'h0
0x085h	Reserve Action for 01-80-c2-00-00-23	Reserve Action for 01-80-c2-00-00-22	16'h0
0x086h	Reserve Action for 01-80-c2-00-00-25	Reserve Action for 01-80-c2-00-00-24	16'h0
0x087h	Reserve Action for 01-80-c2-00-00-27	Reserve Action for 01-80-c2-00-00-26	16'h0
0x088h	Reserve Action for 01-80-c2-00-00-29	Reserve Action for 01-80-c2-00-00-28	16'h0
0x089h	Reserve Action for 01-80-c2-00-00-2B	Reserve Action for 01-80-c2-00-00-2A	16'h0
0x08ah	Reserve Action for 01-80-c2-00-00-2D	Reserve Action for 01-80-c2-00-00-2C	16'h0
0x08bh	Reserve Action for 01-80-c2-00-00-2F	Reserve Action for 01-80-c2-00-00-2E	16'h0
0x08ch	TCP/UDP Filter Rule 0		16'h0
0x08dh	TCP/UDP Filter Rule 1		16'h0
0x08eh	TCP/UDP Filter Rule 2		16'h0
0x08fh	TCP/UDP Filter Rule 3		16'h0
0x090h	TCP/UDP Filter Rule 4		16'h0
0x091h	TCP/UDP Filter Rule 5		16'h0

Register	Bit 15- 0	Default Value
0x092h	TCP/UDP Filter Rule 6	16'h0
0x093h	TCP/UDP Filter Rule 7	16'h0
0x094h	Type Filter Action	16'h0
0x095h	Protocol Filter Action	16'h0
0x096h	TCP/UDP Action 0	16'h0
0x097h	TCP/UDP Action 1	16'h0
0x098h	TCP/UDP Action 2	16'h0
0x099h	Extended IGMP Control/Special Tag Insert Control	16'h01ff
0x09ah	Interrupt Enable Register	16'h0
0x09bh	Interrupt Status Register	16'h0
0x09ch	Security Control	16'h0

4.3.1 VLAN Filter 0 ~ 15 Low

offset: 0x0040h, 0x0042h, 0x0044h, 0x0046h, 0x0048h, 0x004ah 0x004ch, 0x004eh, 0x0050h, 0x0052h, 0x0054h, 0x0056h, 0x0058h, 0x005ah, 0x005ch, 0x005eh

Bits	Type	Description	Initial value
15:12	R/W	FID. The forwarding or learning group that the VID is assigned.	4'b0
11:6	R/W	Tagged Member. These bits indicate which ports associated with the VID should transmit tagged packets. Tagged Member[x] Description 1 = Port x should transmit tagged packets. 0 = Port x should transmit untagged packets.	6'b0
5:0	R/W	Member. These bits indicate which ports are the members of the VLAN. Member[x] Description 1 = Port x is a VLAN member. 0 = Port x is not a VLAN member.	6'b11_1111

4.3.2 VLAN Filter 0 ~ 15 High

offset: 0x0041h, 0x0043h, 0x0045h, 0x0047h, 0x0049h, 0x004bh 0x004dh, 0x004fh, 0x0051h, 0x0053h, 0x0055h, 0x0057h, 0x0059h, 0x005bh, 0x005dh, 0x005fh

Bits	Type	Description	Initial value
15	R/W	VLAN_Valid. 1 = VLAN Filter is valid. 0 = VLAN filter is not valid.	1'b1
14:12	R/W	VLAN PRI. It indicates the VLAN priority associated with VID.	3'b000
11:0	R/W	VID. It indicates the VLAN ID that is associated with FID, Tagged Member, Member and VLAN PRI.	12'b1

4.3.3 Type Filter 0 ~ 7

offset: 0x0060h ~ 0x0067h

Bits	Type	Description	Initial value
15:0	R/W	Value Compared with Ether-Type.	16'b0

4.3.4 Protocol Filter 0 ~ 7

offset: 0x0068h, 0x006bh

Bits	Type	Description	Initial value
15:8	R/W	Value Compared with Protocol in IP Header (Protocol Filter 1, 3, 5, 7)	8'b0
7:0	R/W	Value Compared with Protocol in IP Header (Protocol Filter 0, 2, 4, 6)	8'b0

4.3.5 Service Priority Mapping

offset: 0x006ch

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h7.	2'b0
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h6.	2'b0
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h5.	2'b0
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h4.	2'b0
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3.	2'b0
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2.	2'b0
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1.	2'b0
1:0	R/W	00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3. The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h0.	2'b0

4.3.6 Service Priority Mapping

offset: 0x006dh

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'hf.	2'b0
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'he.	2'b0
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'hd.	2'b0
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'hc.	2'b0
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'hb.	2'b0
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'ha.	2'b0
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h9.	2'b0
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h8.	2'b0

4.3.7 Service Priority Mapping

offset: 0x006eh

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h17.	2'b01
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h16.	2'b01
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h15.	2'b01
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the	2'b01

Bits	Type	Description	Initial value
		IPV4 TOS/IPV6 Traffic Class are 6'h14.	
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h13.	2'b01
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h12.	2'b01
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h11.	2'b01
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h10.	2'b01

4.3.8 Service Priority Mapping

offset: 0x006fh

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1f.	2'b01
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1e.	2'b01
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1d.	2'b01
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1c.	2'b01
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1b.	2'b01
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h1a.	2'b01
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h19.	2'b01
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h18.	2'b01

4.3.9 Service Priority Mapping

offset: 0x0070h

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h27.	2'b10
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h26.	2'b10
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h25.	2'b10
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h24.	2'b10
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h23.	2'b10
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h22.	2'b10
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h21.	2'b10
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h20.	2'b10

4.3.10 Service Priority Mapping

offset: 0x0071h

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2f.	2'b10
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2e.	2'b10
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2d.	2'b10
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2c.	2'b10
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2b.	2'b10
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h2a.	2'b10
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h29.	2'b10
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h28.	2'b10

4.3.11 Service Priority Mapping

offset: 0x0072h

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h37.	2'b11
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h36.	2'b11
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h35.	2'b11
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h34.	2'b11
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h33.	2'b11
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h32.	2'b11
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h31.	2'b11
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h30.	2'b11

4.3.12 Service Priority Mapping

offset: 0x0073h

Bits	Type	Description	Initial value
15:14	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3f.	2'b11
13:12	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3e.	2'b11
11:10	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3d.	2'b11
9:8	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3c.	2'b11

Bits	Type	Description	Initial value
7:6	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3b.	2'b11
5:4	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h3a.	2'b11
3:2	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h39.	2'b11
1:0	R/W	The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 6'h38.	2'b11

4.3.13 Reserve Action

offset: 0x0074h ~0x008bh

Bits	Type	Description	Initial value
15	R/W	Valid. 0 = Not Valid. 1 = Valid.	1'b0
14	R/W	Span. 0 = Don't identify as the span packet. 1 = Identify as the span packet.	1'b0
13	R/W	Management. 0 = Don't identify as the management packet. 1 = Identify as the management packet.	1'b0
12	R/W	Cross_VLAN. 0 = Don't identify as the cross_VLAN packet. 1 = Identify as the cross_VLAN packet.	1'b0
11:10	R/W	TXTAG. 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged. 11 = Always Untagged.	2'b0
9:8	R/W	Action. 00 = Portmap is 6'b11_1111. 01 = Portmap is 6'b0. 10 = Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Reserve Portmap contains all the ports, excluding the CPU port. 11 = Portmap contains all the ports, excluding the CPU port.	2'b0
7	R/W	Valid. 0 = Not Valid. 1 = Valid.	1'b0
6	R/W	Span. 0 = Don't identify as the span packet. 1 = Identify as the span packet.	1'b0
5	R/W	Management. 0 = Don't identify as the management packet. 1 = Identify as the management packet.	1'b0
4	R/W	Cross_VLAN. 0 = Don't identify as the cross_VLAN packet. 1 = Identify as the cross_VLAN packet.	1'b0
3:2	R/W	TXTAG. 00 = System Default Tag. 01 = Unmodified. 10 = Always Tagged.	2'b0

Bits	Type	Description	Initial value
		11 = Always Untagged.	
1:0	R/W	Action. 00 = Portmap is 6'b11_1111. 01 = Portmap is 6'b0. 10 = Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Reserve Portmap contains all the ports, excluding the CPU port. 11 = Portmap contains all the ports, excluding the CPU port	2'b0

4.3.14 TCP/UDP Filter 0 ~ 7

offset: 0x008ch, 0x0093h

Bits	Type	Description	Initial value
15:0	R/W	Value Compared with the Destination Port Number in the TCP/UDP Header	16'b0

4.3.15 Type Filter Action

offset: 0x0094h

Bits	Type	Description	Initial value
15:14	R/W	Action for Type Filter 7.	2'b0
13:12	R/W	Action for Type Filter 6.	2'b0
11:10	R/W	Action for Type Filter 5.	2'b0
9:8	R/W	Action for Type Filter 4.	2'b0
7:6	R/W	Action for Type Filter 3.	2'b0
5:4	R/W	Action for Type Filter 2.	2'b0
3:2	R/W	Action for Type Filter 1.	2'b0
1:0	R/W	Action for Type Filter 0. 00 = Type Portmap is Default Output Ports. 01 = Type Portmap is 6'b0. 10 = Type Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports, excluding the CPU port. 11 = Type Portmap contains Default Output Ports, excluding the CPU port.	2'b0

4.3.16 Protocol Filter Action

offset: 0x0095h

Bits	Type	Description	Initial value
15:14	R/W	Action for Protocol Filter 7.	2'b0
13:12	R/W	Action for Protocol Filter 6.	2'b0
11:10	R/W	Action for Protocol Filter 5.	2'b0
9:8	R/W	Action for Protocol Filter 4.	2'b0
7:6	R/W	Action for Protocol Filter 3.	2'b0
5:4	R/W	Action for Protocol Filter 2.	2'b0
3:2	R/W	Action for Protocol Filter 1.	2'b0
1:0	R/W	Action for Type Filter 0. 00 = Protocol Portmap is Default Output Ports. 01 = Protocol Portmap is 6'b0. 10 = Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports, excluding the CPU port. 11 = Protocol Portmap contains Default Output Ports, excluding the CPU port.	2'b0

4.3.17 TCP/UDP Action 0

offset: 0x0096h

Bits	Type	Description	Initial value
15:14	R/W	Action for TCP/UDP Filter 3.	2'b0
13:12	R/W	TCPUDP PRI for TCP/UDP Filter 3.	2'b0
11:10	R/W	Action for TCP/UDP Filter 2.	2'b0
9:8	R/W	TCPUDP PRI for TCP/UDP Filter 2.	2'b0
7:6	R/W	Action for TCP/UDP Filter 1.	2'b0
5:4	R/W	TCPUDP PRI for TCP/UDP Filter 1.	2'b0
3:2	R/W	Action for TCP/UDP Filter 0. 00 = Protocol Portmap is Default Output Ports. 01 = Protocol Portmap is 6'b0. 10 = Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports, excluding the CPU port. 11 = Protocol Portmap contains Default Output Ports, excluding the CPU port.	2'b0
1:0	R/W	TCPUDP PRI for TCP/UDP Filter 0. 00 = Queue 0. 01 = Queue 1. 10 = Queue 2. 11 = Queue 3	2'b0

4.3.18 TCP/UDP Action 1

offset: 0x0097h

Bits	Type	Description	Initial value
15:14	R/W	Action for TCP/UDP Filter 7.	2'b0
13:12	R/W	TCPUDP PRI for TCP/UDP Filter 7.	2'b0
11:10	R/W	Action for TCP/UDP Filter 6.	2'b0
9:8	R/W	TCPUDP PRI for TCP/UDP Filter 6.	2'b0
7:6	R/W	Action for TCP/UDP Filter 5.	2'b0
5:4	R/W	TCPUDP PRI for TCP/UDP Filter 5.	2'b0
3:2	R/W	Action for TCP/UDP Filter 4.	2'b0
1:0	R/W	TCPUDP PRI for TCP/UDP Filter 4.	2'b0

4.3.19 TCP/UDP Action 2

offset: 0x0098h

Bits	Type	Description	Initial value
15:14	R	Reserve.	2'b0
13:12	R/W	Compare TCP/UDP Source Port or Destination Port. 00 = Don't Compare 01 = Compare DA 10 = Compare SA 11 = Compare DA or SA	2'b0
11	R/W	Port 5 IP over TCP/UPD. 1 = Use IP field when packets contain both TCP/UDP and IP. 0 = Use TCP/UDP field when packets contain both TCP/UDP and IP.	1'b0
10	R/W	Port 4 IP over TCP/UPD 1 = Use IP field when packets contain both TCP/UDP and IP. 0 = Use TCP/UDP field when packets contain both TCP/UDP and IP.	1'b0
9	R/W	Port 3 IP over TCP/UPD. 1 = Use IP field when packets contain both TCP/UDP and IP.	1'b0

Bits	Type	Description	Initial value
		0 = Use TCP/UDP field when packets contain both TCP/UDP and IP.	
8	R/W	Port 2 IP over TCP/UPD. 1 = Use IP field when packets contain both TCP/UDP and IP. 0 = Use TCP/UDP field when packets contain both TCP/UDP and IP.	1'b0
7	R/W	Port 1 IP over TCP/UPD. 1 = Use IP field when packets contain both TCP/UDP and IP. 0 = Use TCP/UDP field when packets contain both TCP/UDP and IP.	1'b0
6	R/W	Port 0 IP over TCP/UPD . 1 = Use IP field when packets contain both TCP/UDP and IP. 0 = Use TCP/UDP field when packets contain both TCP/UDP and IP.	1'b0
5	R/W	Port 5 TCP/UDP PRIEN. 0 = Don't use TCP/UDP priority. 1 = Use TCP/UDP priority.	1'b0
4	R/W	Port 4 TCP/UDP PRIEN. 0 = Don't use TCP/UDP priority. 1 = Use TCP/UDP priority.	1'b0
3	R/W	Port 3 TCP/UDP PRIEN. 0 = Don't use TCP/UDP priority. 1 = Use TCP/UDP priority.	1'b0
2	R/W	Port 2 TCP/UDP PRIEN. 0 = Don't use TCP/UDP priority. 1 = Use TCP/UDP priority.	1'b0
1	R/W	Port 1 TCP/UDP PRIEN. 0 = Don't use TCP/UDP priority. 1 = Use TCP/UDP priority.	1'b0
0	R/W	Port 0 TCP/UDP PRIEN. 0 = Don't use TCP/UDP priority. 1 = Use TCP/UDP priority.	1'b0

4.3.20 Extended IGMP Control/Special Tag Insert Control

offset: 0x099h

Bits	Type	Description	Initial value
15	R/W	Reserved.	1'b0
14:13	R/W	Reserved.	2'b0
12	R/W	Reserved.	1'b0
11:10	R/W	Reserved.	2'b0
9	R/W	Include Address Change into Port Security Interrupt Source. 0 = Don't include. 1 = Include.	1'b0
8	R/W	Insert IP (don't in the TYPE/Protocol/TCPUDP). 0 = Don't insert. 1 = Insert.	1'b1
7	R/W	Insert Reserve. 0 = Don't insert. 1 = Insert.	1'b1
6	R/W	Insert ARP/RARP. 0 = Don't insert. 1 = Insert.	1'b1
5	R/W	Insert Snoop. 0 = Don't insert. 1 = Insert.	1'b1
4	R/W	Insert Type. 0 = Don't insert. 1 = Insert.	1'b1
3	R/W	Insert Protocol. 0 = Don't insert. 1 = Insert.	1'b1
2	R/W	Insert TCP/UDP. 0 = Don't insert. 1 = Insert.	1'b1
1	R/W	Insert Mac Control. 0 = Don't insert. 1 = Insert.	1'b1

Bits	Type	Description	Initial value
0	R/W	Insert Default. 0 = Don't insert. 1 = Insert.	1'b1

4.3.21 Interrupt Enable Register

offset: 0x09ah

Bits	Type	Description	Initial value
15:9	R	Reserve	7'b0
8	R/W	Leaning Table Access Done Interrupt Enable. 0 = Interrupt disable. 1 = Interrupt enable.	1'b0
7:2	R/W	Port Security Interrupt Enable. It's a per port setting. 0 = Interrupt disable. 1 = Interrupt enable.	6'b0
1	R/W	Counter Overflow Interrupt Enable. 0 = Interrupt disable. 1 = Interrupt enable.	1'b0
0	R/W	Port Status Interrupt Enable. 0 = Interrupt disable. 1 = Interrupt enable.	1'b0

4.3.22 Interrupt Status Register

offset: 0x09bh

Bits	Type	Description	Initial value
15:9	R	Reserve	8'b0
8	RC	Leaning Table Access Done. 0 = Access doesn't end. 1 = Access end.	RC
7:2	RC	Port Security Violation. It's a per port setting. 0 = Security didn't violate. 1 = Security violated.	RC
1	RC	Counter Overflow. 0 = Overflow didn't happen. 1 = Overflow happened for any of the counters.	RC
0	RC	Port Status Change. 0 = No status (link, speed, duplex, flow control) changed for any port. 1 = Status changed for any of 6 ports.	RC

4.3.23 Security Control Register (Reserved)

offset: 0x09ch

Bits	Type	Description	Initial value
15:13	R	Reserved.	3'h0
12	R/W	Reserved.	1'b0
11:6	R/W	Reserved.	6'b0
5:0	R/W	Reserved.	6'b0

4.4 Counter and Status Register Map

Register	Bit 15-0	Type	Register	Bit 15-0	Type
0xa0h	Chip Identifier 0	RO	0xf0h	Port 0 Collision Count Low	R/W
0xa1h	Chip Identifier 1	RO	0xf1h	Port 0 Collision Count High	R/W

Register	Bit 15-0	Type	Register	Bit 15-0	Type
0xa2h	Port Status 0	RO	0xf2h	Reserve	RO
0xa3h	Port Status 1	RO	0xf3h	Reserve	RO
0xa4h	Port Status 2	RO	0xf4h	Port 1 Collision Count Low	R/W
0xa5h	Port Status 3	RO	0xf5h	Port 1 Collision Count High	R/W
0xa6h	Reserve	RO	0xf6h	Reserve	RO
0xa7h	Reserve	RO	0xf7h	Reserve	RO
0xa8h	Port 0 Receive Packet Count Low	R/W	0xf8h	Port 2 Collision Count Low	R/W
0xa9h	Port 0 Receive Packet Count High	R/W	0xf9h	Port 2 Collision Count High	R/W
0xaah	Reserve	RO	0xfah	Reserve	RO
0xabh	Reserve	RO	0xfbh	Reserve	RO
0xach	Port 1 Receive Packet Count Low	R/W	0xfch	Port 3 Collision Count Low	R/W
0xadh	Port 1 Receive Packet Count High	R/W	0xfdh	Port 3 Collision Count High	R/W
0xaeh	Reserve	RO	0xfeh	Port 4 Collision Count Low	R/W
0xafh	Reserve	RO	0xffh	Port 4 Collision Count High	R/W
0xb0h	Port 2 Receive Packet Count Low	R/W	0x100h	Port 5 Collision Count Low	R/W
0xb1h	Port 2 Receive Packet Count High	R/W	0x101h	Port 5 Collision Count High	R/W
0xb2h	Reserve	RO	0x102h	Port 0 Error Count Low	R/W
0xb3h	Reserve	RO	0x103h	Port 0 Error Count High	R/W
0xb4h	Port 3 Receive Packet Count Low	R/W	0x104h	Reserve	RO
0xb5h	Port 3 Receive Packet Count High	R/W	0x105h	Reserve	RO
0xb6h	Port 4 Receive Packet Count Low	R/W	0x106h	Port 1 Error Count Low	R/W
0xb7h	Port 4 Receive Packet Count high	R/W	0x107h	Port 1 Error Count High	R/W
0xb8h	Port 5 Receive Packet Count Low	R/W	0x108h	Reserve	RO
0xb9h	Port 5 Receive Packet Count High	R/W	0x109h	Reserve	RO
0xbah	Port 0 Receive Packet Byte Count Low	R/W	0x10ah	Port 2 Error Count Low	R/W
0xbbh	Port 0 Receive Packet Byte Count High	R/W	0x10bh	Port 2 Error Count High	R/W
0xbch	Reserve	RO	0x10ch	Reserve	RO
0xbdh	Reserve	RO	0x10dh	Reserve	RO
0xbeh	Port 1 Receive Packet Byte Count Low	R/W	0x10eh	Port 3 Error Count Low	R/W
0xbfh	Port 1 Receive Packet Byte Count High	R/W	0x10fh	Port 3 Error Count high	R/W
0xc0h	Reserve	RO	0x110h	Port 4 Error Count Low	R/W
0xc1h	Reserve	RO	0x111h	Port 4 Error Count High	R/W
0xc2h	Port 2 Receive Packet Byte Count Low	R/W	0x112h	Port 5 Error Count Low	R/W
0xc3h	Port 2 Receive Packet Byte Count High	R/W	0x113h	Port 5 Error Count High	R/W
0xc4h	Reserve	RO	0x114h	Over Flow Flag 0 Low	RC
0xc5h	Reserve	RO	0x115h	Over Flow Flag 0 High	RC
0xc6h	Port 3 Receive Packet Byte Count Low	R/W	0x116h	Over Flow Flag 1 Low	RC
0xc7h	Port 3 Receive Packet Byte Count High	R/W	0x117h	Over Flow Flag 1 High	RC
0xc8h	Port 4 Receive Packet Byte Count Low	R/W	0x118h	Over Flow Flag 2 Low	RC
0xc9h	Port 4 Receive Packet Byte Count High	R/W	0x119h	Over Flow Flag 2 High	RC
0xcah	Port 5 Receive Packet Byte Count Low	R/W	0x11ah	Address Table Control Register 0	R/W
0xcbh	Port 5 Receive Packet Byte Count High	R/W	0x11bh	Address Table Control Register 1	R/W
0xcch	Port 0 Transmit Packet Count Low	R/W	0x11ch	Address Table Control Register 2	R/W
0xcdh	Port 0 Transmit Packet Count High	R/W	0x11dh	Address Table Control Register 3	R/W
0xceh	Reserve	RC	0x11eh	Address Table Control Register 4	R/W
0xcfh	Reserve	RC	0x11fh	Address Table Control Register 5	R/W
0xd0h	Port 1 Transmit Packet Count Low	R/W	0x120h	Address Table Status Register 0	RO
0xd1h	Port 1 Transmit Packet Count High	R/W	0x121h	Address Table Status Register 1	RO
0xd2h	Reserve	RO	0x122h	Address Table Status Register 2	RO
0xd3h	Reserve	RO	0x123h	Address Table Status Register 3	RO
0xd4h	Port 2 Transmit Packet Count Low	R/W	0x124h	Address Table Status Register 4	RO

Register	Bit 15-0	Type	Register	Bit 15-0	Type
0xd5h	Port 2 Transmit Packet Count High	R/W	0x125h	Address Table Status Register 5	RO
0xd6h	Reserve	RO	0x126h	Reserve	RO
0xd7h	Reserve	RO	0x127h	Reserve	RO
0xd8h	Port 3 Transmit Packet Count Low	R/W	0x128h	BM Status Register 0	RC
0xd9h	Port 3 Transmit Packet Count High	R/W	0x129h	BM Status Register 1	RC
0xdah	Port 4 Transmit Packet Count Low	R/W	0x12ah	BM Status Register 2	RC
0xdbh	Port 4 Transmit Packet Count High	R/W	0x12bh	BM Status Register 3	RC
0xdch	Port 5 Transmit Packet Count Low	R/W	0x12ch	BM Status Register 4	RC
0xddh	Port 5 Transmit Packet Count High	R/W	0x12dh	BM Status Register 5	RC
0xdeh	Port 0 Transmit Packet Byte Count Low	R/W	0x12eh	BM Status Register 6	RC
0xdfh	Port 0 Transmit Packet Byte Count High	R/W	0x12fh	BM Status Register 7	RC
0xe0h	Reserve	RO	0x130h	Hardware Setting Low	R
0xe1h	Reserve	RO	0x131h	Hardware Setting High	R
0xe2h	Port 1 Transmit Packet Byte Count Low	R/W	0x132h	Assign Address [15:0]	R/W
0xe3h	Port 1 Transmit Packet Byte Count High	R/W	0x133h	Assign Address [31:16]	R/W
0xe4h	Reserve	RO	0x134h	Assign Address [47:32]	R/W
0xe5h	Reserve	RO	0x135h	Port / Fid / Pause SA/ Monitor Assign	R/W
0xe6h	Port 2 Transmit Packet Byte Count Low	R/W	0x136h	Mirror Register 0	R/W
0xe7h	Port 2 Transmit Packet Byte Count High	R/W	0x137h	Mirror Register 1	R/W
0xe8h	Reserve	RO	0x138h	Security Violation Port	RC
0xe9h	Reserve	RO	0x139h	Security Status 0	R
0xeah	Port 3 Transmit Packet Byte Count Low	R/W	0x13ah	Security Status 1	R
0xebh	Port 3 Transmit Packet Byte Count High	R/W	0x13bh	First Lock Address Search	R/W
0xech	Port 4 Transmit Packet Byte Count Low	R/W	0x13ch	First Lock Address [15:0]	R
0xedh	Port 4 Transmit Packet Byte Count High	R/W	0x13dh	First Lock Address [31:16]	R
0xeeh	Port 5 Transmit Packet Byte Count Low	R/W	0x13eh	First Lock Address [47:32]	R
0xefh	Port 5 Transmit Packet Byte Count High	R/W	0x13fh	First Lock FID	R
			0x140h	Counter Control Low	R/W
			0x141h	Counter Control High	R/W
			0x142h	Counter Status Low	RO
			0x143h	Counter Status High	RO

4.4.1 Chip Identifier 0, offset: 0xa0h

Bits	Type	Description	Initial value
15:4	RO	Product Code[11:0]	0x102h
3:0	RO	Version Number	0x1h

4.4.2 Chip Identifier 1, offset: 0xa1h

Bits	Type	Description	Initial value
15:4	RO	Reserve	0x0h
3:0	RO	Product Code[15:12]	0x7h

4.4.3 Port Status 0, offset: 0xa2h

Bits	Type	Description	Initial value
15:12	RO	Reserve	1'b0
11	RO	Port 1 Flow Control Status 0 = Port 1 disables the Full Flow Control/Half Back Pressure Function. 1 = Port 1 enabled the Full Flow Control/Half Back Pressure Function.	Real Time
10	RO	Port 1 Duplex Status. 0 = Port 1 operates in the Half Duplex.	Real Time

Bits	Type	Description	Initial value
		1 = Port 1 operates in the Full Duplex.	
9	RO	Port 1 Speed Status:. 1 = Port 1 operates in the 100M. 0 = Port 1 operates in the 10M.	Real Time
8	RO	Port 1 Link Status: 0 = Port 1 links down. 1 = Port 1 links up.	Real Time
7:4	RO	Reserve	1'b0
3	RO	Port 0 Flow Control Status. 0 = Port 0 disables the Full Flow Control/Half Back Pressure Function. 1 = Port 0 enabled the Full Flow Control/Half Back Pressure Function.	Real Time
2	RO	Port 0 Duplex Status. 0 = Port 0 operates in the Half Duplex. 1 = Port 0 operates in the Full Duplex.	Real Time
1	RO	Port 0 Speed Status. 1 = Port 0 operates in the 100M. 0 = Port 0 operates in the 10M.	Real Time
0	RO	Port 0 Link Status. 0 = Port 0 links down. 1 = Port 0 links up.	Real Time

4.4.4 Port Status 1, offset: 0xa3h

Bits	Type	Description	Initial value
15	RO	Port 4 Flow Control Status. 0 = Port 4 disables the Full Flow Control/Half Back Pressure Function. 1 = Port 4 enabled the Full Flow Control/Half Back Pressure Function.	Real Time
14	RO	Port 4 Duplex Status. 0 = Port 4 operates in the Half Duplex. 1 = Port 4 operates in the Full Duplex.	Real Time
13	RO	Port 4 Speed Status. 1 = Port 4 operates in the 100M. 0 = Port 4 operates in the 10M.	Real Time
12	RO	Port 4 Link Status. 0 = Port 4 links down. 1 = Port 4 links up.	Real Time
11	RO	Port 3 Flow Control Status. 0 = Port 3 disables the Full Flow Control/Half Back Pressure Function. 1 = Port 3 enabled the Full Flow Control/Half Back Pressure Function.	Real Time
10	RO	Port 3 Duplex Status. 0 = Port 3 operates in the Half Duplex. 1 = Port 3 operates in the Full Duplex.	Real Time
9	RO	Port 3 Speed Status. 1 = Port 3 operates in the 100M. 0 = Port 3 operates in the 10M.	Real Time
8	RO	Port 3 Link Status. 0 = Port 3 links down. 1 = Port 3 links up.	Real Time
7:4	RO	Reserve	1'b0
3	RO	Port 2 Flow Control Status. 0 = Port 2 disables the Full Flow Control/Half Back Pressure Function. 1 = Port 2 enabled the Full Flow Control/Half Back Pressure Function.	Real Time
2	RO	Port 2 Duplex Status.	Real Time

Bits	Type	Description	Initial value
		0 = Port 2 operates in the Half Duplex. 1 = Port 2 operates in the Full Duplex.	
1	RO	Port 2 Speed Status. 1 = Port 2 operates in the 100M. 0 = Port 2 operates in the 10M.	Real Time
0	RO	Port 2 Link Status. 0 = Port 2 links down. 1 = Port 2 links up.	Real Time

4.4.5 Port Status 2, offset: 0xa4h

Bits	Type	Description	Initial value
15:5	RO	Reserve	1'b0
4	RO	Port 5 Flow Control Enable. 0 = Port 5 disables the Full Flow Control/Half Back Pressure Function. 1 = Port 5 enabled the Full Flow Control/Half Back Pressure Function.	Real Time
3	RO	Port 5 Duplex Status. 0 = Port 5 operates in the Half Duplex. 1 = Port 5 operates in the Full Duplex.	Real Time
2	RO	Reserve.	1'b0
1	RO	Port 5 Speed Status. 1 = Port 5 operates in the 100M. 0 = Port 5 operates in the 10M.	Real Time
0	RO	Port 5 Link Status. 0 = Port 5 links down. 1 = Port 5 links up.	Real Time

4.4.6 Port Status 3, offset: 0xa5h

Bits	Type	Description	Initial value
15:0	R	Reserve	16'b0

4.4.7 Reserved Register, offset: 0xa6h

Bits	Type	Description	Initial value
15:0	RO	Reserve.	16'b0

4.4.8 Reserved Register, offset: 0xa7h

Bits	Type	Description	Initial value
15:0	RO	Reserve	16'b0

4.4.9 Counter Low, offset: 0x0a8h ~ 0x113h

Bits	Type	Description	Initial value
15:0	RO	Counter[15:0]	16'b0

4.4.10 Counter High, offset: 0x0a8h ~ 0x113h

Bits	Type	Description	Initial value
15:0	RO	Counter[31:16]	16'b0

4.4.11 Over-Flow Flag 0, offset: 0x114h

Bits	Type	Description	Initial value

15	RC	Overflow of Port 3 Receive Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
14	RO	Reserved	1'b0
13	RC	Overflow of Port 2 Receive Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
12	RO	Reserved	1'b0
11	RC	Overflow of Port 1 Receive Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
10	RO	Reserved	1'b0
9	RC	Overflow of Port 0 Receive Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
8	RC	Overflow of Port 5 Receive Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
7	RC	Overflow of Port 4 Receive Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
6	RC	Overflow of Port 3 Receive Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
5	RO	Reserved	1'b0
4	RC	Overflow of Port 2 Receive Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
3	RO	Reserved	1'b0
2	RC	Overflow of Port 1 Receive Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
1	RO	Reserve	1'b0
0	RC	Overflow of Port 0 Receive Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0

4.4.12 Over-Flow Flag 1, offset: 0x115h

Bits	Type	Description	Initial value
15:2	RO	Reserve	14'b0
1	RC	Overflow of Port 5 Receive Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
0	RC	Overflow of Port 4 Receive Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0

4.4.13 Over-Flow Flag 2, offset: 0x116h

Bits	Type	Description	Initial value
15	RC	Overflow of Port 3 Transmit Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0

14	RO	Reserve	1'b0
13	RC	Overflow of Port 2 Transmit Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
12	RO	Reserve	1'b0
11	RC	Overflow of Port 1 Transmit Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
10	RO	Reserve	1'b0
9	RC	Overflow of Port 0 Transmit Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
8	RC	Overflow of Port 5 Transmit Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
7	RC	Overflow of Port 4 Transmit Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
6	RC	Overflow of Port 3 Transmit Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
5	RO	Reserve	1'b0
4	RC	Overflow of Port 2 Transmit Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
3	RO	Reserve	1'b0
2	RC	Overflow of Port 1 Transmit Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0
1	RO	Reserve	1'b0
0	RC	Overflow of Port 0 Transmit Packet Count 0 = Don't overflow. 1 = Overflow.	1'b0

4.4.14 Over-Flow Flag 3: Register 0x117h

Bits	Type	Description	Initial value
15:2	RO	Reserve	14'b0
1	RC	Overflow of Port 5 Transmit Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0
0	RC	Overflow of Port 4 Transmit Packet Byte Count 0 = Don't overflow. 1 = Overflow.	1'b0

4.4.15 Over-Flow Flag 4, offset: 0x118h

Bits	Type	Description	Initial value
15	RC	Overflow of Port 3 Error Count 0 = Don't overflow. 1 = Overflow.	1'b0
14	RO	Reserve	1'b0
13	RC	Overflow of Port 2 Error Count 0 = Don't overflow.	1'b0

		1 = Overflow.	
12	RO	Reserve	1'b0
11	RC	Overflow of Port 1 Error Count 0 = Don't overflow. 1 = Overflow.	1'b0
10	RO	Reserve	1'b0
9	RC	Overflow of Port 0 Error Count 0 = Don't overflow. 1 = Overflow.	1'b0
8	RC	Overflow of Port 5 Collision Count 0 = Don't overflow. 1 = Overflow.	1'b0
7	RC	Overflow of Port 4 Collision Count 0 = Don't overflow. 1 = Overflow.	1'b0
6	RC	Overflow of Port 3 Collision Count 0 = Don't overflow. 1 = Overflow.	1'b0
5	RO	Reserve	1'b0
4	RC	Overflow of Port 2 Collision Count 0 = Don't overflow. 1 = Overflow.	1'b0
3	RO	Reserve	1'b0
2	RC	Overflow of Port 1 Collision Count 0 = Don't overflow. 1 = Overflow.	1'b0
1	RO	Reserve	1'b0
0	RC	Overflow of Port 0 Collision Count 0 = Don't overflow. 1 = Overflow.	1'b0

4.4.16 Over-Flow Flag 5: Register 0x119h

Bits	Type	Description	Initial value
15:2	RO	Reserve	14'b0
1	RC	Overflow of Port 5 Error Count 0 = Don't overflow. 1 = Overflow.	1'b0
0	RC	Overflow of Port 4 Error Count 0 = Don't overflow. 1 = Overflow.	1'b0

4.4.17 Hardware Setting Low: Register 0x130h

Bits	Type	Description	Initial value
15	RO	Reserved	Power on Value
14	RO	Bond	Power on Value
13	RO	Disable DM8606BF function	Power on Value
12	RO	BPEN	Power on Value
11	RO	16/32 Bit Data Bus	Power on Value
10	RO	GPSI Mode	Power on Value
9	RO	RMII Mode	Power on Value
8:7	RO	Port 4 Interface Type	Power on Value
6	RO	Global Flow Control	Power on Value

5	RO	Port 4 Fiber Mode	Power on Value
4	RO	Dual Color	Power on Value
3:2	RO	Chip Address	Power on Value
1	RO	Auto-Crossover	Power on Value
0	RO	Auto-Negotiation	Power on Value

4.4.18 Hardware Setting High: Register 0x131h

Bits	Type	Description	Initial value
15:10	RO	Reserve	0x0h
9	RO	Learning Table Bist Result. 0 = Work. 1 = Don't Work.	1'b0
8	RO	Linklist Table Bist Result. (Linklist Table doesn't do bist test in normal mode) 0 = Work. 1 = Don't Work.	1'b1
7	RO	Control Table Bist Result. 0 = Work. 1 = Don't work.	1'b0
6	RO	Hardware IGMP Table Bist Result. 0 = Work. 1 = Don't work.	1'b0
5	RO	Data buffer Bist Result. 0 = Work. 1 = Don't work.	1'b0
4:3	RO	P5 Mode. 00 = GPSI 01 = RMII 10 = MII	Power on Value
2:1	RO	Reserved	Power on Value
0	RO	CFG	Power on Value

4.4.19 Assign Address [15:0]: Register 0x132h

Bits	Type	Description	Initial value
15:0	R/W	Assign Address [15:0]	0x0h

4.4.20 Assign Address [31:16]: Register 0x133h

Bits	Type	Description	Initial value
15:0	R/W	Assign Address [31:16]	0x0h

4.4.21 Assign Address [47:32]: Register 0x134h

Bits	Type	Description	Initial value
15:0	R/W	Assign Address [47:32]	0x0h

4.4.22 Assign Option Register: 0x135h

Bits	Type	Description	Initial value
15:10	R	Reserve	6'b0
9	R/W	Pause Address Change. It is useful only when assign address is used for PAUSE source address. 0 = All the ports use this assign address as the source address of the PAUSE commands. 1 = Port 0 uses {assign address[47:3], 3'b000} as the source address of the PAUSE commands.	1'b0

		Port 1 uses {assign address[47:3], 3'b001} as the source address of the PAUSE commands. Port 2 uses {assign address[47:3], 3'b010} as the source address of the PAUSE commands. Port 3 uses {assign address[47:3], 3'b011} as the source address of the PAUSE commands. Port 4 uses {assign address[47:3], 3'b100} as the source address of the PAUSE commands. Port 5 uses {assign address[47:3], 3'b101} as the source address of the PAUSE commands.	
8:7	R/W	Assign Address Option. 00 = Assign address is useless. 01 = Assign address is used for PAUSE source address. 10 = Assign address is used for assign lock address or the monitor address. 11 = Assign address is used for PAUSE source address.	2'b00
6:3	R/W	Assign Fid. It is used for assign lock FID.	4'b0
2:0	R/W	Assign Port. It is used for the port that the user wants to assign or for the monitor port.	3'b.

4.4.23 Mirror Register 0: 0x136h

Bits	Type	Description	Initial value
14:15	R/W	Port 3 Transmit Mirror Option.	2'b0
13:12	R/W	Port 3 Receive Mirror Option.	2'b0
11:10	R/W	Port 2 Transmit Mirror Option.	2'b0
9:8	R/W	Port 2 Receive Mirror Option.	2'b0
7:6	R/W	Port 1 Transmit Mirror Option.	2'b0
5:4	R/W	Port 1 Receive Mirror Option.	2'b0
3:2	R/W	Port 0 Transmit Mirror Option. 00 = Don't be mirrored. 01 = The traffic transmitted from Port 0 is mirrored. 10 = The traffic with DA = assign address transmitted from Port 0 is mirrored. 11 = The traffic with SA = assign address transmitted from Port 0 is mirrored.	2'b0
1:0	R/W	Port 0 Receive Mirror Option. 00 = Don't be mirrored. 01 = The traffic received on Port 0 is mirrored. 10 = The traffic with DA = assign address received on Port 0 is mirrored. 11 = The traffic with SA = assign address received on Port 0 is mirrored.	2'b0

4.4.24 Mirror Register 1: 0x137h

Bits	Type	Description	Initial value
15	R/W	Mirror Enable 0 = Disable. 1 = Enable.	1'b0
14	R/W	Mirror CRC Also 0 = Don't mirror. 1 = Mirror.	1'b0
13	R/W	Mirror RXER Also 0 = Don't mirror. 1 = Mirror.	1'b0
12	R/W	Mirror PAUSE Also 0 = Don't mirror. 1 = Mirror.	1'b0
11	R/W	Mirror Long Also	1'b0

		0 = Don't mirror. 1 = Mirror.	
10	R/W	Mirror Short Also 0 = Don't mirror. 1 = Mirror.	1'b0
9	R/W	Reserved.	1'b0
8	R/W	Enable Transmit Unmonitored Packet to the Mirror Port. 0 = Mirror port only mirrors the mirrored packets. 1 = Mirror port also receives packets that are not mirrored but their output ports also contain the mirror port.	1'b0
7:6	R/W	Port 5 Transmit Mirror Option	2'b0
5:4	R/W	Port 5 Receive Mirror Option	2'b0
3:2	R/W	Port 4 Transmit Mirror Option	2'b0
1:0	R/W	Port 4 Receive Mirror Option	2'b0

4.4.25 Security Violation Port: 0x138h

Bits	Type	Description	Initial value
15:12	R	Reserve	4'b0
11:6	RC	Port Source Intrusion. 0 = Source Intrusion didn't happen. 1 = Source Intrusion happened.	6'b0
5:0	R	Reserve	6'b0

4.4.26 Security Status 0: 0x139h

Bits	Type	Description	Initial value
15:12	R	Reserve	4'b0
11:6	R	First Lock. 0 = Port didn't lock the address. 1 = Port locked the address.	6'b0
5:0	R	Port Locked. 0 = Port didn't close. 1 = Port closed because of source violation.	6'b0

4.4.27 Security Status 1: 0x13ah

Bits	Type	Description	Initial value
15:6	R	Reserve	10'b0
5:0	R	Link Lock. 0 = Link Lock didn't happen. 1 = Link Lock happened.	6'b0

4.4.28 First Lock Address Search: 0x13bh

Bits	Type	Description	Initial value
15:3	R	Reserve	13'b0
2:0	R/W	First Lock Search Port. Users could write this register to get the lock address and the lock FID (returned in the 0x13c, 0x13d, 0x13e, 0x13f) associated with the port. 000 = Search the address and FID locked on the port 0. 001 = Search the address and FID locked on the port 1. 010 = Search the address and FID locked on the port 1. 011 = Search the address and FID locked on the port 1. 100 = Search the address and FID locked on the port 1.	3'b0

		101 = Search the address and FID locked on the port 1.	

4.4.29 First Lock Address [15:0]: 0x13ch

Bits	Type	Description	Initial value
15:0	R	First Lock Address [15:0]	16'h0

4.4.30 First Lock Address [31:16]: 0x13dh

Bits	Type	Description	Initial value
15:0	R	First Lock Address [31:16]	16'h0

4.4.31 First Lock Address [47:32]: 0x13eh

Bits	Type	Description	Initial value
15:0	R	First Lock Address [47:32]	16'h0

4.4.32 First Lock FID: 0x13fh

Bits	Type	Description	Initial value
15:4	R	Reserve	12'b0
3:0	R	First Lock FID	4'b0

4.4.33 Counter Control Low: Register 0x140h

Bits	Type	Description	Initial value
15:8	R	Reserve	8'b0
7	R/W	Busy/Access Start. 1 = The counter control is busy, or users should write 1'b1 into this bit to start the access when the engine is free. 0 = The counter control is free.	1'b0
6	R/W	0 = Indirect Read Counter 1 = Renew Port Counter	1'b0
5:0	R/W	Indirect Read Counter: It means the counter address. Renew Port Counter: It means the counters on each port to renew.	6'b0

4.4.34 Counter Control High: Register 0x141h

Bits	Type	Description	Initial value
15:0	R	Reserve	16'b0

4.4.35 Counter Status Low: Register 0x142h

Bits	Type	Description	Initial value
15:0	R	Counter [15:0]	16'b0

4.4.36 Counter Status High: Register 0x143h

Bits	Type	Description	Initial value
15:0	R	Counter [31:16]	16'b0

4.5 PHY Register Map

4.5.1 PHY Control Register of Port0 ~ 4

offset: 0x200, 0x220, 0x240, 0x260, 0x280

Bits	Type	Name	Description	Initial value
15	R/W, SC	RST	RESET 1 – PHY Reset 0 – Normal operation Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values The software reset process takes 25us to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.	0x0h
14	R/W	LPBK	Loop Back Enable 1 – Enable loopback mode 0 – Disable Loopback mode This bit controls the PHY loopback operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register	0x0h
13	R/W	SPEED_LSB	Speed Selection LSB 0.6, 0.13 0 0 10 Mbits/s 0 1 100 Mbits/s 1 0 1000 Mbits/s 1 1 Reserved Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). If it is fiber mode, 0.13 is always 1. Any write to this bit will have no effect.	0x1h
12	R/W	ANEN	Auto Negotiation Enable 1 – Enable auto negotiation process 0 – Disable Auto negotiation process This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the RECANEN pin detects a logic 1 input level in Twisted-Pair Mode. If it is set when fiber mode is configured, any write to this bit will be ignored.	0x1h
11	R/W	PDN	Power Down Enable 1 – Power Down 0 – Normal Operation Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the D7001 into power down mode. During the power down mode, TXP/TXN and all LED outputs are tri-stated and the MII interfaces are isolated.	0x0h
10	R/W	ISO	Isolate D7001 from Network 1 – Isolate PHY from MII 0 – Normal Operation Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the D7001 does not respond to TXD, TXEN and TXER inputs, and it presents a high impedence on its TXC, RXC, CRSDV, RXER, RXD, COL and CRS outputs.	0x0h
9	R/W, SC	ANEN_RST	Restart Auto Negotiation 1 – Restart Auto Negotiation Process 0 – Normal Operation	0x0h

Bits	Type	Name	Description	Initial value
			Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced.	
8	R/W	DPLX	Duplex Mode 1 – Full Duplex mode 0 – Half Duplex mode If auto negotiation is disabled, this bit determines the duplex mode for the link.	0x1h
7	R/W	COLTST	Collision Test 1 – Enable COL signal test 0 – Disable COL signal test When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN.	0x0h
6	RO	SPEED_MSB	Speed Selection MSB Set to 0 all the time indicate that the D7001 does not support 1000 Mbits/s function.	0x0h
5:0	RO	Reserved	Not Applicable	0x00h

4.5.2 PHY Status Register of Port0 ~ 4

offset : 0x201, 0x221, 0x241, 0x261, 0x281

Bits	Type	Name	Description	Initial value
15	RO	CAP_T4	100Base-T4 Capable Set to 0 all the time to indicate that the D7001 does not support 100Base-T4	0x0h
14	RO	CAP_TXF	100Base-X Full Duplex Capable Set to 1 all the time to indicate that the D7001 does support Full Duplex mode	0x1h
13	RO	CAP_TXH	100Base-X Half Duplex Capable Set to 1 all the time to indicate that the D7001 does support Half Duplex mode	0x1h
12	RO	CAP_TF	10M Full Duplex Capable TP : Set to 1 all the time to indicate that the D7001 does support 10M Full Duplex mode FX : Set to 0 all the time to indicate that the D7001 does not support 10M Full Duplex mode	0x1h 0x0h
11	RO	CAP_TH	10M Half Duplex Capable TP : Set to 1 all the time to indicate that the D7001 does support 10M Half Duplex mode FX : Set to 0 all the time to indicate that the D7001 does not support 10M Half Duplex mode	0x1h 0x0h
10	RO	CAP_T2	100Base-T2 Capable Set to 0 all the time to indicate that the D7001 does not support 100Base-T2	0x0h
9:7	RO	Reserved	Not Applicable	0x0h
6	RO	CAP_SUPR	MF Preamble Suppression Capable This bit is hardwired to 1 indicating that the D7001 accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification.	0x1h
5	RO	AN_COMP	Auto Negotiation Complete 1 – Auto Negotiation process completed 0 – Auto Negotiation process not completed	0x0h

Bits	Type	Name	Description	Initial value
			If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected.	
4	RO	REM_FLT	Remote Fault Detect 1 – Remote Fault detected 0 – Remote Fault not detected This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05h) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read.	0x0h
3	RO	CAP_ANEG	Auto Negotiation Ability 1 – Capable of auto negotiation 0 – Not capable of auto negotiation TP : This bit is set to 1 all the time, indicating that D7001 is capable of auto negotiation. FX : This bit is set to 0 all the time, indicating that D7001 is not capable of auto negotiation in Fiber Mode.	0x1h 0x0h
2	RO	LINK	Link Status 1 – Link is up 0 – Link is down This bit reflects the current state of the link –test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status	0x0h
1	RO	JAB	Jabber Detect 1 – Jabber condition detected 0 – Jabber condition not detected	0x0h
0	RO	EXTREG	Extended Capability 1 – Extended register set 0 – No extended register set This bit defaults to 1, indicating that the D7001 implements extended registers.	0x0h

4.5.3 PHY Identifier Register of Port0 ~ 4

offset : 0x202, 0x222, 0x242, 0x262, 0x282

Bits	Type	Name	Description	Initial value
15:0	RO	PHY-ID[15:0]	IEEE Address	0x0302h

4.5.4 PHY Identifier Register of Port0 ~ 4

offset : 0x203, 0x223, 0x243, 0x263, 0x283

Bits	Type	Name	Description	Initial value
15:10	RO	PHY-ID[5:0]	IEEE Address	0x18h
9:4	RO	Model-ID[5:0]	IEEE Model No.	0x07h
3:0	RO	REV-ID[3:0]	IEEE Revision No.	0x01h

Note: Register 3 = 0xCC10

4.5.5 Auto Negotiation Advertisement Register of Port0 ~ 4

offset : 0x204, 0x224, 0x244, 0x264, 0x284

Bits	Type	Name	Description	Initial value
15	RO	NP	Next Page This bit is defaults to 1, indicating that D7001 is next page capable.	0x0h

Bits	Type	Name	Description	Initial value
14	R/W	Reserved	Not Applicable	0x0h
13	RO	RF	Remote Fault 1 – Remote Fault has been detected 0 – No remote fault has been detected This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner.	0x0h
12	RO	Reserved	Not Applicable	0x0h
11	R/W	ASM_DIR	Asymmetric Pause Direction. Bit[11:10] Capability 00 No Pause 01 Symmetric PAUSE 10 Asymmetric PAUSE toward Link Partner 11 Both Symmetric PAUSE and Asymmetric PAUSE toward local device	0x0h
10	R/W	PAUSE	Pause Operation for Full Duplex Value on PAUREC will be stored in this bit during power on reset.	0x1h
9	RO	T4	Technology Ability for 100Base-T4 Defaults to 0.	0x0h
8	R/W	TX_FDX	100Base-TX Full Duplex 1 – Capable of 100M Full duplex operation 0 – Not capable of 100M Full duplex operation	0x1h
7	R/W	TX_HDX	100Base-TX Half Duplex 1 – Capable of 100M operation 0 – Not capable of 100M operation	0x1h
6	R/W	10_FDX	10BASE-T Full Duplex 1 – Capable of 10M Full Duplex operation 0 – Not capable of 10M full duplex operation	0x1h
5	R/W	10_HDX	10Base-T Half Duplex 1 – Capable of 10M operation 0 – Not capable of 10M operation Note that bit 8:5 should be combined with REC100, RECFUL pin input to determine the finalized speed and duplex mode.	0x1h
4:0	RO	Selector Field	These 5 bits are hardwired to 00001b, indicating that the D7001 supports IEEE 802.3 CSMA/CD.	0x1h

4.5.6 Auto Negotiation Link Partner Ability Register of Port0 ~ 4

offset : 0x205, 0x225, 0x245, 0x265, 0x285

Bits	Type	Name	Description	Initial value
15	RO	NPAGE	Next Page 1 – Capable of next page function 0 – Not capable of next page function	0x0h
14	RO	ACK	Acknowledge 1 – Link Partner acknowledges reception of the ability data word 0 – Not acknowledged	0x0h
13	RO	RF	Remote Fault 1 – Remote Fault has been detected 0 – No remote fault has been detected	0x0h
12	RO	Reserved	Not Applicable	0x0h
11	RO	LP_DIR	Link Partner Asymmetric Pause Direction.	0x0h
10	RO	LP_PAU	Link Partner Pause Capability Value on PAUREC will be stored in this bit during power on reset.	0x0h

Bits	Type	Name	Description	Initial value
9	RO	LP_T4	Link Partner Technology Ability for 100Base-T4 Defaults to 0.	0x0h
8	RO	LP_FDX	100Base-TX Full Duplex 1 – Capable of 100M Full duplex operation 0 – Not capable of 100M Full duplex operation	0x0h
7	RO	LP_HDX	100Base-TX Half Duplex 1 – Capable of 100M operation 0 – Not capable of 100M operation	0x0h
6	RO	LP_F10	10BASE-T Full Duplex 1 – Capable of 10M Full Duplex operation 0 – Not capable of 10M full duplex operation	0x0h
5	RO	LP_H10	10Base-T Half Duplex 1 – Capable of 10M operation 0 – Not capable of 10M operation	0x0h
4:0	RO	Selector Field	Encoding Definitions.	0x01h

4.5.7 Auto Negotiation Expansion Register of Port0 ~ 4

offset : 0x206, 0x226, 0x246, 0x266, 0x286

Bits	Type	Name	Description	Initial value
15:5	RO	Reserved	Not Applicable	0x000h
4	RO, LH	PFAULT	Parallel Detection Fault 1 – Fault has been detected 0 – No Fault Detect	0x0h
3	RO	LPNPABLE	Link Partner Next Page Able 1 – Link Partner is next page capable 0 – Link Partner is not next page capable	0x0h
2	RO	NPABLE	Next Page Able Defaults to 1, indicating D7001 is next page able.	0x1h
1	RO	PGRCV	Page Received 1 – A new page has been received 0 – No new page has been received	0x0h
0	RO	LPANABLE	Link Partner Auto Negotiation Able 1 – Link Partner is auto negotiable 0 – Link Partner is not auto negotiable	0x0h

4.5.8 Next Page Transmit Register of Port0 ~ 4

offset : 0x207, 0x227, 0x247, 0x267, 0x287

Bits	Type	Name	Description	Initial value
15	RO	TNPAGE	Transmit Next Page Transmit Code Word Bit 15	0x0h
14	RO	Reserved	Reserved Transmit Code Word Bit 14	0x0h
13	R/W	TMSG	Transmit Message Page Transmit Code Word Bit 13	0x1h
12	R/W	TACK2	Transmit Acknowledge 2 Transmit Code Word Bit 12	0x0h
11	RO	TTOG	Transmit Toggle Transmit Code Word Bit 11	0x0h
10:0	R/W	TFLD[10:0]	Transmit Message Field Transmit Code Word Bit 10..0	0x001h

4.5.9 Link Partner Next Page Register of Port0 ~ 4

offset : 0x208, 0x228, 0x248, 0x268, 0x288

Bits	Type	Name	Description	Initial value
15	RO	PNPAGE	Link Partner Next Page Receive Code Word Bit 15	0x0h
14	RO	PACK	Link Partner Acknowledge Receive Code Word Bit 14	0x0h
13	RO	PMSGP	Link Partner Message Page Receive Code Word Bit 13	0x0h
12	RO	PACK2	Link Partner Acknowledge 2 Receive Code Word Bit 12	0x0h
11	RO	PTOG	Link Partner Toggle Receive Code Word Bit 11	0x0h
10:0	RO	PFLD[10:0]	Link Partner Message Field Receive Code Word Bit 11	0x001h

Chapter 5 Electrical Specification

5.1 TX/FX Interface

5.1.1 TP Interface

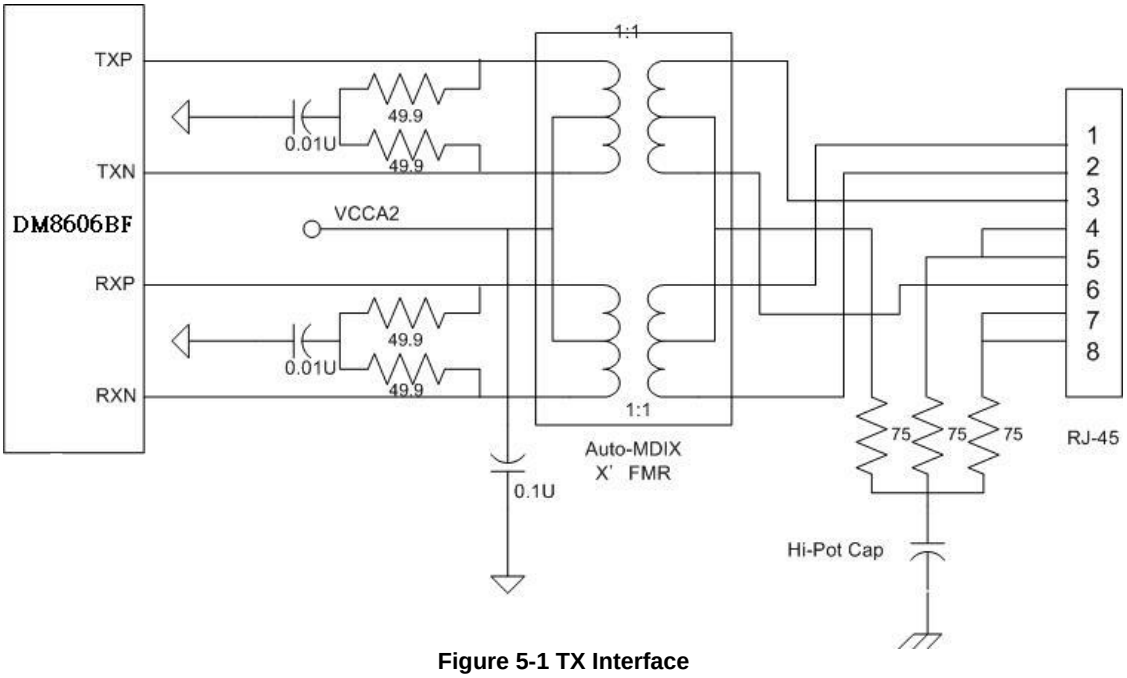


Figure 5-1 TX Interface

Transformer requirement:
. TX/RX rate 1:1
. TX/RX central tap connect together to VCCA2.
User can change TX/RX pin for easy layout but do not change polarity. DM8606BF supports auto polarity on receiving side.

5.1.2 FX Interface

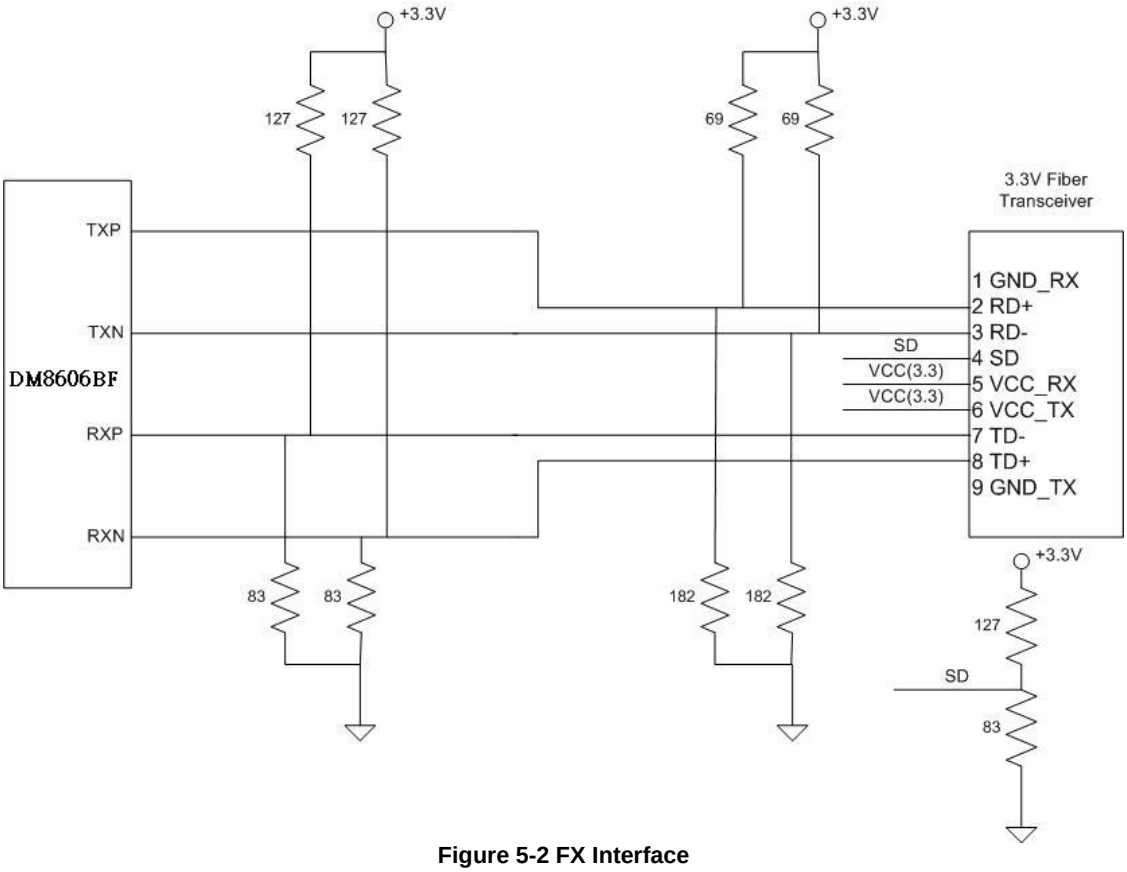


Figure 5-2 FX Interface

5.2 DC Characteristics

5.2.1 Power Consumption

(Under EEPROM Register 0x29 = 0xC000, and 0x30 = 0x0985)

Symbol	Parameter	Rating	Units
P_{100M_5TP}	Power consumption when all twisted pair ports are linked at 100Mbps.	930	mW
P_{10M_5TP}	Power consumption when all twisted pair ports are linked at 10Mbps (include transformer).	1270	mW
P_{DIS_5TP}	Power consumption when all twisted pair ports are disconnected.	450	mW

Table 5-1 Power Consumption

5.2.2 Absolute Maximum Rating

Symbol	Parameter	Rating	Units
V_{CC3O}	3.3V Power Supply for I/O pad	2.97 to 3.63	V
V_{CCBIAS}	3.3V Power Supply for bias circuit	2.97 to 3.63	V
V_{CCAD}	3.3V Power Supply for A/D converter	2.97 to 3.63	V
V_{CCA2}	1.8V Power Supply for line driver	1.62 to 1.98	V
V_{CCPLL}	1.8V Power Supply for PLL	1.62 to 1.98	V
V_{CCIK}	1.8V Power Supply for Digital core	1.62 to 1.98	V
V_{IN}	Input Voltage	-0.3 to V_{CC3O} + 0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC3O} + 0.3	V
$I_{3.3VMAX}$	Maximum current for 3.3V power supply	100	mA
$I_{1.8MAX}$	Maximum current for 1.8V power supply (include transformer)	750	mA
T_{STG}	Storage Temperature	-55 to 155	°C
ESD	ESD Rating	1.5	KV

Table 5-2 Electrical Absolute Maximum Rating

5.2.3 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units
V_{CC3O}	3.3V Power Supply for I/O pad	3.135	3.3	3.465	V
V_{CCBIAS}	3.3V Power Supply for bias circuit	3.135	3.3	3.465	V
V_{CCAD}	3.3V Power Supply for A/D converter	3.135	3.3	3.465	V
V_{CCA2}	1.8V Power Supply for line driver	1.71	1.8	1.89	V
V_{CCPLL}	1.8V Power Supply for PLL	1.71	1.8	1.89	V
V_{CCIK}	1.8V Power Supply for Digital core	1.71	1.8	1.89	V
V_{IN}	Input Voltage	0	-	V_{CC3O}	V
T_J	Junction Operating Temperature	0	25	115	°C

Table 5-3 Recommended Operating Conditions

5.2.4 DC Electrical Characteristics for 3.3V Operation

(Under V_{CC3O}=2.97V ~ 3.63V, T_J= 0°C ~ 115°C)

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IH}	Input High Voltage	TTL	2.0			V
V_{OL}	Output Low Voltage	TTL			0.4	V
V_{OH}	Output High Voltage	TTL	2.4			V
R_I	Input Pull_up/down Resistance	V_{IL}= 0V or $V_{IH} = V_{CC3O}$		50		KΩ

Table 5-4 DC Electrical Characteristics for 3.3V Operation

5.3 AC Characteristics

5.3.1 XTAL/OSC Timing

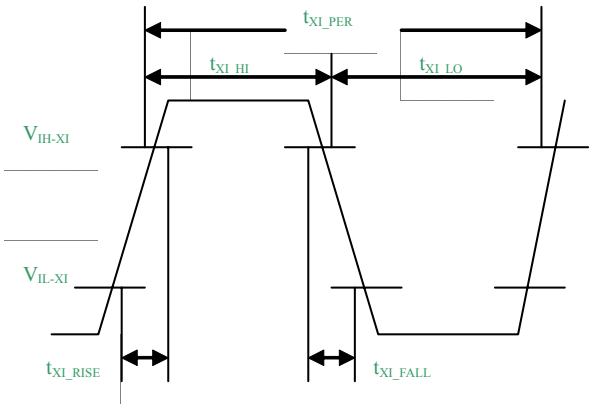


Figure 5-3 XTAL/OSC Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_XI_PER	XI/OSCI Clock Period		40.0 – 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High		14	20.0		ns
T_XI_LO	XI/OSCI Clock Low		14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time , V_{IL} (max) to V_{IH} (min)				4	ns
T_XI_FALL	XI/OSCI Clock Fall Time , V_{IH} (min) to V_{IL} (max)				4	ns

Table 5-5 XTAL/OSC Timing

5.3.2 Power On Reset

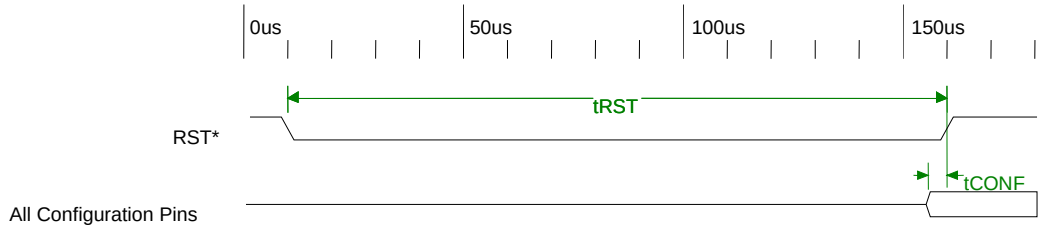


Figure 5-4 Power On Reset Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tRST	RST Low Period		100			ms
tCONF	Start of Idle Pulse Width		100			ns

Table 5-6 Power on reset timing

5.3.3 EEPROM Interface Timing

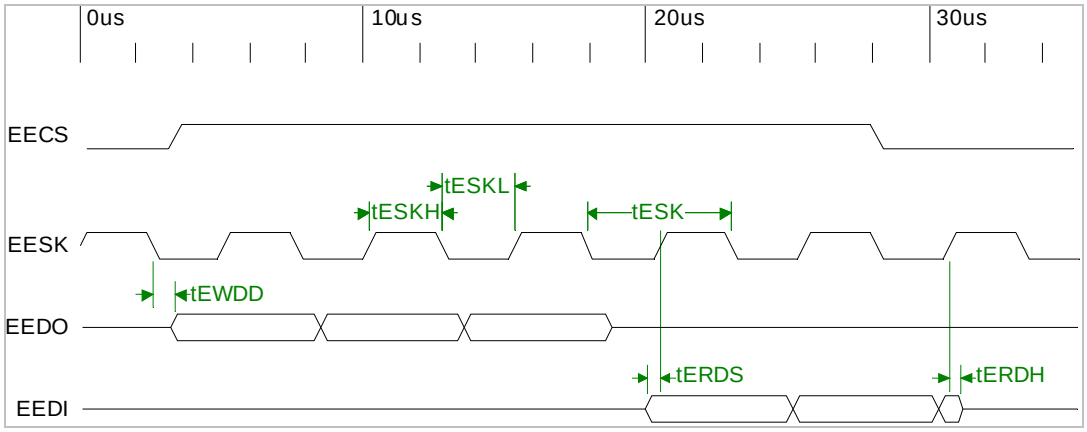


Figure 5-5 EEPROM Interface Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tESK	EESK Period			5120		ns
tESKL	EESK Low Period		2550		2570	ns
tESKH	EESK High Period		2550		2570	ns
tERDS	EEDI to EESK Rising Setup Time		10			ns
tERDH	EEDI to EESK Rising Hold Time		10			ns
tEWDD	EESK Falling to EEDO Output Delay Time				20	ns

Table 5-7 EEPROM Interface Timing

5.3.4 10Base-TX MII Input Timing

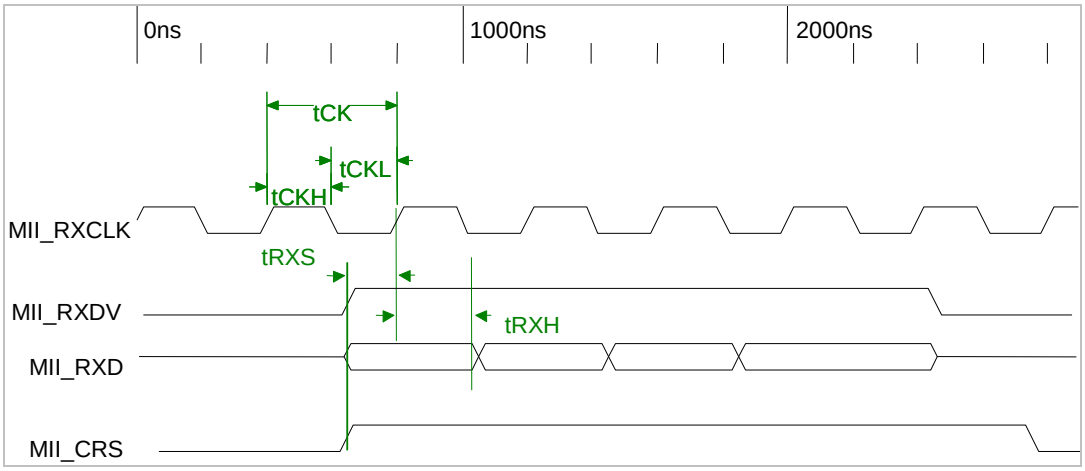


Figure 5-6 10Base-TX MII Input Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_RXCLK Period			400		ns
tCKL	MII_RXCLK Low Period		180		220	ns
tCKH	MII_RXCLK High Period		180		220	ns
tRXS	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup		10			ns
tRXH	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold		10			ns

Table 5-8 10Base-TX MII Input Timing

5.3.5 10Base-TX MII Output Timing

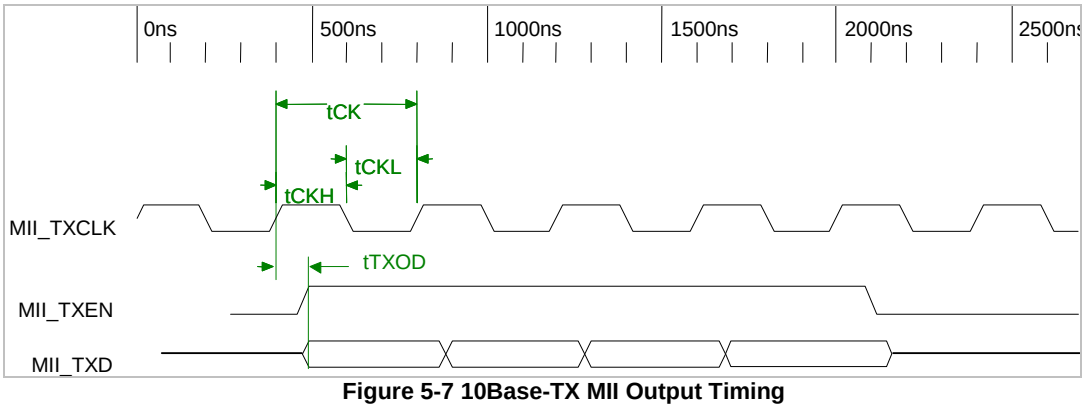


Figure 5-7 10Base-TX MII Output Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_TXCLK Period			400		ns
tCKL	MII_TXCLK Low Period		180		220	ns
tCKH	MII_TXCLK High Period		180		220	ns
tTXOD	MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay		0		25	ns

Table 5-9 10Base-TX MII Output Timing

5.3.6 100Base-TX MII Input Timing

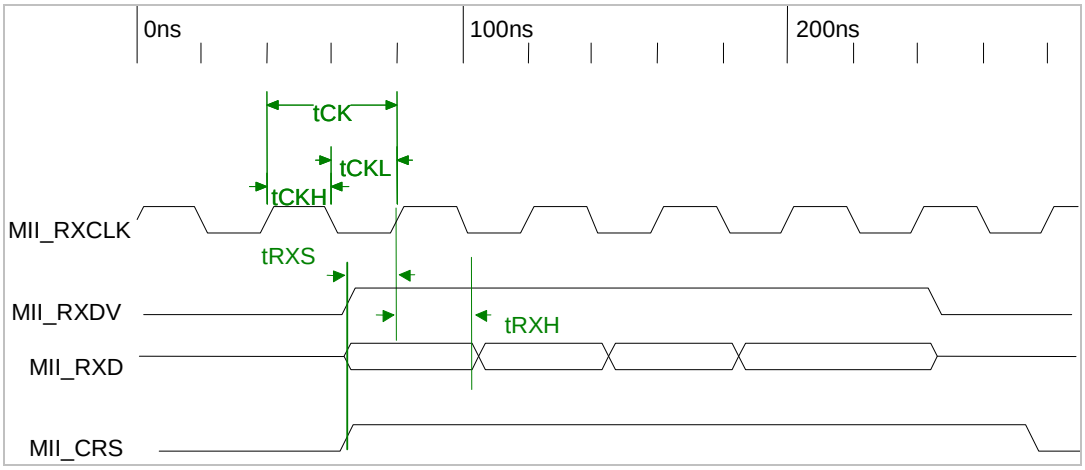


Figure 5-8 100Base-TX MII Input Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_RXCLK Period			40		ns
tCKL	MII_RXCLK Low Period		18		22	ns
tCKH	MII_RXCLK High Period		18		22	ns
tRXS	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup		10			ns
tRXH	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold		10			ns

Table 5-10 100Base-TX MII Input Timing

5.3.7 100Base-TX MII Output Timing

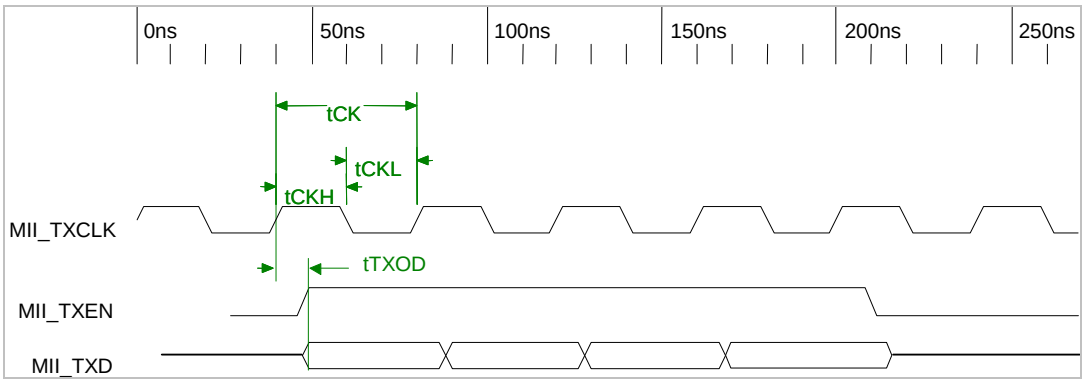


Figure 5-9 100Base-TX MII Output Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_TXCLK Period			40		ns
tCKL	MII_TXCLK Low Period		18		22	ns
tCKH	MII_TXCLK High Period		18		22	ns
tTXOD	MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay		0		25	ns

Table 5-11 100Base-TX MII Output Timing

5.3.8 GPSI (7-wire) Input Timing

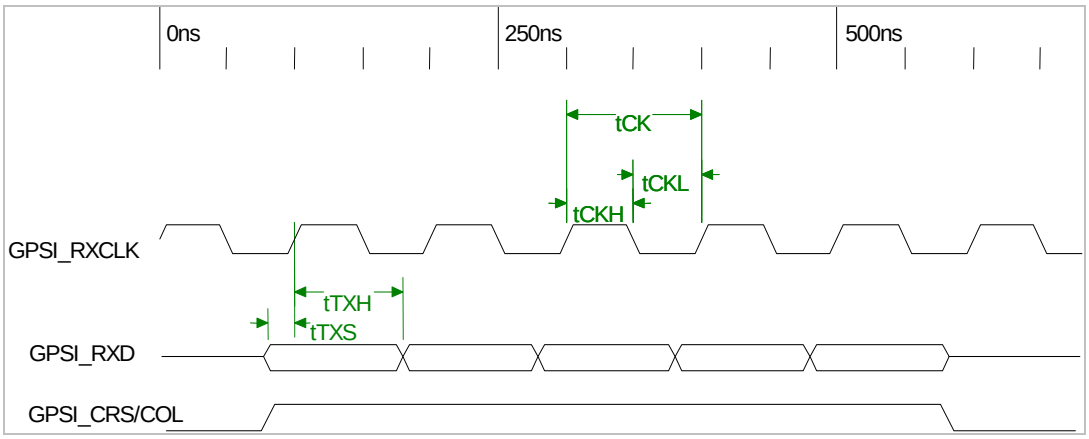


Figure 5-10 GPSI (7-wire) Input Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
TCK	GPSI_RXCLK Period			100		ns
TCKL	GPSI_RXCLK Low Period		40		60	ns
TCKH	GPSI_RXCLK High Period		40		60	ns
TTXS	GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising Setup Time		10			ns
TTXH	GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising Hold Time		10			ns

Table 5-12 GPSI (7-wire) Input Timing

5.3.9 GPSI (7-wire) Output Timing

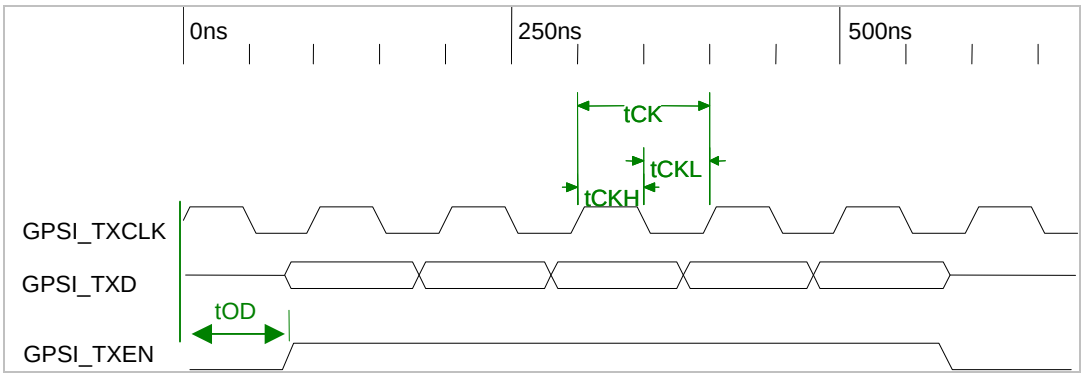


Figure 5-11 GPSI (7-wire) Output Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
TCK	GPSI_TXCLK Period			100		ns
TCKL	GPSI_TXCLK Low Period		40		60	ns
TCKH	GPSI_TXCLK High Period		40		60	ns
TOD	GPSI_TXCLK Rising to GPSI_TXEN/GPSI_TXD Output Delay		50		70	ns

Table 5-13 GPSI (7-wire) Output Timing

5.3.10 SDC/SDIO Timing

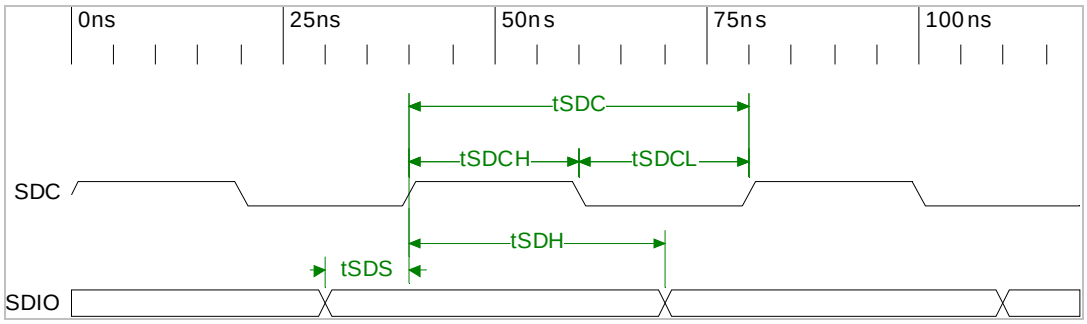


Figure 5-12 SDC/SDIO Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	SDC Period		20			ns
TCKL	SDC Low Period		10			ns
TCKH	SDC High Period		10			ns
TSDS	SDIO to SDC rising setup time on read/write cycle		4			ns
TSDH	SDIO to SDC rising hold time on read/write cycle		2			ns

Table 5-14 SDC/SDIO Timing

5.3.11 MDC/MDIO Timing

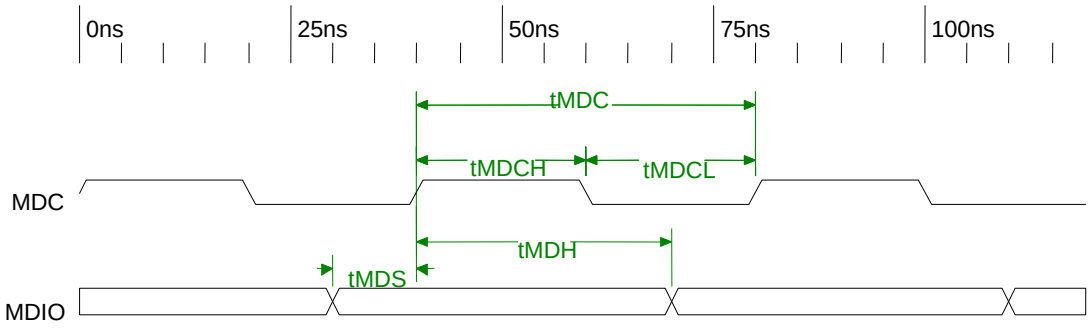


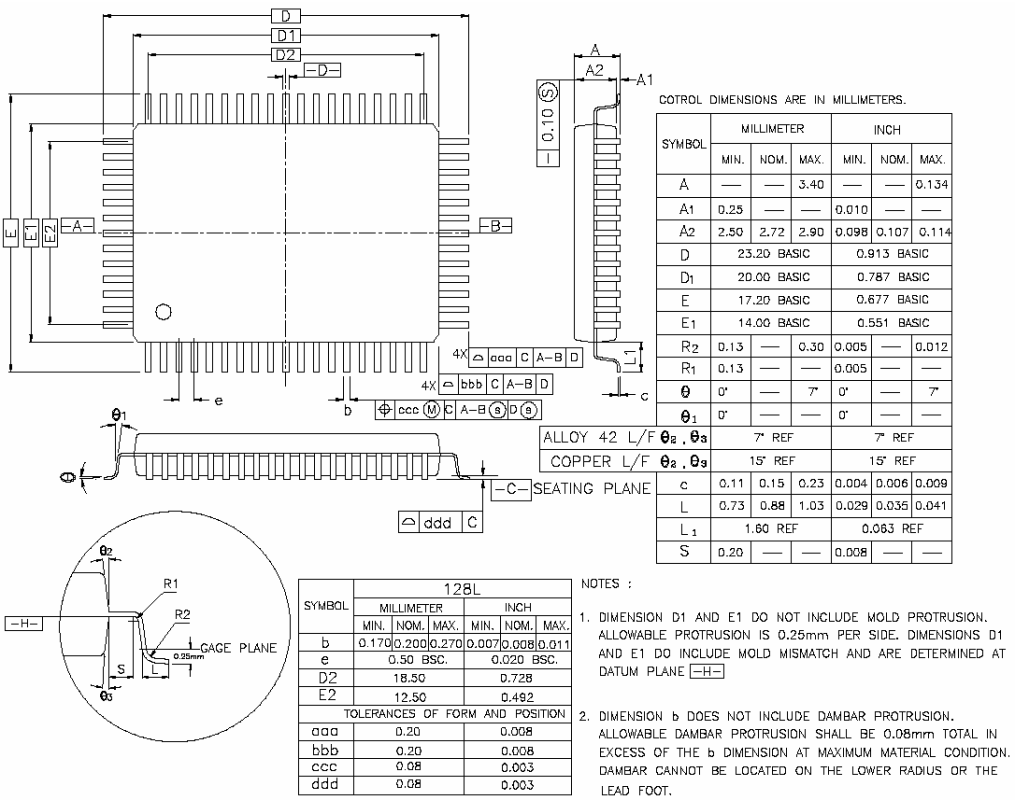
Figure 5-13 MDC/MDIO Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tMDC	MDC Period		100			ns
tMDCL	MDC Low Period		40			ns
tMDCH	MDC High Period		40			ns
TMDS	MDIO to MDC rising setup time on read/write cycle				10	ns
TMDH	MDIO to MDC rising hold time on read/write cycle		10			ns

Table 5-15 MDC/MDIO Timing

Chapter 6 Packaging and Ordering

128 Pin QFP Outside Dimension



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2, θ3	7° REF			7° REF		
COPPER L/F θ2, θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

Figure 6-6-1 128 Pin QFP Outside Dimension

Ordering Information

Part Number	Pin Count	Package
DM8606BF	128	QFP

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DAVICOM Semiconductor, Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.