DAVICOM Semiconductor, Inc.

DM8606C/DM8606CI

6-Port 10/100Mb Fast Ethernet Smart Switch

DATA SHEET

Final

Version: DM8606C/DM8606CI-12-M3-DS-F01

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CONTENT

1 General Description

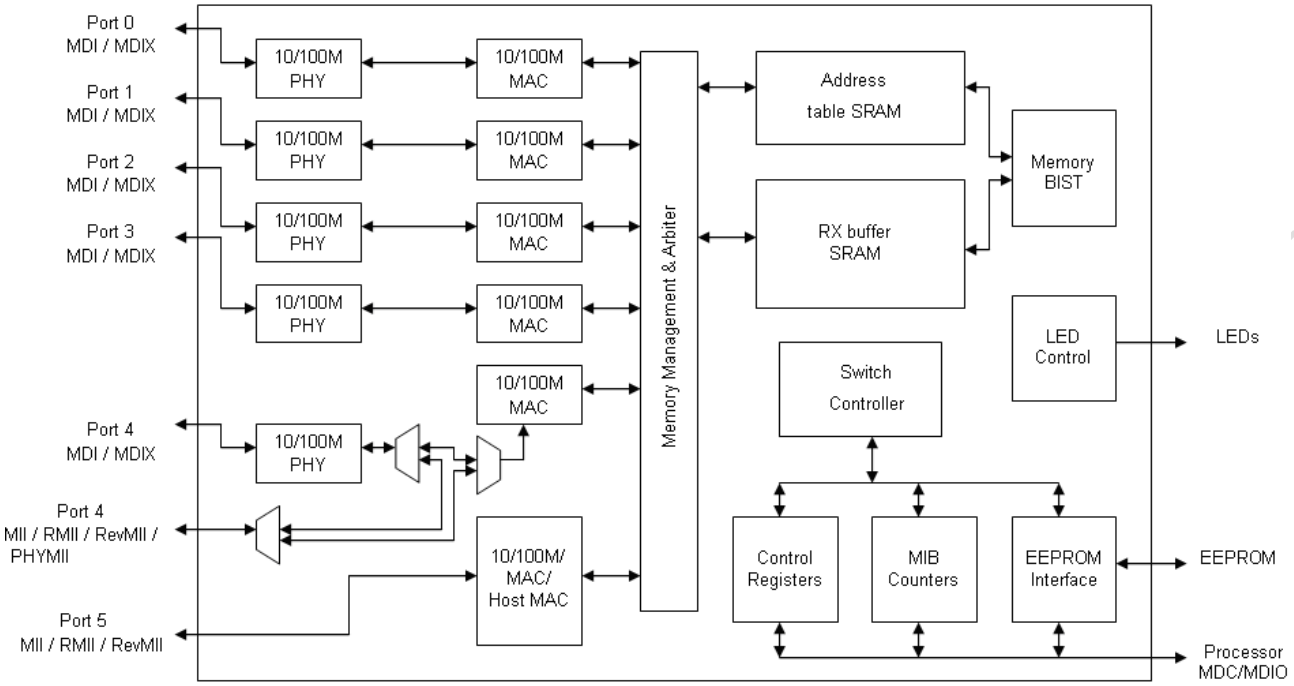
The embedded DM8606C/DM8606CI is a industrial-temperature (DM8606CI only) high performance and cost-effective 6-port 10/100Mbps Fast Ethernet smart switch. The smart switch incorporates five internal 10/100Mbps Ethernet PHY/ two media-independent interface (MII/RMII/RevMII/PHYMII) accesses with six 10/100Mbps MAC.

The DM8606C/DM8606CI management features include IEEE 802.1q VLAN, IEEE 802.1p Class of Service (CoS), Uni/Multi-cast MAC addresses, and IPv4 TOS. The five PHYs are all fully compliant with IEEE 802.3 10BASE-T Ethernet, IEEE802.3u 100BASE-TX Fast Ethernet, and IEEE802.3x Flow Control. EEPROM interface is used for convenient of registers default configurations.

2 Features

- **IEEE 802.3 10BASE-T/ IEEE 802.3u 100BASE-TX compatible**
- **Ethernet Switch Ports**
  - Five 10/100Mb PHY built-in, that can be used for Copper or Fiber application
  - Port 4 support MII/RMII/RevMII interface to MAC or MII interface to internal PHY
  - Port 5 support MII/RMII/RevMII interface to MAC
- **Each internal PHY supports HP Auto-MDIX**
- **Support bandwidth, ingress and egress rate control on a per MAC port basis**
- **Priority transmit queues for QoS is supported per each MAC port:**
  - Each port have four queues with strict or weight ratio priority schemes
  - IEEE 802.1p VLAN, Port based, MAC based, IPv4 TOS, Special Tag
- **Per port support broadcast storming filter function for broadcast, multicast – and unknown unicast packets**
- **Flow Control:**
  - Supports IEEE 802.3x Flow Control in full-duplex mode
  - Supports Back Pressure Flow Control in half-duplex mode
- **Support special Tag to communication with CPU**
- **Record up to 2K Uni/Multi-cast MAC addresses**
- **IEEE 802.1Q VLAN up-to 16 VLAN groups**
  - Full 12-bit VID, 4-bit FID, Tag/untag,
  - Support SVL/IVL
- **Support hardware IGMP snooping v1/v2 and MLD v1**
- **Support STP/RSTP**
- **Support automatic aging scheme**
- **Support trunk ports**
- **Support EEPROM interface for power up configurations**
- **Support serial data management interface and MIB counter for diagnostic**
- **Supports industrial-temperature (-40℃ ~ +85℃)**
- **128 pin QFP package**
- **0.18um CMOS Technology**
- **Power Input: 1.8V and 3.3V**
- **3.3V I/Os with 5V tolerant**

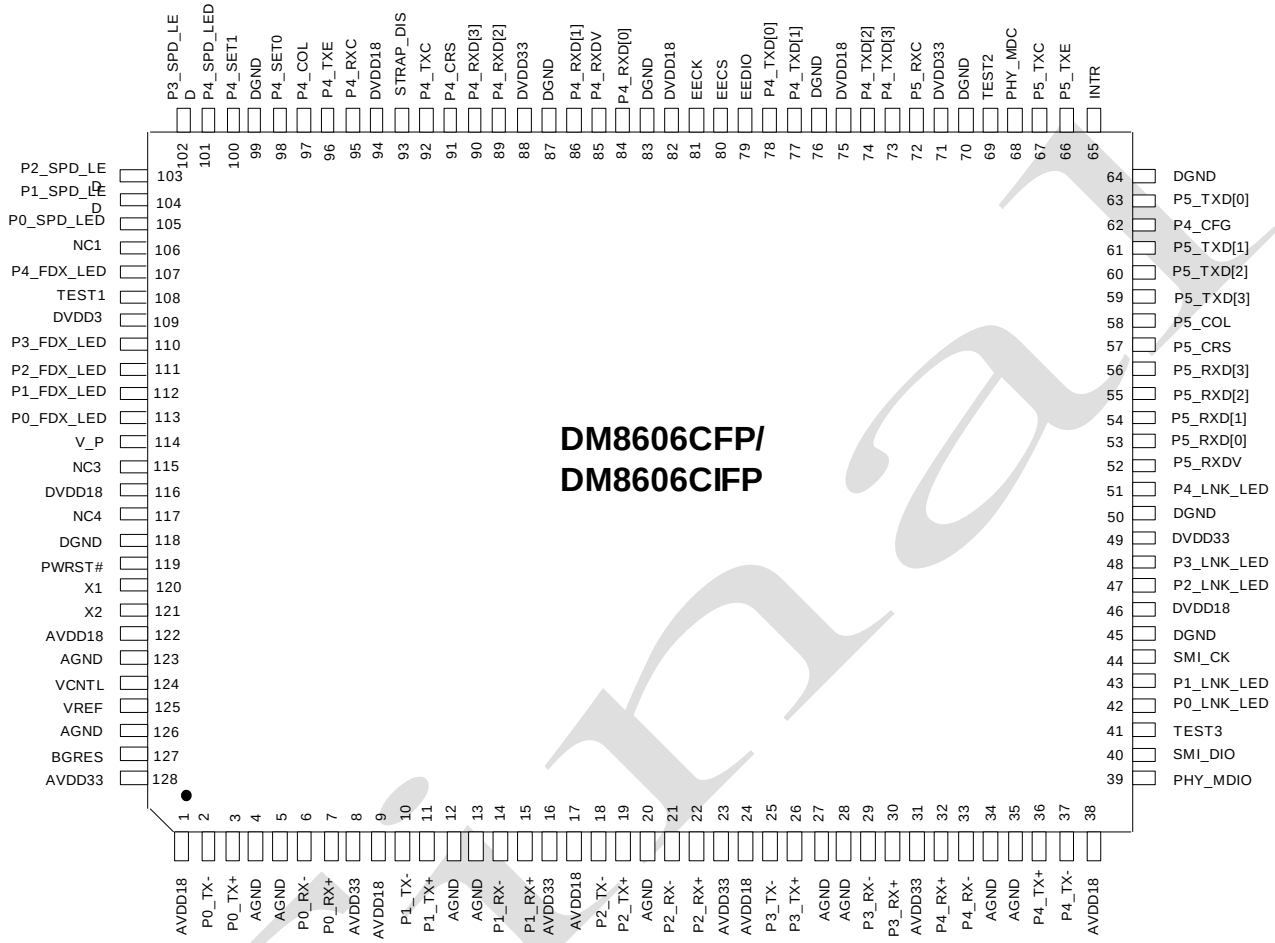
3 Block Diagram



4 Pin Configuration

4.1 Pin Diagram

4.1.1 128-Pin QFP



4.2 Pin Description

Buffer Type:					
I = Input	O = Output	I/O = Input / Output	O/D = Open Drain	P = Power	# = Asserted Low,
ANA = Analog	PD = Always internal pull – low (about 50K Ohm)			PU = always internal pull-high	
Pd = Internal pull-low during pwrst# period			Pu = Internal pull-high during pwrst# period		

4.2.1 LED Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
42	P0_LNK_LED	PU,6mA	O/D	Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY0
105	P0_SPD_LED	Pu,6mA	O/D	Port 0 Speed LED Its active state indicates that the internal PHY0 is operated in 100Mbps, or it is floating for the 10Mbps mode of the internal PHY0
113	P0_FDX_LED	Pu,6mA	O/D	Port 0 Full-duplex LED Its active state indicates that the internal PHY0 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY0
43	P1_LNK_LED	Pu,6mA	O/D	Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY1
104	P1_SPD_LED	Pu,6mA	O/D	Port 1 Speed LED Its active state indicates that the internal PHY1 is operated in 100Mbps, or it is floating for the 10Mbps mode of the internal PHY1
112	P1_FDX_LED	Pd,6mA	O/D	Port 1 Full-duplex LED Its active state indicates that the internal PHY1 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY1
47	P2_LNK_LED	Pu,6mA	O/D	Port 2 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY2
103	P2_SPD_LED	Pu,6mA	O/D	Port 2 Speed LED Its active state indicates that the internal PHY2 is operated in 100Mbps, or it is floating for the 10Mbps mode of the internal PHY2
111	P2_FDX_LED	Pu,6mA	O/D	Port 2 Full-duplex LED Its active state indicates that the internal PHY2 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY2
48	P3_LNK_LED	Pu,6mA	O/D	Port 3 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY3
102	P3_SPD_LED	Pu,6mA	O/D	Port 3 Speed LED Its active state indicates that the internal PHY3 is operated in 100Mbps, or it is floating for the 10Mbps mode of the internal PHY3

110	P3_FDX_LED	Pu,6mA	O/D	Port 3 Full-duplex LED Its active state indicates that the internal PHY3 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY3
51	P4_LNK_LED	Pu,6mA	O/D	Port 4 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY4
101	P4_SPD_LED	Pu,6mA	O/D	Port 4 Speed LED Its active state indicates that the internal PHY4 is operated in 100Mbps, or it is floating for the 10Mbps mode of the internal PHY4.
107	P4_FDX_LED	Pu,6mA	O/D	Port 4 Full-duplex LED Its active state indicates that the internal PHY4 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY4

4.2.2 EEPROM Interface

Pin No.	Pin Name	Buffer Type	I/O	Description
79	EEDIO	PD,4mA	I/O	EEPROM Data In/Output Drive/Read data to/from EEPROM
81	EECK	Pd,4mA	O	EEPROM Serial Clock Drive clock to EEPROM
80	EECS	PD,4mA	O	EEPROM Chip Selection. Drive chip selection to EEPROM

4.2.3 Clock Interface

Pin No.	Pin Name	Buffer Type	I/O	Description
120	X1	ANA	I	**25 MHz Crystal /Oscillator Input** Variation is limited to +/- 50 ppm.
121	X2	ANA	O	**25 MHz Crystal Output** When X1 is connected to oscillator, this pin should left unconnected.

4.2.4 Network Interface

Pin No.	Pin Name	Buffer Type	I/O	Description
2 3	P0_TX- P0_TX+	ANA	I/O	Port 0 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
6 7	P0_RX- P0_RX+	ANA	I/O	Port 0 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
10 11	P1_TX- P1_TX+	ANA	I/O	Port 1 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
14 15	P1_RX- P1_RX+	ANA	I/O	Port 1 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
18 19	P2_TX- P2_TX+	ANA	I/O	Port 2 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
21 22	P2_RX- P2_RX+	ANA	I/O	Port 2 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
25 26	P3_TX- P3_TX+	ANA	I/O	Port 3 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
29 30	P3_RX- P3_RX+	ANA	I/O	Port 3 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
32 33	P4_RX+ P4_RX-	ANA	I/O	Port 4 TP RX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
36 37	P4_TX+ P4_TX-	ANA	I/O	Port 4 TP TX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
127	BGRES	ANA	I/O	Bandgap Pin Connect a 6.8K 1% precision resistor to AGND in application.
124	VCNTL	ANA	I/O	1.8V Voltage control to control external BJT
125	VREF	ANA	O	Voltage Reference Connect a 0.1u capacitor to ground in application.

4.2.5 Port 4 MAC MII/RevMII/RMII and PHY MII interfaces

PORT4 MAC MII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
73,74,77,78	P4_TXD[3:0]	Pd,4mA	O	Transmit Data
96	P4_TXE	Pd,4mA	O	Transmit Enable
92	P4_TXC	Pd	I	Transmit Clock.
91	P4_CRS	PD	I	Carrier Sense
97	P4_COL	Pd	I	Collision Detect.
95	P4_RXC	Pd	I	Receive Clock
85	P4_RXDV	-	I	Receive Data Valid
90,89,86,84	P4_RXD[3:0]	PD,PD PU,PU	I	Receive Data

PORT4 MAC Reverse MII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
73,74,77,78	P4_TXD[3:0]	Pd,4mA	O	Transmit Data
96	P4_TXE	Pd,4mA	O	Transmit Enable
92	P4_TXC	Pd,4mA	O	Transmit Clock.
91	P4_CRS	PD,4mA	O	Carrier Sense
97	P4_COL	Pd,4mA	O	Collision Detect.
95	P4_RXC	Pd	I	Receive Clock
85	P4_RXDV	-	I	Receive Data Valid
90,89,86,84	P4_RXD[3:0]	PD,PD PU,PU	I	Receive Data

PORT4 MAC RMII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
73,74	P4_TXD[3:2]	Pd,4mA	O	Reserved (No connection)
77,78	P4_TXD[1:0]	Pd,4mA	O	Port4 RMII Transmit Data
96	P4_TXE	Pd,4mA	O	Transmit Enable
92	OSC50M4	Pd,4mA	O	50MHz clock for Port 4 RMII. The output is disabled in default and can be enabled by EEPROM or register 314H.
91	P4_CRS	PD	I	Reserved (No connection)
97	P4_COL	Pd	I	Reserved (No connection)
95	50MCLK4	Pd	I	50MHz clock for Port4 RMII
85	P4_CRSDV	-	I	Receive Data Valid
86,84	P4_RXD[1:0]	PU	I	Receive Data
90,89	P4_RXD[3:2]	PD	I	Reserved (No connection)

PORT4 PHY MII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
90,89,86,84	P4_TXD[3:0]	PD,PD PU,PU	I	Transmit Data
85	P4_TXE	-	I	Transmit Enable
92	P4_TXC	Pd,4mA	O	Transmit Clock.
91	P4_CRS	PD,4mA	O	Carrier Sense
97	P4_COL	Pd,4mA	O	Collision Detect.
95	P4_RXC	Pd,4mA	O	Receive Clock
96	P4_RXDV	Pd,4mA	O	Receive Data Valid
73,74,77,78	P4_RXD[3:0]	Pd,4mA	O	Receive Data

4.2.6 Port 5 MII/RevMII/RMII interfaces

PORT5 MII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
59,60,61,63	P5_TXD[3:0]	Pd,4mA	O	Transmit Data
66	P5_TXE	Pd,4mA	O	Transmit Enable
67	P5_TXC	Pd	I	Transmit Clock.
57	P5_CRS	Pd	I	Carrier Sense
58	P5_COL	Pd	I	Collision Detect.
72	P5_RXC	Pd	I	Receive Clock
52	P5_RXDV	PD	I	Receive Data Valid
56,55,54,53	P5_RXD[3:0]	PD	I	Receive Data

PORT5 Reverse MII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
59,60,61,63	P5_TXD[3:0]	Pd,4mA	O	Transmit Data
66	P5_TXE	Pd,4mA	O	Transmit Enable
67	P5_TXC	Pd,4mA	O	Transmit Clock Output.
57	P5_CRS	Pd,4mA	O	Carrier Sense Output
58	P5_COL	Pd,4mA	O	Collision Detect Output.
72	P5_RXC	Pd	I	Receive Clock
52	P5_RXDV	PD	I	Receive Data Valid
56,55,54,53	P5_RXD[3:0]	PD	I	Receive Data

PORT5 RMII pins

Pin No.	Pin Name	Buffer Type	I/O	Description
59,60	P5_TXD[3:2]	Pd	I	Reserved (No connection)
61,63	P5_TXD[1:0]	Pd,4mA	O	Transmit Data
66	P5_TXE	Pd,4mA	O	Transmit Enable
67	OSC50M5	Pd,4mA	O	50MHz Clock Output. The output is disabled in default and can be enabled by EEPROM or register 315H.
57	P5_CRS	Pd	I	Reserved (No connection)
58	P5_COL	Pd	I	Reserved (No connection)
72	50MCLK5	Pd	I	50MHz clock for Reference Clock
52	P5_CRSDV	PD	I	Receive Data Valid
54,53	P5_RXD[1:0]	PD	I	Receive Data
56,55	P5_RXD[3:2]	PD	I	Reserved (No connection)

4.2.7 Miscellaneous Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
40	SMI_DIO	PD,4mA	I/O	Serial Management Data Input/output as CPU interface
44	SMI_CK	PD,4mA	I	Serial Management Data Clock as CPU interface
39	PHY_MDIO	PD,4mA	I/O	MII Serial Management Data Input/output as External PHY interface
68	PHY_MDC	Pd,4mA	O	MII Serial Management Data Clock as External PHY interface
65	INTR	-	O	Interrupt signals to external CPU
93	STRAP_DIS	PD	I	Strap pins disabled 0: strap pins enabled 1: no strap pin function
62, 98, 100	CFG4, P4_SET0, P4_SET1	PD Pu Pd	I I I	Port 4 operation mode CFG4 P4_SET1 P4_SET0 0 0 0 use internal PHY 0 0 1 MAC MII/RMII/RevMII 1 X X PHY MII
119	PWRST#	-	I	Power on Reset Low active with minimum 10ms
41, 69, 108	TEST3, TEST2, TEST1	PD PD PD	I I I	Test pins Tie TEST3 to ground in application Tie TEST2 and TEST1 to DVDD33 in application
114	V_P	Pd	I	Virtual PHY 1 = Enable 0 = Disable
106, 115, 117	NC1, NC3, NC4	Pd Pd Pd	I I I	NO Connection Pull low to these pins in application, unless the strap pin is used.

4.2.8 Power Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
49,71,88,109	DVDD33	PWR		Digital 3.3V power
46,75,82,94,116	DVDD18	PWR		Digital 1.8V power
50,64,70,76, 83,87,99,118	DGND	GND		Digital GND
8,16,23,31,128	AVDD33	PWR		Analog 3.3V power
1,9,17,24,38,122	AVDD18	PWR		Analog 1.8V power
4,5,12,13,20,27, 28,34,35,123,126	AGND	GND		Analog GND

4.3 Strap Pin Table

1: pull-high 1K~10K, 0: floating

Pin No.	Pin Name	Description
51	P4_LNK_LED	Port 4 PHY 1 = Copper mode 0 = Fiber mode
101	P4_SPD_LED	When in Port4 in force mode 1 = link ON 0 = link OFF
102,103	P3_SPD_LED, P2_SPD_LED	When Port 4 in MAC MII/RMII/RevMII P3_SPD_LED P2_SPD_LED 0 0 RevMII with P4_TXC turbo clock 0 1 RMII 1 0 MII 1 1 RevMII with P4_TXC 25MHz/2.5MHz clock When Port 4 PHY MII mode P3_SPD_LED P2_SPD_LED 0 X Reserved 1 X PHY_MII
104	P1_SPD_LED	When,Port4 in force mode 1 = 100M mode 0 = 10M mode
105	P0_SPD_LED	When,Port4 in force mode 1 = Full-duplex mode 0 = Half-duplex mode
107	P4_FDX_LED	When Port5 in force mode 1 = link ON 0 = link OFF

110,111	P3_FDX_LED, P2_FDX_LED	Port 5 Mode P3_FDX_LED P2_FDX_LED 0 0 Reserved 0 1 RMII 1 0 MII 1 1 RevMII
112	P1_FDX_LED	When Port5 in force mode 1 = 100M mode 0 = 10M mode
113	P0_FDX_LED	When Port5 in force mode 1 = Full-duplex mode 0 = Half-duplex mode
115	NC3	Flow Control in PHY Register 4 bit 10 1 = bit value is “0” 0 = bit value is “1”
80	EECS	Port 5 link/duplex/speed mode in MII/RMII 1 = PHY_MDC/PHY_MDIO polling mode 0 = force mode If Port 5 link/duplex/speed mode in RevMII mode, Port 5 always in force mode
81	EECK	When Port 4 link/duplex/speed mode in MII/RMII 1 = PHY_MDC/PHY_MDIO polling mode 0 = force mode When Port 4 link/duplex/speed mode in RevMII mode, Port 4 always in force mode

5 Control and Status Register Set

The DM8606C/DM8606CI implements several control and status registers (CSRs), which can be accessed by the host SMI interface via SMI_CK and SMI_DIO pins. The serial format of host SMI can be referenced in Section 6.2. The absolute address in the following register table is the 10-bit R9~R0 field in the SMI format. For easy to understanding, the 10-bit **absolute address** can be divided to 5-bit **PHY address** plus 5-bit **register address** like used in general MII serial format. All CSRs are set to their default values by hardware or software reset unless specified

Register Table

Register Name	PHY Address	Register Address	Absolute Address
P0 PHY Control	02H	00H	040H
P0 PHY Status	02H	01H	041H
P0 PHY ID 1	02H	02H	042H
P0 PHY ID 2	02H	03H	043H
P0 PHY Auto-N Advertisement	02H	04H	044H
P0 PHY Auto-N Link Partner Ability	02H	05H	045H
P0 PHY Auto-N Expansion	02H	06H	046H
P0 PHY Standard Reserved	02H	07H~0FH	047H~04FH
P0 PHY Vendor Registers	02H	10H~1FH	050H~05FH
Port 1 PHY Registers	03H	00H~1FH	060H~07FH
Port 2 PHY Registers	04H	00H~1FH	080H~09FH
Port 3 PHY Registers	05H	00H~1FH	0A0H~0BFH
Port 4 PHY Registers	06H	00H~1FH	0C0H~0DFH
Port 5 External PHY Registers	07H	00H~1FH	0E0H~0FFH
P0 Port Status	08H	10H	110H
P0 Basic Control 0	08H	11H	111H
P0 Basic Control 1	08H	12H	112H
P0 Block Contrl 0	08H	13H	113H
P0 Block Contrl 1	08H	14H	114H
P0 Bandwidth Control	08H	15H	115H
P0 VLAN Tag Infomation	08H	16H	116H
P0 Priority & VLAN Control	08H	17H	117H
P0 Security Control	08H	18H	118H
P0 Spanning Tree state Control	08H	19H	119H
P0 Memory Configuration	08H	1AH	11AH
P0 Discard packet limitation	08H	1BH	11BH
Port 1 Registers	09H	10H~1FH	130H~14FH
Port 2 Registers	0AH	10H~1FH	150H~16FH
Port 3 Registers	0BH	10H~1FH	170H~18FH
Port 4 Registers	0CH	10H~1FH	190H~1AFH
Port 5 Registers	0DH	10H~1FH	1B0H~1CFH
Switch Status	10H	10H	210H
Switch Reset	10H	11H	211H
Switch Control	10H	12H	212H
CPU Port & Mirror Control	10H	13H	213H
Special Tag Ether-Type	10H	14H	214H
Global Learning & Aging Control	10H	15H	215H
VLAN Priority Map	10H	17H	217H
TOS Priority Map 0~7	10H	18H~1FH	218H~21FH
MIB Counter Disable	11H	10H	230H

MIB Counter Control	11H	11H	231H
MIB Counter Data Low	11H	12H	232H
MIB Counter Data High	11H	13H	233H
QinQ TPID	11H	1DH	23DH
VLAN Mode & Rule Control	11H	1EH	23EH
VLAN Table - Valid Control	11H	1FH	23FH
VLAN Table - ID_0H~FH	12H	10H~1FH	250H~25FH
VLAN Table - MEMBER_0H~FH	13H	10H~1FH	270H~27FH
VLAN Table - Priority Enable	14H	10H	290H
RESERVED	14H	11H	291H
VLAN Table - STP Index Enable	14H	12H	292H
VLAN Table - Misc_0~7	14H	13H~1AH	293H~29AH
Snooping Control 0	14H	1BH	29BH
Snooping Control 1	14H	1CH	29CH
Address Table Control & Status	15H	10H	2B0H
Address Table Data 0~4	15H	11H~15H	2B1H~2B5H
Vendor ID	18H	10H	310H
Product ID	18H	11H	311H
Chip Revision	18H	12H	312H
Port 4 MAC Control	18H	14H	314H
Port 5 MAC Control	18H	15H	315H
LED Control	18H	17H	317H
Interrupt Status Register	18H	18H	318H
Interrupt Mask & Control Register	18H	19H	319H
EEPROM Control & Address	18H	1AH	31AH
EEPROM Data	18H	1BH	31BH
Monitor Register 1 ~ 3	18H	1CH~1EH	31CH~31EH
System Clock Select Register	19H	18H	338H
Serial Bus Error Check Registers	19H	19H~1AH	339H~33AH
Virtual PHY Control Register	19H	1DH	33DH
PHY Control Test	19H	1EH	33EH

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>:

1	Bit set to logic one	P =	power on reset default value
0	Bit set to logic zero	Y =	default value from PHY software reset by per port PHY register 0 bit 15
X	No default value	S =	software reset default value
?H	Bits set to hex. value	E =	default value from EEPROM
		T =	default value from strap pin

<Access Type>:

RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1 = Read/Write and Cleared by write 1
WO = Write only
R/WC = Read/Write and auto-cleared

Reserved bits should be written with 0.
Reserved bits are undefined on read access.

5.1 Port0~Port4 PHY Registers (000H~0FFH)

5.1.1 Basic Mode Control Register (BMCR) (040H,060H,080H,0A0H,0C0H)

Bit	Bit Name	Default	Description
15	Reset	P0, RW/SC	Reset 1 = Software reset 0 = Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
14	Loopback	PY0,RW	Loopback Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs
13	Speed selection	PY1,RW	Speed Select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled (bit 12 is set), this bit will return auto-negotiation selected medium type
12	Auto-negotiation enable	PT1,RW	Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status 0 = Auto-negotiation is disabled
11	Power down	PY0,RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1 = Power down 0 = Normal operation
10	Isolate	PY0,RW	Isolate 1 = Reserved in DM8606C/DM8606CI 0 = Normal operation
9	Restart Auto-negotiation	PY0, RW/SC	Restart Auto-negotiation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM8606C/DM8606CI. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation
8	Duplex mode	PY1,RW	Duplex Mode 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation
7	Collision test	PY0,RW	Collision Test 1 = Reserved in DM8606C/DM8606CI 0 = Normal operation
6:0	Reserved	P0H,RO	Reserved Read as 0, ignore on write

5.1.2 Basic Mode Status Register (BMSR) (041H,061H,081H,0A1H,0C1H)

Bit	Bit Name	Default	Description
15	100BASE-T4	P0,RO	100BASE-T4 Capable 1 = perform in 100BASE-T4 mode 0 = not able to perform in 100BASE-T4 mode
14	100BASE-TX full-duplex	P1,RO	100BASE-TX Full Duplex Capable 1 = perform 100BASE-TX in full duplex mode 0 = not able to perform 100BASE-TX in full duplex mode
13	100BASE-TX half-duplex	P1,RO	100BASE-TX Half Duplex Capable 1 = perform 100BASE-TX in half duplex mode 0 = not able to perform 100BASE-TX in half duplex mode
12	10BASE-T full-duplex	P1,RO	10BASE-T Full Duplex Capable 1 = perform 10BASE-T in full duplex mode 0 = not able to perform 10BASE-TX in full duplex mode
11	10BASE-T half-duplex	P1,RO	10BASE-T Half Duplex Capable 1 = perform 10BASE-T in half duplex mode 0 = not able to perform 10BASE-T in half duplex mode
10:7	Reserved	P0,RO	Reserved Read as 0, ignore on write
6	MF preamble suppression	PY1,RO	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-negotiation Complete	PY0,RO	Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
4	Remote fault	PY0,RO	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
3	Auto-negotiation ability	P1,RO	Auto Configuration Ability 1 = perform auto-negotiation 0 = not able to perform auto-negotiation
2	Link status	PY0,RO	Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1	Jabber detect	PY0,RO	Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit works only in 10Mbps mode
0	Extended capability	P1,RO	Extended Capability 1 = Extended register capable 0 = Basic register capable only

5.1.3 PHY ID Identifier Register #1 (PHYID1) (042H,062H,082H,0A2H,0C2H)

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM8606C/DM8606CI. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15:0	OUI_MSB	PE0181H, RO	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

5.1.4 PHY ID Identifier Register #2 (PHYID2) (043H,063H,083H,0A3H,0C3H)

Bit	Bit Name	Default	Description
15:10	OUI_LSB	PE101110, RO	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9:4	VNDR_MDL	PE001011, RO	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3:0	MDL_REV	PE0001, RO	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

5.1.5 Auto-Nego. Advertised Register (ANAR) (044H,064H,084H,0A4H,0C4H)

This register contains the advertised abilities of this port as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	P0,RO	Next page Indication 1 = Next page available 0 = No next page available The DM8606C/DM8606CI has no next page, so this bit is permanently set to 0
14	ACK	PY0,RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM8606C/DM8606CI's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit.
13	RF	PY0,RW	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
12:11	Reserved	X,RW	Reserved Write as 0, ignore on read
10	FCS	PT0,RW	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	P0,RO	100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM8606C/DM8606CI does not support 100BASE-T4 so this bit is permanently set to 0
8	TX_FDX	PY1,RW	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
7	TX_HDX	PY1,RW	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported
6	10_FDX	PY1,RW	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
5	10_HDX	PY1,RW	10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported
4:0	Selector	PY00001, RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

5.1.6 Auto-Nego. Partner Ability Register (ANPAR) (045H,065H,085H,0A5H,0C5H)

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	PY0,RO	Next Page Indication 1 = Link partner, next page available 0 = Link partner, no next page available
14	ACK	PY0,RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM8606C/DM8606CI's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit
13	RF	PY0,RO	Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12:11	Reserved	PY0,RO	Reserved Read as 0, ignore on write
10	FCS	PY0,RO	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	PY0,RO	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	PY0,RO	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
7	TX_HDX	PY0,RO	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
6	10_FDX	PY0,RO	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5	10_HDX	PY0,RO	10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
4:0	Selector	PY00000, RO	Protocol Selection Bits Link partner's binary encoded protocol selector

5.1.7 Auto-Nego. Expansion Register (ANER) (046H,066H,086H,0A6H,0C6H)

Bit	Bit Name	Default	Description
15:5	Reserved	P0,RO	Reserved Read as 0, ignore on write
4	PDF	PY0,RO	Local Device Parallel Detection Fault 1 = A fault detected via parallel detection function. 0 = No fault detected via parallel detection function
3	LP_NP_EN	PY0,RO	Link Partner Next Page Able 1 = Link partner, next page available 0 = Link partner, no next page
2	NP_ABLE	P0,RO	Local Device Next Page Able 1 = this port next page available 0 = this port no next page DM9161C does not support this function, so this bit is always 0
1	PAGE_RX	PY0,RO	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_EN	PY0,RO	Link Partner Auto-negotiation Able 1 = the link partner supports Auto-negotiation 0 = the link partner do not support Auto-negotiation

5.1.8 Specified Control 1 Register (SC1R) (050H,070H,090H,0B0H,0D0H)

Bit	Bit Name	Default	Description
15	BP_4B5B	PY0,RW	Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
14	BP_SCR	PY0,RW	Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
13	BP_ALIGN	PY0,RW	Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
12:11	Reserved	PY0,RW	Reserved
10	TX	PY1,RW	100BASE-TX Mode Control 1 = 100BASE-TX operation 0 = 100BASE-FX operation (Fiber mode)
9:5	Reserved	PY0,RW	Reserved
4	Reserved	PY1,RW	Reserved
3	Reserved	PY0,RW	Reserved
2	Reserved	PY1,RW	Reserved
1:0	Reserved	PY0,RW	Reserved

5.1.9 Specified Control 2 Register (SC2R) (054H,074H,094H,0B4H,0D4H)

Bit	Bit Name	Default	Description
15:12	RESERVED	PY0,RW	Reserved
11	PREAMBLEX	PY0,RW	Preamble Saving Control 1 = 10M TX preamble bit count is normal. 0 = when bit 10 is set, the 10M TX preamble count is reduced When bit 11 of per port PHY register 1DH is set, 12-bit preamble bit is reduced; otherwise 22-bit preamble bit is reduced.
10	TX10M_PWR	PY0,RW	10M TX Power Saving Control 1 = enable 10M TX power saving 0 = disable 10M TX power saving
9	NWAY_PWR	PY0,RW	N-Way Power Saving Control 1 = disable N-Way power saving 0 = enable N-Way power saving
8	Reserved	P0, RO	Reserved Read as 0, ignore on write
7	MDIX_CNTL	PYX,RO	The polarity of MDI/MDIX value 1 = MDIX mode 0 = MDI mode
6	AutoNeg_dpbk	PY0,RW	Auto-negotiation Loopback 1 = test internal digital auto-negotiation Loopback 0 = normal.
5	Mdix_fix Value	PY0,RW	MDIX_CNTL force value: When MDIX_DOWN = 1, MDIX_CNTL value depend on the register value.
4	Mdix_down	PY0,RW	MDIX Down Manual force MDI/MDIX. 1 = Disable HP Auto-MDIX , MDIX_CNTL value depend on bit 5 0 = Enable HP Auto-MDIX
3:0	Reserved	PY0,RW	Reserved

5.1.10 Power Saving Control Register (PSCR) (05DH,07DH,09DH,0BDH,0DDH)

Bit	Bit Name	Default	Description
15:12	RESERVED	P0,RO	Reserved
11	PREAMBLEX	PY0,RW	Preamble Saving Control When bit 10 of per port PHY register 14H is cleared and bit 11 of Per port PHY register 14H is set, the 10M TX preamble count is reduced. 1 = 10-bit preamble bit is reduced. 0 = 20-bit preamble bits is reduced.
10	RESERVED	PY0,RW	Reserved
9	TX_PWR	PY0.RW	TX Power Saving Control Disabled 1 = disable TX driving power saving function 0 = when cable is unconnected with link partner, the driving current of transmit is reduced for power saving.
8:0	RESERVED	P0,RO	Reserved

5.2 Switch Per-Port Registers (100H~1FFH)

5.2.1 Per Port Status Data Register (110H,130H,150H,170H,190H,1B0H)

Bit	Name	ROM	Default	Description
15:5	RESERVED	---	P0,RO	Reserved
4	LP_FCS	---	P0,RO	Link Partner Flow Control Enable Status This bit is same as bit 10 of per port PHY register 15H.
3:2	SPEED	---	P0,RO	PHY Speed Status 00 = 10Mbps 01 = 100Mbps 1X = Reserved
1	FDX	---	P0,RO	PHY Duplex Status 1 = Full-duplex 0 = Half-duplex
0	LINK	---	P0,RO	PHY Link Status 1 = Link OK 0 = Link fail

5.2.2 Per Port Basic Control 0 Register (111H,131H,151H,171H,191H,1B1H)

Bit	Name	ROM	Default	Description
15	RESERVED	---	P0,RO	Reserved
14	UPLG_CLS	128[14] 14414] 160[14] 176[14] 192[14] 208[14]	PSE0,RW	Unplug Clear Address Enable Enable to automatically clear address record in address table after unplug 1 = Enable, clearing address record 0 = Disable, retaining address record
13	AGE_DIS	128[13] 144[13] 160[13] 176[13] 192[13] 208[13]	PSE0,RW	Address Table Aging 1 = Age function is disabled 0 = Age function is enabled
12	ADLRN_DIS	128[12] 144[12] 160[12] 176[12] 192[12] 208[12]	PSE0,RW	Address Learning Disabled 1 = The SMAC field of packet will not be learned to address table. 0 = Source address (SMAC) learning function is enabled
11	DIS_PAUSE	128[11] 144[11] 160[11] 176[11] 192[11] 208[11]	PSE0,RW	Maximum Pause Packet from Link Partner 1 = Pause packet is bypassed after 7 continued pause packet from link partner 0 = Always care pause packet from link partner
10	RESERVED	---	P0,RO	Reserved
9	HOB_DIS	128[9] 144[9] 160[9] 176[9] 192[9] 208[9]	PSE0,RW	Head-of-Line Blocking Prevent Control 1 = Enable 0 = Disable
8	LOOPBACK	---	PS0,RW	Loop-Back Mode 1 = The transmitted packets will be forward to this port itself. 0 = Disable

7	PAUSE_CN	128[7] 144[7] 160[7] 176[7] 192[7] 208[7]	PSE0,RW	Send PAUSE Continuously If buffer congestion occur on full duplex, switch will send PAUSE frames: 1 = Continuously until alleviation. 0 = Up to 8-times.
6	PARTI_EN	128[6] 144[6] 160[6] 176[6] 192[6] 208[6]	PSE0,RW	Partition Detection Enable 1 = Enable 0 = Disable
5	FCBP_DIS	128[5] 144[5] 160[5] 176[5] 192[5] 208[5]	PSE0,RW	Back pressure Flow-Control in half duplex disable 1 = Back pressure is disabled 0 = Back pressure is enabled
4	FC3X_DIS	128[4] 144[4] 160[4] 176[4] 192[4] 208[4]	PSE0,RW	IEEE 802.3x Flow control in full duplex mode 1 = 802.3x flow-control is disabled 0 = 802.3x flow-control is enabled
3:2	MAX_PKLN	128[3:2] 144[3:2] 160[3:2] 176[3:2] 192[3:2] 208[3:2]	PSE0,RW	Max accept packet length by RX from this port 00 = 1536-bytes 01 = 1552-bytes 10 = 1800-bytes 11 = 2032-bytes
1	RX_DIS	---	PS0,RW	Receive Disable 1 = All received packets from this port are discarded. 0 = Receive is enabled
0	TX_DIS	---	PS0,RW	Transmit Disable 1 = All packets forward to this port are discarded. 0 = Transmit function is enabled

5.2.3 Per Port Basic Control 1 Register (112H,132H,152H,172H,192H,1B2H)

Bit	Name	ROM	Default	Description
15	NO_DIS_RX	129[15] 145[15] 161[15] 177[15] 193[15] 209[15]	PSE0,RW	RX Packet Control When bandwidth of RX Packets reach Ingress bandwidth control value: 1 = Retain RX packets in memory 0 = Discard RX packets
14	BANDWIDTH	129[14] 145[14] 161[14] 177[14] 193[14] 209[14]	PSE0,RW	Bandwidth Control Mode 1 = Combined mode. Combining the rate of ingress and egress 0 = Separated mode. Rate control of ingress and egress is separate.
13	STORM_UP	129[13] 145[13] 161[13] 177[13] 193[13] 209[13]	PSE0,RW	Storm Control for Un-learned Unicast Packets 1 = Enable; treat the un-learned uni-cast packets as broadcast storm packets 0 = Disable
12	STORM_MP	129[12] 145[12] 161[12] 177[12] 193[12] 209[12]	PSE0,RW	Storm Control for Multicast Packets 1 = Enable; treat the multicast packets as broadcast storm packets 0 = Disable
11	MIRR_DBP	129[11] 145[11] 161[11] 177[11] 193[11] 209[11]	PSE0,RW	Don't Mirror Broadcast/Multicast Packets If mirror function is enabled 1 = Broadcast/Multicast would not be mirrored 0 = Broadcast/Multicast would be mirrored
10	FIR_SPEC	129[10] 145[10] 161[10] 177[10] 193[10] 209[10]	PSE0,RW	Specific MAC Filtering Control Enable Enable to filter packet with source or destination MAC address that is specified in the address table. 1 = Enable 0 = Disable
9	FIR_UUSID	129[9] 145[9] 1619] 177[9] 193[9] 209[9]	PSE0,RW	Filter Packets with Un-learned Unicast SMAC 1 = Enable 0 = Disable
8	FIR_UUDID	129[8] 145[8] 161[8] 177[8] 193[8] 209[8]	PSE0,RW	Filter Packets with Un-learned Unicast DMAC 1 = Enable 0 = Disable
7	FIR_UMDID	129[7] 145[7] 161[7] 177[7] 193[7] 209[7]	PSE0,RW	Filter Packets with Un-learned Multicast DMAC 1 = Enable 0 = Disable

6	FIR_BDMAC	129[6] 145[6] 161[6] 177[6] 193[6] 209[6]	PSE0,RW	Filter Packets with Broadcast DMAC 1 = Enable 0 = Disable
5	FIR_MDMAC	129[5] 145[5] 161[5] 177[5] 193[5] 209[5]	PSE0,RW	Filter Packets with Multicast DMAC 1 = Enable 0 = Disable
4	FIR_MSMAC	129[4] 145[4] 161[4] 177[4] 193[4] 209[4]	PSE0,RW	Filter Packets with Multicast SMAC 1 = Enable 0 = Disable
3:2	MIRR_TX	129[3:2] 145[3:2] 1613:2] 177[3:2] 193[3:2] 209[3:2]	PSE0,RW	Port TX Mirror Option TX Packet is mirrored to sniffer port. 00 = TX mirror function is disabled 01 = All transmitted packets is mirrored 10 = Packet is mirrored if (DMAC search result is hit & ATB_MIRR==1 & Transmit from this port) 11 = Packet is mirrored if (SMAC search result is hit & ATB_MIRR==1 & Transmit from this port)
1:0	MIRR_RX	129[1:0] 145[1:0] 161[1:0] 177[1:0] 193[1:0] 209[1:0]	PSE0,RW	Port RX Mirror Option RX Packet is mirrored to sniffer port. 00 = RX mirror function is disabled 01 = All received packets is mirrored 10 = Packet is mirrored if (DMAC search result is hit & ATB_MIRR==1 & Receive from this port) 11 = Packet is mirrored if (SMAC search result is hit & ATB_MIRR==1 & Receive from this port)

5.2.4 Per Port Block Control 0 Register (113H,133H,153H,173H,193H,1B3H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	BLK_MP	130[13:8] 146[13:8] 162[13:8] 178[13:8] 194[13:8] 210[13:8]	PSE0,RW	Block Packet with Multicast DMAC [13]: Block such packet forward to port 5 [12]: Block such packet forward to port 4 [11]: Block such packet forward to port 3 [10]: Block such packet forward to port 2 [09]: Block such packet forward to port 1 [08]: Block such packet forward to port 0
7:6	RESERVED	---	P0,RO	Reserved
5:0	BLK_BP	130[5:0] 146[5:0] 162[5:0] 178[5:0] 194[5:0] 210[5:0]	PSE0,RW	Block Packet with Broadcast DMAC [05]: Block such packet forward to port 5 [04]: Block such packet forward to port 4 [03]: Block such packet forward to port 3 [02]: Block such packet forward to port 2 [01]: Block such packet forward to port 1 [00]: Block such packet forward to port 0

5.2.5 Per Port Block Control 1 Register (114H,134H,154H,174H,194H,1B4H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	BLK_UKP	131[13:8] 147[13:8] 163[13:8] 179[13:8] 195[13:8] 211[13:8]	PSE0,RW	Block Packet with Unlearned Unicast DMAC [13]: Block such packet forward to port 5 [12]: Block such packet forward to port 4 [11]: Block such packet forward to port 3 [10]: Block such packet forward to port 2 [09]: Block such packet forward to port 1 [08]: Block such packet forward to port 0
7:6	RESERVED	---	P0,RO	Reserved
5:0	BLK_UP	131[5:0] 147[5:0] 163[5:0] 179[5:0] 195[5:0] 211[5:0]	PSE0,RW	Block Packet with Unicast DMAC The received unicast packets are not forward to the assigned ports. Note that the assigned port definition: bit 0 for port 0, bit 1 for port 1, bit 2 for port 2, and so on [05]: Block such packet forward to port 5 [04]: Block such packet forward to port 4 [03]: Block such packet forward to port 3 [02]: Block such packet forward to port 2 [01]: Block such packet forward to port 1 [00]: Block such packet forward to port 0

5.2.6 Per Port Bandwidth Control Register (115H,135H,155H,175H,195H,1B5H)

Bit	Name	ROM	Default	Description
15:12	INGRESS	132[15:12] 148[15:12] 164[15:12] 180[15:12] 196[15:12] 212[15:12]	PSE0,RW	Ingress Rate Control (Separated mode) These bits define the bandwidth threshold that received packets over the threshold are discarded. 0000 = none 0001 = 64Kbps 0010 = 128Kbps 0011 = 256Kbps 0100 = 512Kbps 0101 = 1Mbps 0110 = 2Mbps 0111 = 4Mbps 1000 = 8Mbps 1001 = 16Mbps 1010 = 32Mbps 1011 = 48Mbps 1100 = 64Mbps 1101 = 72Mbps 1110 = 80Mbps 1111 = 88Mbps
11:8	EGRESS	132[11:8] 148[11:8] 164[11:8] 180[11:8] 196[11:8] 212[11:8]	PSE0,RW	Egress Rate Control These bits define the bandwidth threshold that transmitted packets over the threshold are discarded. 0000 = none 0001 = 64Kbps 0010 = 128Kbps 0011 = 256Kbps 0100 = 512Kbps 0101 = 1Mbps 0110 = 2Mbps 0111 = 4Mbps 1000 = 8Mbps 1001 = 16Mbps 1010 = 32Mbps 1011 = 48Mbps 1100 = 64Mbps 1101 = 72Mbps 1110 = 80Mbps 1111 = 88Mbps

7:4	BSTH	132[7:4] 148[7:4] 164[7:4] 180[7:4] 196[7:4] 212[7:4]	PSE0,RW	Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded 0000 = no broadcast storm control 0001 = 8K packets/sec 0010 = 16K packets/sec 0011 = 64K packets/sec 0100 = 5% 0101 = 10% 0110 = 20% 0111 = 30% 1000 = 40% 1001 = 50% 1010 = 60% 1011 = 70% 1100 = 80% 1101 = 90% 111X = no broadcast storm control
3:0	BW_CTRL	132[3:0] 148[3:0] 164[3:0] 180[3:0] 196[3:0] 212[3:0]	PSE0,RW	Ingress and Egress Rate Control (Combined mode) Received and Transmitted Bandwidth Control These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded 0000 = none 0001 = 64Kbps 0010 = 128Kbps 0011 = 256Kbps 0100 = 512Kbps 0101 = 1Mbps 0110 = 2Mbps 0111 = 4Mbps 1000 = 8Mbps 1001 = 16Mbps 1010 = 32Mbps 1011 = 48Mbps 1100 = 64Mbps 1101 = 72Mbps 1110 = 80Mbps 1111 = 88Mbps

5.2.7 Per Port VLAN Tag Infomation Register (116H,136H,156H,176H,196H,1B6H)

Bit	Name	ROM	Default	Description
15:13	PPRI	133[15:13] 149[15:13] 165[15:13] 18115:13] 197[15:13] 213[15:13]	PSE0,RW	Port VLAN Priority Used for tag insertion
12	PCFI	133[12] 149[12] 165[12] 181[12] 197[12] 213[12]	PSE0,RW	Port VLAN CFI Used for tag insertion
11:0	PVID	133[11:0] 149[11:0] 165[11:0] 181[11:0] 197[11:0] 213[11:0]	PSE1,RW	Port VLAN Identification Used for tag insertion and VLAN table

5.2.8 Per Port Priority and VLAN Control Register (117H,137H,157H,177H,197H,1B7H)

Bit	Name	ROM	Default	Description
15	RESERVED	---	P0,RO	Reserved
14	TAG_OUT	134[14] 150[14] 166[14] 182[14] 198[14] 214[14]	PSE0,RW	Output Tagging Enable Force output tagging regardless of VLAN table setting. 1 = Enable 0 = Disable
13	FIR_VPKT	134[13] 150[13] 166[13] 182[13] 198[13] 214[13]	PSE0, RW	Filter VLAN Packet To filter incoming packet if its port does not exist in VLAN member set 1 = Enable 0 = Disable
12	UNTAG_IN	134[12] 150[12] 166[12] 182[12] 198[12] 214[12]	PSE0,RW	Input Force No Tag Assume all received frame are untagged 1 = Enable 0 = Disable
11:10	RESERVED	---	P0,RO	Reserved
9:8	VLAN_IAC	134[9:8] 150[9:8] 166[9:8] 182[9:8] 198[9:8] 214[9:8]	PSE0,RW	VLAN Ingress Admit Only Control 00 = Accept all frames 01 = Accept VLAN-tagged frames only Untagged or priority tagged(VID=0) frames will be dropped 10 = Accept untagged frames only 11 = Accept frame's VID equal to ingress PVID
7	RESERVED	---	PSE0,RW	Reserved

6	PRI_DIS	134[6] 150[6] 166[6] 182[6] 198[6] 214[6]	PSE0,RW	Priority Queue Disable 1 = Priority Queue is disabled 0 = Priority Queue is enabled
5	WFQUE	134[5] 150[5] 166[5] 182[5] 198[5] 214[5]	PSE0,RW	Priority Scheduling Method 1 = Weighted Round-Robin with 8:4:2:1 ratio 0 = Strict (Queue 3 > 2 > 1 > 0). Always highest priority queue first.
4	TOS_PRI	134[4] 150[4] 166[4] 182[4] 198[4] 214[4]	PSE0,RW	Priority Classification IP ToS over VLAN 1 = Priority Classification base on IP ToS field 0 = Priority Classification base on VLAN
3	TOS_OFF	134[3] 150[3] 166[3] 182[3] 198[3] 214[3]	PSE0,RW	IP ToS Priority Classification Disable 1 = Classification is disabled 0 = Classification is enabled
2	PRI_OFF	134[2] 150[2] 166[2] 182[2] 198[2] 214[2]	PSE0,RW	VLAN Priority Classification Disable 1 = Classification is disabled 0 = Classification is enabled
1:0	PB_PQ	134[1:0] 150[1:0] 166[1:0] 182[1:0] 198[1:0] 214[1:0]	PSE0,RW	Port-based Priority Queue Number 00 = Queue 0 01 = Queue 1 10 = Queue 2 11 = Queue 3

5.2.9 Per Port Security Control Register (118H,138H,158H,178H,198H,1B8H)

Bit	Name	ROM	Default	Description
15	RESERVED	---	P0,RO	Reserved
14:10	MAX_LRN	135[14:10] 151[14:10] 167[14:10] 183[14:10] 199[14:10] 215[14:10]	PSE0,RW	Learning Restriction. Limited number of learned MAC address 1~31, 0 = Limitless
9	P_UNAUTH	135[9] 151[9] 167[9] 183[9] 199[9] 215[9]	PSE0,RW	Port in Unauthorized State 1 = Port is in unauthorized state (disable mode). TX/RX and learning capability is disabled. Only EAPoL packet can be forwarded. 0 = Port is in authorized state (normal mode). TX/RX and learning capability is enabled.
8:2	RESERVED	---	P0,RO	Reserved
1:0	PLOCK_M	135[1:0] 151[1:0] 167[1:0] 183[1:0] 199[1:0] 215[1:0]	PSE0,RW	Port Locking Mode 00 = Port Lock is disabled 01 = First Lock 10 = First Link Lock 11 = Assign Lock

5.2.10 Per Port Advanced Control register (119H,139H,159H,179H,199H,1B9H)

Bit	Name	ROM	Default	Description
15:9	RESERVED	---	P0,R0	Reserved
8	FAST_LEAVE	136[8] 152[8] 168[8] 184[8] 200[8] 216[8]	PSE,R0	IGMP Snooping Fast Leave Enable 1 = Enable 0 = Disable
7:6	RESERVED	---	PS00,RW	Reserved
5:4	RESERVED	---	PS00,RW	Reserved
3:2	RESERVED	---	PS00,RW	Reserved
1:0	STPS0	---	PS00,RW	STP/RSTP Port State There are 4 port states for STP supporting, and 3 port states for RSTP supporting. 00 = Forwarding State, The port transmits and receives packets normally & learning is enabled. 01 = Disabled State/Discarding, The port will only forward the packets that are to and from uP port (span packets) & learning is disabled. 10 = Learning State, The port will only forward the packets that are to and from uP port (span packets) & leaning is enabled. 11 = Blocking/Listening State, The port will only forward the packets that are to and from uP port (span packets) & learning is disabled.

5.2.11 Per Port Memory Control Register (11AH,13AH,15AH,17AH,19AH,1BAH)

Bit	Name	ROM	Default	Description
15:8	TDRQ_TH	137[15:8] 153[15:8] 169[15:8] 185[15:8] 201[15:8] 217[15:8	PSE19H, RW	TDR output queue block threshold value, the block unit is “128bytes”. It is used generally when Head-of-Line Blocking, per port register 1 bit 19H, is set.
7	RESERVED	---	P0,RO	Reserved
6:0	RV_BLKSIZ	137[6:0] 153[6:0] 169[6:0] 185[6:0] 201[6:0] 217[6:0]	PSE3AH, RW	Per port receive buffer reserved block size, the block unit is “128bytes”. Use software to programming this field, the Maximum value is 3EH

5.2.12 Per Port Discard Limitation Register (11BH,13BH,15BH,17BH,19BH,1BBH)

Bit	Name	ROM	Default	Description
15	RESERVED	---	P0,R0	Reserved
14:8	RV_HI_TH	138[14:8] 154[14:8] 170[14:8] 186[14:8] 202[14:8] 218[14:8]	PSE20H, RW	Per port receive buffer reserved block high water threshold, the block unit is “128bytes”
7	RESERVED	---	P0,R0	Reserved
6:0	RV_LO_TH	138[6:0] 154[6:0] 170[6:0] 186[6:0] 202[6:0] 218[6:0]	PSE0,RW	Per port receive buffer reserved block Low water threshold, the block unit is “128bytes”

5.3 Switch Engine Registers (200H~2FFH)

5.3.1 Switch Status Register (210H)

Bit	Name	ROM	Default	Description
15:4	RESERVED	---	RO	Reserved
3	RV_BUF_ST	---	RO	Receive Buffer Status 1 = There are packets in buffer 0 = No packet in buffer
2	RESERVED	---	RO	Reserved
1	BIST_1	---	RO	Memory 1 BIST Status for address table memory 1 = Fail 0 = Pass
0	BIST_0	---	RO	Memory 0 BIST Status for receive packet memory 1 = Fail 0 = Pass

5.3.2 Switch Reset Register (211H)

Bit	Name	ROM	Default	Description
15:3	RESERVED	---	P0,RO	Reserved
2	PD_ANLG	---	P0,RW	Power down all analog PHY 1 = Power Down 0 = Power On
1	RST_ANLG	---	P0,R/WC	Analog PHY Core Reset Write 1 to reset, and auto-clear after 10us
0	RST_SW	---	P0,R/WC	Switch Core Reset Write 1 to reset, and auto-clear after 10us

5.3.3 Switch Control Register Register (212H)

Bit	Name	ROM	Default	Description
15:12	RESERVED	18[15]	P0,RO	Reserved
11:8	TRUNK_EN	18[11:8]	PSE0, RW	Trunk Enable {P3,P2,P1,P0} [11] 1 = Port3 trunk is enabled 0 = Port3 trunk is disabled [10] 1 = Port2 trunk is enabled 0 = Port2 trunk is disabled [9] 1 = Port1 trunk is enabled 0 = Port1 trunk is disabled [8] 1 = Port0 trunk is enabled 0 = Port0 trunk is disabled
7:5	RESERVED	---	P0,RO	Reserved
4	NO_REG	18[4]	PE0,RW	NO Initial of Register in Software Reset 1 = no initial of register in software reset command. 0 = initial of registers in software reset command
3	AUTO_RST	18[3]	PE0,RW	Disable RV Buffer Count Checking 1 = disable checking (for testing only) 0 = auto switch reset if per port's RV buffer error RV buffer count > 31 and not changed for 40ms.
2	DIS_CRCC	18[2]	PSE0,RW	CRC Checking Disable 1 = CRC checking is disabled 0 = CRC checking is enabled
1:0	RESERVED	---	P0,RO	Reserved

5.3.4 CPU Port & Mirror Control Register (213H)

Bit	Name	ROM	Default	Description
15:11	RESERVED	----	P0,RO	Reserved
10	MIRR_PAIR	19[10]	PSE0,RW	Mirror RX/TX Pair Mode Enable 1 = Enable 0 = Disable
7	STAG_TXE	19[7]	PSE0,RW	Special Tag Transmit Enable 1 = Identifies the Special Tag for outgoing packets 0 = Doesn't insert the Special Tag for outgoing packets
9:8	RESERVED	----	P0,RO	Reserved
6	STAG_RXE	19[6]	PSE0,RW	Special Tag Receive Enable 1 = Identifies the Special Tag for incoming packets 0 = Doesn't identify the Special Tag for incoming packets
5:3	SNF_PORT	19[5:3]	PSE0,RW	Sniffer Port Number 000 = Sniffer Port is Port 0 001 = Sniffer Port is Port 1 010 = Sniffer Port is Port 2 011 = Sniffer Port is Port 3 100 = Sniffer Port is Port 4 101 = Sniffer Port is Port 5 110 = Reserved 111 = Reserved
2:0	CPU_PORT	19[2:0]	PE5,RW	Select CPU Port Number 000 = Port 0 001 = Port 1 010 = Port 2 011 = Port 3 100 = Port 4 101 = Port 5 110 = Port 5 111 = Port 5

5.3.5 Special Tag Ether-Type Register (214H)

Bit	Name	ROM	Default	Description
15:0	STAG_ETH	20[15:0]	PSE,8606 H,RW	Special Tag Ether-Type

5.3.6 Global Learning & Aging Control Register (215H)

Bit	Name	ROM	Default	Description
15:6	RESERVED	---	P0,RO	Reserved
5	LRN_PAUSE	21[5]	PSE0,RW	Learn PAUSE Frame 1 = Enable 0 = Disable
4	LRN_VLAN	21[4]	PSE0,RW	Address Learning Consider VLAN Member 1 = Address learning is disable, if incoming port doesn't exist in its member set. 0 = Address learning despite VLAN member
3	ATB_KEY	21[3]	PSE0,RW	Address Table Hash Key 1 = Use (DMAC+FID) for searching and (SMAC+FID) for learning Note: Must clear address table after this bit is changed. 0 = Use (DMAC) for searching and (SMAC) for learning
2	ATB_MODE	21[2]	PSE0,RW	Address Table Mode 1 = Separated mode, 1K for unicast and 1K for multicast Note: Must clear address table after this bit is changed. 0 = Mixed mode, 2K address table for unicast or multicast
1:0	AGE_TIME	21[1:0]	PSE0,RW	Aging Time Value 00 = 512 sec ±256 sec 01 = 256 sec ±128 sec 10 = 128 sec ± 64 sec 11 = 64 sec ± 32 sec

5.3.7 VLAN Priority Map Register (217H)

Bit	Name	ROM	Default	Description
15:14	VLAN_PM7	28[15:14]	PSE3,RW	When VLAN tag priority value = 07H, the VLAN priority is mapping to these two bits.
13:12	VLAN_PM6	28[13:12]	PSE3,RW	When VLAN tag priority value = 06H, the VLAN priority is mapping to these two bits.
11:10	VLAN_PM5	28[11:10]	PSE2,RW	When VLAN tag priority value = 05H, the VLAN priority is mapping to these two bits.
9:8	VLAN_PM4	28[9:8]	PSE2,RW	When VLAN tag priority value = 04H, the VLAN priority is mapping to these two bits.
7:6	VLAN_PM3	28[7:6]	PSE1,RW	When VLAN tag priority value = 03H, the VLAN priority is mapping to these two bits.
5:4	VLAN_PM2	28[5:4]	PSE1,RW	When VLAN tag priority value = 02H, the VLAN priority is mapping to these two bits.
3:2	VLAN_PM1	28[3:2]	PSE0,RW	When VLAN tag priority value = 01H, the VLAN priority is mapping to these two bits.
1:0	VLAN_PM0	28[1:0]	PSE0,RW	When VLAN tag priority value = 00H, the VLAN priority is mapping to these two bits.

5.3.8 TOS Priority Map 0 Register (218H)

If register 23EH bit 7 is set, for register 218H decode full TOS[5:0]; Otherwise decode TOS[2:0].
For registers 219H ~ 21FH full TOS[5:0] is decoded.

Bit	Name	ROM	Default	Description
15:14	TOS_PM07	29[15:14]	PSE0,RW	TOS value = 07H
13:12	TOS_PM06	29[13:12]	PSE0,RW	TOS value = 06H
11:10	TOS_PM05	29[11:10]	PSE0,RW	TOS value = 05H
9:8	TOS_PM04	29[9:8]	PSE0,RW	TOS value = 04H
7:6	TOS_PM03	29[7:6]	PSE0,RW	TOS value = 03H
5:4	TOS_PM02	29[5:4]	PSE0,RW	TOS value = 02H
3:2	TOS_PM01	29[3:2]	PSE0,RW	TOS value = 01H
1:0	TOS_PM00	29[1:0]	PSE0,RW	TOS value = 00H

5.3.9 TOS Priority Map 1 Register (219H)

Bit	Name	ROM	Default	Description
15:14	TOS_PM0F	30[15:14]	PSE0,RW	TOS value = 0FH
13:12	TOS_PM0E	30[13:12]	PSE0,RW	TOS value = 0EH
11:10	TOS_PM0D	30[11:10]	PSE0,RW	TOS value = 0DH
9:8	TOS_PM0C	30[9:8]	PSE0,RW	TOS value = 0CH
7:6	TOS_PM0B	30[7:6]	PSE0,RW	TOS value = 0BH
5:4	TOS_PM0A	30[5:4]	PSE0,RW	TOS value = 0AH
3:2	TOS_PM09	30[3:2]	PSE0,RW	TOS value = 09H
1:0	TOS_PM08	30[1:0]	PSE0,RW	TOS value = 08H

5.3.10 TOS Priority Map 2 Register (21AH)

Bit	Name	ROM	Default	Description
15:14	TOS_PM17	31[15:14]	PSE1,RW	TOS value = 17H
13:12	TOS_PM16	31[13:12]	PSE1,RW	TOS value = 16H
11:10	TOS_PM15	31[11:10]	PSE1,RW	TOS value = 15H
9:8	TOS_PM14	31[9:8]	PSE1,RW	TOS value = 14H
7:6	TOS_PM13	31[7:6]	PSE1,RW	TOS value = 13H
5:4	TOS_PM12	31[5:4]	PSE1,RW	TOS value = 12H
3:2	TOS_PM11	31[3:2]	PSE1,RW	TOS value = 11H
1:0	TOS_PM10	31[1:0]	PSE1,RW	TOS value = 10H

5.3.11 TOS Priority Map 3 Register (21BH)

Bit	Name	ROM	Default	Description
15:14	TOS_PM1F	32[15:14]	PSE1,RW	TOS value = 1FH
13:12	TOS_PM1E	32[13:12]	PSE1,RW	TOS value = 1EH
11:10	TOS_PM1D	32[11:10]	PSE1,RW	TOS value = 1DH
9:8	TOS_PM1C	32[9:8]	PSE1,RW	TOS value = 1CH
7:6	TOS_PM1B	32[7:6]	PSE1,RW	TOS value = 1BH
5:4	TOS_PM1A	32[5:4]	PSE1,RW	TOS value = 1AH
3:2	TOS_PM19	32[3:2]	PSE1,RW	TOS value = 19H
1:0	TOS_PM18	32[1:0]	PSE1,RW	TOS value = 18H

5.3.12 TOS Priority Map 4 Register (21CH)

Bit	Name	ROM	Default	Description
15:14	TOS_PM27	33[15:14]	PSE2,RW	TOS value = 27H
13:12	TOS_PM26	33[13:12]	PSE2,RW	TOS value = 26H
11:10	TOS_PM25	33[11:10]	PSE2,RW	TOS value = 25H
9:8	TOS_PM24	33[9:8]	PSE2,RW	TOS value = 24H
7:6	TOS_PM23	33[7:6]	PSE2,RW	TOS value = 23H
5:4	TOS_PM22	33[5:4]	PSE2,RW	TOS value = 22H
3:2	TOS_PM21	33[3:2]	PSE2,RW	TOS value = 21H
1:0	TOS_PM20	33[1:0]	PSE2,RW	TOS value = 20H

5.3.13 TOS Priority Map 5 Register (21DH)

Bit	Name	ROM	Default	Description
15:14	TOS_PM2F	34[15:14]	PSE2,RW	TOS value = 2FH
13:12	TOS_PM2E	34[13:12]	PSE2,RW	TOS value = 2EH
11:10	TOS_PM2D	34[11:10]	PSE2,RW	TOS value = 2DH
9:8	TOS_PM2C	34[9:8]	PSE2,RW	TOS value = 2CH
7:6	TOS_PM2B	34[7:6]	PSE2,RW	TOS value = 2BH
5:4	TOS_PM2A	34[5:4]	PSE2,RW	TOS value = 2AH
3:2	TOS_PM29	34[3:2]	PSE2,RW	TOS value = 29H
1:0	TOS_PM28	34[1:0]	PSE2,RW	TOS value = 28H

5.3.14 TOS Priority Map 6 Register (21EH)

Bit	Name	ROM	Default	Description
15:14	TOS_PM37	35[15:14]	PSE3,RW	TOS value = 37H
13:12	TOS_PM36	35[13:12]	PSE3,RW	TOS value = 36H
11:10	TOS_PM35	35[11:10]	PSE3,RW	TOS value = 35H
9:8	TOS_PM34	35[9:8]	PSE3,RW	TOS value = 34H
7:6	TOS_PM33	35[7:6]	PSE3,RW	TOS value = 33H
5:4	TOS_PM32	35[5:4]	PSE3,RW	TOS value = 32H
3:2	TOS_PM31	35[3:2]	PSE3,RW	TOS value = 31H
1:0	TOS_PM30	35[1:0]	PSE3,RW	TOS value = 30H

5.3.15 TOS Priority Map 7 Register (21FH)

Bit	Name	ROM	Default	Description
15:14	TOS_PM3F	36[15:14]	PSE3,RW	TOS value = 3FH
13:12	TOS_PM3E	36[13:12]	PSE3,RW	TOS value = 3EH
11:10	TOS_PM3D	36[11:10]	PSE3,RW	TOS value = 3DH
9:8	TOS_PM3C	36[9:8]	PSE3,RW	TOS value = 3CH
7:6	TOS_PM3B	36[7:6]	PSE3,RW	TOS value = 3BH
5:4	TOS_PM3A	36[5:4]	PSE3,RW	TOS value = 3AH
3:2	TOS_PM39	36[3:2]	PSE3,RW	TOS value = 39H
1:0	TOS_PM38	36[1:0]	PSE3,RW	TOS value = 38H

5.3.16 MIB Counter Disable Register (230H)

Bit	Name	ROM	Default	Description
15:8	RESERVED	---	P0,RO	Reserved
7:6	RESERVED	---	P0,RO	Reserved
5:0	MIB_DIS	22[5:0]	PSE0,RW	Per-Port MIB Counter Disable [5] 1 = Port5 MIB counter is disabled 0 = Port5 MIB counter is enabled [4] 1 = Port4 MIB counter is disabled 0 = Port4 MIB counter is enabled [3] 1 = Port3 MIB counter is disabled 0 = Port3 MIB counter is enabled [2] 1 = Port2 MIB counter is disabled 0 = Port2 MIB counter is enabled [1] 1 = Port1 MIB counter is disabled 0 = Port1 MIB counter is enabled [0] 1 = Port0 MIB counter is disabled 0 = Port0 MIB counter is enabled

5.3.17 MIB Counter Control Register (231H)

Bit	Name	ROM	Default	Description
15	MIB_READY	---	PS0,RO	Counter Data is Ready
14:10	RESERVED	---	P0,RO	Reserved
9:8	MIB_CMD	---	PS0,RW	MIB Command 00 = Read & Clear 01 = Read only 10 = Clear MIB counters of port 11 = Clear MIB counters of all ports
7:5	MIB_PORT	---	PS0,RW	Port Index (0~5)
4:0	MIB_OFSET	---	PS0,RW	Counter Offset (0~9)

MIB counter offset 00H: RX Byte Counter Register
MIB counter offset 01H: RX Uni-cast Packet Counter Register
MIB counter offset 02H: RX Multi-cast Packet Counter Register
MIB counter offset 03H: RX Discard Packet Counter Register
MIB counter offset 04H: RX Error Packet Counter Register
MIB counter offset 05H: TX Byte Counter Register
MIB counter offset 06H: TX Uni-cast Packet Counter Register
MIB counter offset 07H: TX Multi-cast Packet Counter Register
MIB counter offset 08H: TX Discard Packet Counter Register
MIB counter offset 09H: TX Error Packet Counter Register

5.3.18 MIB Counter Data Low Register (232H)

Bit	Name	ROM	Default	Description
15:0	MIB_DL	---	PS0,RW	Counter Data Low (Bit 15:00)

5.3.19 MIB Counter Data High Register (233H)

Bit	Name	ROM	Default	Description
15:0	MIB_DH	---	PS0,RW	Counter Data High (Bit 31:16)

5.3.20 QinQ TPID Register (23DH)

Bit	Name	ROM	Default	Description
15:0	QinQ_TPID	48[15:0]	PSE88A8 H,RW	QinQ Tag Protocol Identifier For VLAN stacking function

5.3.21 VLAN Mode and Rule Control Register (23EH)

Bit	Name	ROM	Default	Description
15	FIR_VIDFFF	49[15]	PSE0,RW	Enable to drop Pakcet with VID==FFFH 1 = Enable 0 = Disable
14	FIR_CFI	49[14]	PSE0,RW	Enable to drop Pakcet with Nonzero CFI Drop incoming packet, if the CFI field is not equal to zero. 1 = Enable 0 = Disable
13:12	RESERVED	---	P0,RO	Reserved
11:9	RESERVED	---	P0,RO	Reserved
8	QINQ_EN	49[8]	PSE0,RW	VLAN Stacking Enable (QinQ) 1 = Enable 0 = Disable
7	TOS6	49[7]	PE0,RW	Full IP ToS Field for Priority Queue 1 = check most significant 6-bit of TOS 0 = check most significant 3-bit only of TOS
6	RESERVED	---	P0,RO	Reserved
5	UNICAST	49[5]	PE0,RW	Unicast packet can across VLAN boundary 1 = Enable 0 = Disable
4	VLAN_RFFF	49[4]	PSE0,RW	Replace VIDFFF with PVID Enable Replace VID field of VLAN tag with PVID, if VID is FFFH 1 = Enable 0 = Disable
3	VLAN_RVD1	49[3]	PSE0,RW	Replace VID1 with PVID Enable Replace VID field of VLAN tag with PVID, if VID is 001H 1 = Enable 0 = Disable
2	VLAN_RVD0	49[2]	PSE0,RW	Replace VID0 with PVID Enable Replace VID field of VLAN tag with PVID, if VID is 000H 1 = Enable 0 = Disable
1	VLAN_RPRI	49[1]	PSE0,RW	Replace Priority Enable Replace priority field of VLAN tag with PPRI 1 = Enable 0 = Disable
0	VLAN_MOD	49[0]	PSE0,RW	VLAN_MODE 1 = Tag-based VLAN 0 = Port-based VLAN

5.3.22 VLAN Table - Valid Control Register (23FH)

Bit	Name	ROM	Default	Description
15:0	VTAB_VALD	50[15:0]	PSE,01H, RW	Entry Vailid Bits in VLAN Table There are 16 entries in VLAN Table, VTAB_VALID indicate which entries are valid 1 = Valid 0 = Invalid

5.3.23 VLAN Table - ID_0H Register (250H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID0	51[15:12]	PSE0,RW	FID of Entry 0H in VLAN Table
11:00	VTAB_VID0	51[11:00]	PSE1,RW	VID of Entry 0H in VLAN Table

5.3.24 VLAN Table - ID_1H Register (251H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID1	52[15:12]	PSE0,RW	FID of Entry 1H in VLAN Table
11:00	VTAB_VID1	52[11:00]	PSE0,RW	VID of Entry 1H in VLAN Table

5.3.25 VLAN Table - ID_2H Register (252H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID2	53[15:12]	PSE0,RW	FID of Entry 2H in VLAN Table
11:00	VTAB_VID2	53[11:00]	PSE0,RW	VID of Entry 2H in VLAN Table

5.3.26 VLAN Table - ID_3H Register (253H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID3	54[15:12]	PSE0,RW	FID of Entry 3H in VLAN Table
11:00	VTAB_VID3	54[11:00]	PSE0,RW	VID of Entry 3H in VLAN Table

5.3.27 VLAN Table - ID_4H Register (254H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID4	55[15:12]	PSE0,RW	FID of Entry 4H in VLAN Table
11:00	VTAB_VID4	55[11:0]	PSE0,RW	VID of Entry 4H in VLAN Table

5.3.28 VLAN Table - ID_5H Register (255H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID5	56[15:12]	PSE0,RW	FID of Entry 5H in VLAN Table
11:00	VTAB_VID5	56[11:0]	PSE0,RW	VID of Entry 5H in VLAN Table

5.3.29 VLAN Table - ID_6H Register (256H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID6	57[15:12]	PSE0,RW	FID of Entry 6H in VLAN Table
11:00	VTAB_VID6	57[11:0]	PSE0,RW	VID of Entry 6H in VLAN Table

5.3.30 VLAN Table - ID_7H Register (257H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID7	58[15:12]	PSE0,RW	FID of Entry 7H in VLAN Table
11:00	VTAB_VID7	58[11:0]	PSE0,RW	VID of Entry 7H in VLAN Table

5.3.31 VLAN Table - ID_8H Register (258H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID8	59[15:12]	PSE0,RW	FID of Entry 8H in VLAN Table
11:00	VTAB_VID8	59[11:0]	PSE0,RW	VID of Entry 8H in VLAN Table

5.3.32 VLAN Table - ID_9H Register (259H)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID9	60[15:12]	PSE0,RW	FID of Entry 9H in VLAN Table
11:00	VTAB_VID9	60[11:0]	PSE0,RW	VID of Entry 9H in VLAN Table

5.3.33 VLAN Table - ID_AH Register (25AH)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDA	61[15:12]	PSE0,RW	FID of Entry AH in VLAN Table
11:00	VTAB_VIDA	61[11:0]	PSE0,RW	VID of Entry AH in VLAN Table

5.3.34 VLAN Table - ID_BH Register (25BH)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDB	62[15:12]	PSE0,RW	FID of Entry BH in VLAN Table
11:00	VTAB_VIDB	62[11:0]	PSE0,RW	VID of Entry BH in VLAN Table

5.3.35 VLAN Table - ID_CH Register (25CH)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDC	63[15:12]	PSE0,RW	FID of Entry CH in VLAN Table
11:00	VTAB_VIDC	63[11:0]	PSE0,RW	VID of Entry CH in VLAN Table

5.3.36 VLAN Table - ID_DH Register (25DH)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDD	64[15:12]	PSE0,RW	FID of Entry DH in VLAN Table
11:00	VTAB_VIDD	64[11:0]	PSE0,RW	VID of Entry DH in VLAN Table

5.3.37 VLAN Table - ID_EH Register (25EH)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDE	65[15:12]	PSE0,RW	FID of Entry EH in VLAN Table
11:00	VTAB_VIDE	65[11:0]	PSE0,RW	VID of Entry EH in VLAN Table

5.3.38 VLAN Table - ID_FH Register (25FH)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDF	66[15:12]	PSE0,RW	FID of Entry FH in VLAN Table
11:00	VTAB_VIDF	66[11:0]	PSE0,RW	VID of Entry FH in VLAN Table

5.3.39 VLAN Table - MEMBER_0H Register (270H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM0	67[13:8]	PSE0,RW	VLAN Entry 0H Tagged Member The content of 250H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM0	67[5:0]	PSE,3FH, RW	VLAN Entry 0H VLAN Member

5.3.40 VLAN Table - MEMBER_1H Register (271H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM1	68[13:8]	PSE0,RW	VLAN Entry 1H Tagged Member The content of 251H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM1	68[5:0]	PSE0,RW	VLAN Entry 1HVLAN Member

5.3.41 VLAN Table - MEMBER_2H Register (272H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM2	69[13:8]	PSE0,RW	VLAN Entry 2H Tagged Member The content of 252H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM2	69[5:0]	PSE0,RW	VLAN Entry 2H VLAN Member

5.3.42 VLAN Table - MEMBER_3H Register (273H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM3	70[13:8]	PSE0,RW	VLAN Entry 3H Tagged Member The content of 253H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets.
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM3	70[5:0]	PSE0,RW	VLAN Entry 3H VLAN Member

5.3.43 VLAN Table - MEMBER_4H Register (274H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM4	71[13:8]	PSE0,RW	VLAN Entry 4H Tagged Member The content of 254H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM4	71[5:0]	PSE0,RW	VLAN Entry 4H VLAN Member

5.3.44 VLAN Table - MEMBER_5H Register (275H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM5	72[13:8]	PSE0,RW	VLAN Entry 5H Tagged Member The content of 255H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM5	72[5:0]	PSE0,RW	VLAN Entry 5H VLAN Member

5.3.45 VLAN Table - MEMBER_6H Register (276H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM6	73[13:8]	PSE0,RW	VLAN Entry 6H Tagged Member The content of 256H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM6	73[5:0]	PSE0,RW	VLAN Entry 6H VLAN Member

5.3.46 VLAN Table - MEMBER_7H Register (277H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM7	74[13:8]	PSE0,RW	VLAN Entry 7H Tagged Member The content of 257H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM7	74[5:0]	PSE0,RW	VLAN Entry 7H VLAN Member

5.3.47 VLAN Table - MEMBER_7H Register (277H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM8	75[13:8]	PSE0,RW	VLAN Entry 8H Tagged Member The content of 258H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets.
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM8	75[5:0]	PSE0,RW	VLAN Entry 8H VLAN Member

5.3.48 VLAN Table - MEMBER_9H Register (279H)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TM9	76[13:8]	PSE0,RW	VLAN Entry 9H Tagged Member The content of 259H.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VM9	76[5:0]	PSE0,RW	VLAN Entry 9H VLAN Member

5.3.49 VLAN Table - MEMBER_AH Register (27AH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TMA	77[13:8]	PSE0,RW	VLAN Entry 0AH Tagged Member The content of 25AH.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VMA	77[5:0]	PSE0,RW	VLAN Entry 0AH VLAN Member

5.3.50 VLAN Table - MEMBER_BH Register (27BH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TMB	78[13:8]	PSE0,RW	VLAN Entry 0BH Tagged Member The content of 25BH.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VMB	78[5:0]	PSE0,RW	VLAN Entry 0BH VLAN Member

5.3.51 VLAN Table - MEMBER_CH Register (27CH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TMC	79[13:8]	PSE0,RW	VLAN Entry 0CH Tagged Member The content of 25CH.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VMC	79[5:0]	PSE0,RW	VLAN Entry 0CH VLAN Member

5.3.52 VLAN Table - MEMBER_DH Register (27DH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TMD	80[13:8]	PSE0,RW	VLAN Entry 0DH Tagged Member The content of 25DH.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VMD	80[5:0]	PSE0,RW	VLAN Entry 0DH VLAN Member

5.3.53 VLAN Table - MEMBER_EH Register (27EH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TME	81[13:8]	PSE0,RW	VLAN Entry 0EH Tagged Member The content of 25EH.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VME	81[5:0]	PSE0,RW	VLAN Entry 0EH VLAN Member

5.3.54 VLAN Table - MEMBER_FH Register (27FH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	VTAB_TMF	82[13:8]	PSE0,RW	VLAN Entry 0FH Tagged Member The content of 25FH.[11:0] equal to VID field of a tagged frame which be received . The mapping ports of this field is the direction of forwarding packets .
7:6	RESERVED	---	P0,RO	Reserved
5:0	VTAB_VMF	82[5:0]	PSE0,RW	VLAN Entry 0FH VLAN Member

5.3.55 VLAN Table - Priority Enable Register (290H)

Bit	Name	ROM	Default	Description
15:0	VTAB_PEN	83[15:0]	PSE0,RW	Priority Enable Bits in VLAN Table Assign VLAN priority queue number from VLAN table (293H~299H) field VTAB_QUE_0~F to be transmit queue number. 1 = Enable 0 = Disable

5.3.56 VLAN Table - STP Index Enable Register (292H)

Bit	Name	ROM	Default	Description
15:0	VTAB_STPE	85[15:0]	PSE0,RW	Spanning Tree Protocol I VLAN Table To enable the STP function of the ports from VLAN table 1 = Enable 0 = Disable

5.3.57 VLAN Table - Misc_0 Register (293H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	86[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUE1	86[9:8]	PSE0,RW	VLAN Entry 1H, Priority Queue Number
7:2	RESERVED	86[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUE0	86[1:0]	PSE0,RW	VLAN Entry 0H, Priority Queue Number

5.3.58 VLAN Table - Misc_1 Register (294H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	87[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUE3	87[9:8]	PSE0,RW	VLAN Entry 3H, Priority Queue Number
7:2	RESERVED	87[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUE2	87[1:0]	PSE0,RW	VLAN Entry 2H, Priority Queue Number

5.3.59 VLAN Table - Misc_2 Register (295H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	88[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUE5	88[9:8]	PSE0,RW	VLAN Entry 5H, Priority Queue Number
7:2	RESERVED	88[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUE4	88[1:0]	PSE0,RW	VLAN Entry 4H, Priority Queue Number

5.3.60 VLAN Table - Misc_3 Register (296H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	89[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUE7	89[9:8]	PSE0,RW	VLAN Entry 7H, Priority Queue Number
7:2	RESERVED	89[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUE6	89[1:0]	PSE0,RW	VLAN Entry 6H, Priority Queue Number

5.3.61 VLAN Table - Misc_4 Register (297H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	90[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUE9	90[9:8]	PSE0,RW	VLAN Entry 9H, Priority Queue Number
7:2	RESERVED	90[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUE8	90[1:0]	PSE0,RW	VLAN Entry 8H, Priority Queue Number

5.3.62 VLAN Table - Misc_5 Register (298H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	91[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUB	91[9:8]	PSE0,RW	VLAN Entry 0BH, Priority Queue Number
7:2	RESERVED	91[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUA	91[1:0]	PSE0,RW	VLAN Entry 0AH, Priority Queue Number

5.3.63 VLAN Table - Misc_6 Register (299H)

Bit	Name	ROM	Default	Description
15:10	RESERVED	92[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUD	92[9:8]	PSE0,RW	VLAN Entry 0DH, Priority Queue Number
7:2	RESERVED	92[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUC	92[1:0]	PSE0,RW	VLAN Entry 0CH, Priority Queue Number

5.3.64 VLAN Table - Misc_7 Register (29AH)

Bit	Name	ROM	Default	Description
15:10	RESERVED	93[15:10]	PSE0,RW	Reserved
9:8	VTAB_QUF	93[9:8]	PSE0,RW	VLAN Entry 0FH, Priority Queue Number
7:2	RESERVED	93[6:2]	PSE0,RW	Reserved
1:0	VTAB_QUE	93[1:0]	PSE0,RW	VLAN Entry 0EH, Priority Queue Number

5.3.65 Snooping Control 0 Register (29BH)

Bit	Name	ROM	Default	Description
15:14	RESERVED	---	P0,RO	Reserved
13:8	RPP	23[13:8]	PSE0,RW	Router Port Portmap Bit8 = Port 0 Bit9 = Port 1 Bit10 = Port 2 Bit11 = Port 3 Bit12 = Port 4 Bit13 = Port 5
7	UD_RP	23[7]	PSE0,RW	User-defined Router Port Enable
6	RESERVED	---	P0,RO	Reserved
5:4	MC_CTRL	23[5:4]	PSE0,RW	Multicast Control Packet Handle 00 = Forward Membership Reports to router port. General Query to all port. 01 = Mirror to CPU (Forward to CPU also) 10 = Trap to CPU (Forward to CPU only) 11 = Flood
3:2	UMD_CTRL	23[3:2]	PSE0,RW	Unregistered Multicast Data Packet Handle 00 = As normal multicast packets 01 = Dropped. 10 = Trap to CPU 11 = Flood except CPU
1	MLDS_EN	23[1]	PSE0,RW	MLD Snooping Enable 1 = Enable 0 = Disable
0	HIGS_EN	23[0]	PSE0,RW	Hardware IGMP Snooping Enable 1 = Enable 0 = Disable

5.3.66 Snooping Control 1 Register (29CH)

Bit	Name	ROM	Default	Description
15:13	RESERVED	---	P0,RO	Reserved
12	IGS_TODIS	24[12]	PSE0,RW	IGMP Snooping Timeout Scheme Disable 1 = Timeout is disabled 0 = Timeout is enabled
11:10	RP_TV	24[11:10]	PSE0,RW	Router Port Timeout Value Selection 00 = 1 times of Query Interval 01 = 2 times of Query Interval 10 = 3 times of Query Interval (default) 11 = 4 times of Query Interval
9:8	IGS_RV	24[9:8]	PSE0,RW	Robustness Variable 00 = 1 times 01 = 2 times (default) 10 = 3 times 11 = 4 times
7:0	IGS_QI	24[7:0]	PSE7DH, RW	Query Interval Default = 125 (sec)

5.3.67 Address Table Control & Status Register (2B0H)

Bit	Name	ROM	Default	Description
15	ATB_S	---	PS0,RO	Address Table Access is Busy 1 = Busy (Access process is operating) 0 = Available (Access process is completed)
14:13	ATB_CR	---	PS0,RO	Address Table Command Result 00 = Command OK, entry doesn't exist a. Create an new entry (Write Command) b. Do noting (Delete Command) c. not found (Search Command) d. Entry is invalid (Read Command) e. Process is successful (Clear Command) 01 = Command OK, entry is exist a. Overwrite entry (Write Command) b. Delete entry (Delete Command) c. Entry found (Search Command) d. Entry is valid (Read Command) e. Process is successful (Clear Command) 1X = Command Error
12:8	RESERVED	---	P0,RO	Reserved
7	RESERVED	---	P0,RO	Reserved
6	ATB_CLSE_FID	---	PS0,RW	Enable to Clear Entries with Specified FID 1 = Enable 0 = Disable
5	ATB_CLSE_PORT	---	PS0,RW	Enable to Clear Entries with Specified Port Number or Port Map (Port number for accessing unicast address table, port map for multicast) 1 = Enable 0 = Disable
4:2	ATB_CMD	---	PS0,RW	Command 000 = Read a entry with sequence number of address table 001 = Write a entry with MAC address 010 = Delete a entry with MAC address 011 = Search a entry with MAC address 100 = Clear one or more than one entries with Port or FID 101,110,111 = Reserved
1:0	ATB_IDX	---	PS0,RW	Address Table Index 00 = Unicast Address Table 01 = Multicast Address Table 10 = IGMP Table 11 = Reserved

5.3.68 Address Table Data 0 Register (2B1H)

Bit	Name	ROM	Default	Description
15:12	RESERVED	---	P0,RO	Reserved
11:8	ATB_FID	---	PS0,RW	FID Value
7:6	RESERVED	---	P0,RO	Reserved
5:0	ATB_PORT	---	PS0,RW	Address Table Port Number or Port Map

5.3.69 Address Table Data 1 Register (2B2H)

Bit	Name	ROM	Default	Description
15:0	ATB_DW1	---	PSE0,RW	Address Table Data Word 1

5.3.70 Address Table Data 2 Register (2B3H)

Bit	Name	ROM	Default	Description
15:0	ATB_DW2	---	PSE0,RW	Address Table Data Word 2

5.3.71 Address Table Data 3 Register (2B4H)

Bit	Name	ROM	Default	Description
15:0	ATB_DW3	---	PSE0,RW	Address Table Data Word 3

5.3.72 Address Table Data 4 Register (2B5H)

Bit	Name	ROM	Default	Description
15:0	ATB_DW4	---	PSE0,RW	Address Table Data Word 4

5.4 Chip Control and Status Registers (300H~3FFH)

5.4.1 Vendor ID Register (310H)

Bit	Name	ROM	Default	Description
15:0	VID	4[15:0]	PE,0A46H ,RO	Vendor ID

5.4.2 Product ID Register (311H)

Bit	Name	ROM	Default	Description
15:0	PID	5[15:0]	PE,8606H, RO	Product ID

5.4.3 Chip Revision ID Register (312H)

Bit	Name	ROM	Default	Description
15:0	CHIPR	----	P0,RO	Chip Revision

5.4.4 Port 4 MAC Control Register (314H)

Bit	Name	ROM	Default	Description
15:12	RESERVED	---	P0,RO	Reserved
11,10	P4_TB_SEL	12[11:10]	PE00, RW	Port4 turbo speed in RevMII 00 = Default TXCLK 25MHz(100M)/2.5MHz(10M) 01 = P4 RevMII TXCLK generate 50MHz clock 10 = P4 RevMII TXCLK generate 100MHz clock 11 = P4 RevMII TXCLK generate 125MHz clock
9:8	P4_DRIVE	12[9:8]	PE01,RW	Port 4 output pin Current Driving/Sinking Capability 00 = 2mA 01 = 4mA (default) 10 = 6mA 11 = 8mA
7	P4_SLEW	12[7]	PET0,RW	Port 4 output pin slew rate 1 = low slew rate 0 = normal slew rate
6	P4_50M_IN	12[6]	PE0,RW	When Port4 be configured as RMII/TP RMII 1 = 50MHz clock source from internal chip 0 = 50MHz clock source from pin
5	P4_50MOUT	12[5]	PE0,RW	When Port4 be configured as RMII/TPRMII 1 = Output 50MHz clock 0 = Disable as High impedance
4	RESERVED	---	P0,RO	Reserved
3	P4_MODE	12[3]	PET0,RW	Port4 in auto-negotiation mode for MII/RevMII/RMII 1 = force mode 0 = auto-negotiation mode
2	P4_LINK	12[2]	PET0,RW	When Port4 in force mode for MII/RevMII/RMII 1 = link OFF 0 = link ON
1	P4_DPX	12[1]	PET0,RW	When Port4 in force mode for MII/RevMII/RMII 1 = Half-duplex mode 0 = Full-duplex mode
0	P4_SPEED	12[0]	PET0,RW	When Port4 in force mode for MII/RevMII/RMII 1 = 10M mode 0 = 100M mode

5.4.5 Port 5 MAC Control Register (315H)

Bit	Name	ROM	Default	Description
15	Reserved	13[15]	PE1,RW	Reserved
14	Reserved	13[14]	PET0,RW	Reserved
13	Reserved	13[13]	PET0,RW	Reserved
12	Reserved	13[12]	PET0,RW	Reserved
11	Reserved	13[11]	PET0,RW	Reserved
10	Reserved	---	P0,RO	Reserved
9,8	P5_DRIVE	13[9:8]	PE01,RW	Port 5 output pin Current Driving/Sinking Capability 00 = 2mA 01 = 4mA (default) 10 = 6mA 11 = 8mA
7	P5_SLEW	13[7]	PE0,RW	Port 5 output pin slew rate 1 = low slew rate 0 = normal slew rate
6	P5_50M_IN	13[6]	PE0,RW	When Port5 be configured as RMII 1 = 50MHz clock source from internal chip 0 = 50MHz clock source from pin
5	P5_50M_OUT	13[5]	PE0,RW	When Port5 be configured as RMII 1 = Output 50MHz clock 0 = Disable as High impedance
4	Reserved	---	P0,RO	Reserved
3	P5_MODE	13[3]	PET0,RW	When Port5 in MII/RevMII/RMII 1 = force mode 0 = auto-negotiation mode
2	P5_LINK	13[2]	PET0,RW	When Port5 in force mode 1 = link OFF 0 = link ON
1	P5_DPX	13[1]	PET0,RW	When Port5 in force mode 1 = Half-duplex mode 0 = Full-duplex mode
0	P5_SPEED	13[0]	PET0,RW	When Port5 in force mode 1 = 10M mode 0 = 100M mode

5.4.6 LED Control Register (317H)

Bit	Name	ROM	Default	Description
15	IRQ_PIN	6[15]	PSE0,RW	Output Mode of INTR Pin 1 = Open-collected mode 0 = Direct output mode
14	IRQ_POL	6[14]	PSE,0,RW	Polarity Mode of INTR Pin 1 = Active low 0 = Active high
13	RESERVED	---	P0,RO	Reserved
12,11	CTL_DRIVE	6[12:11]	PET01,RW	Switch Control output pin Current Driving/Sinking Capability 00 = 2mA 01 = 4mA (default) 10 = 6mA 11 = 8mA
10	CTL_SLEW	6[10]	PE0,RW	Switch Control output pin slew rate 1 = low slew rate 0 = normal slew rate
9,8	LED_DRIVE	6[9:8]	PE01,RW	LED pin Current Driving/Sinking Capability 00 = 2mA 01 = 4mA 10 = 6mA (default) 11 = 8mA
7	LED_SLEW	6[7]	PE1,RW	LED pin slew rate 1 = low slew rate 0 = normal slew rate
6:2	RESERVED	---	P0,RO	Reserved
1:0	LED_CR	6[1:0]	PE3,RW	LED mode select 00 = LED mode 0 01 = LED mode 1 ,dual color mode 10 = LED mode 2 , 11 = LED mode 3 (default)

5.4.7 Interrupt Status Register (318H)

Bit	Name	ROM	Default	Description
15:4	RESERVED	---	P0,RO	Reserved
0	LNKCHG	---	PS0, RW/C1	Link Status Change

5.4.8 Interrupt Mask & Control Register (319H)

Bit	Name	ROM	Default	Description
15:4	RESERVED	---	P0,RO	Reserved
0	LNKCHG	---	PS0,RW	Enable Link Status Change Interrupt

5.4.9 EEPROM Control & Address Register (31AH)

Bit	Name	ROM	Default	Description
15:8	EROA	---	PS0,RW	EEPROM Word Address
7	RESERVED	---	P0,RO	Reserved
6	EETYPE	---	0,RO	EEPROM Type 1 = 93C66 / 93C56 0 = 93C46
5	REEP	---	PS0,RW	Reload EEPROM. Write 1 and then write 0 to generate a pulse to active EEPROM reload circuit
4	WEP	---	PS0,RW	Write EEPROM Enable
3	EPOS	---	PS0,RW	External PHY Operation Select When set, Enable access external PHY .
2	ERPRR	---	PS0,RW	EEPROM Read . Driver needs to clear it up after the operation completes.
1	ERPRW	---	PS0,RW	EEPROM Write . Driver needs to clear it up after the operation completes.
0	ERRE	---	PS0,RO	EEPROM Access Status When set, it indicates that the EEPROM or PHY access is in progress When cleared, it indicates that the EEPROM or PHY reload is completed or idle.

5.4.10 EEPROM Data Register (31BH)

Bit	Name	ROM	Default	Description
15:0	EE_DATA	---	PS0,RW	EEPROM 16bit Data

5.4.11 Monitor Register 1 (31CH)

Bit	Name	ROM	Default	Description
15	STRP_DIS	---	RO	Pin 93
14	RESERVED	---	RO	Reserved
13	TEST3	---	RO	Pin 41
12	TEST2	---	RO	Pin 69
11	TEST1	---	RO	Pin 108
10	RESERVED	---	RO	Reserved
9	RESERVED	---	RO	Reserved
8	P2_SPD	---	RO	Pin 103
7	P1_SPD	---	RO	Pin 104
6	P0_SPD	---	RO	Pin 105
5	NC1	---	RO	Pin 106
4	RESERVED	---	RO	Pin 77
3	RESERVED	---	RO	Pin 78
2	EECS	---	RO	Pin 80
1	EECK	---	RO	Pin 81
0	RESERVED	---	RO	Pin 79

5.4.12 Monitor Register 2 (31DH)

Bit	Name	ROM	Default	Description
15	P3_SPD	---	RO	Reserved
14	P4_SPD	---	RO	Reserved
13	RESERVED	---	RO	Reserved
12	P4_FDX	---	RO	Pin 107
11	P3_FDX	---	RO	Pin 110
10	P2_FDX	---	RO	Pin 111
9	P1_FDX	---	RO	Pin 112
8	RESERVED	---	RO	Reserved
7	RESERVED	---	RO	Reserved
6	RESERVED	---	RO	Reserved
5	P4_LNK	---	RO	Pin 51
4	RESERVED	---	RO	Reserved
3	RESERVED	---	RO	Reserved
2	RESERVED	---	RO	Reserved
1	RESERVED	---	RO	Reserved
0	RESERVED	---	RO	Reserved

5.4.13 Monitor Register 3 (31EH)

Bit	Name	ROM	Default	Description
15	P3_LNK	---	RO	Pin 48
14	P2_LNK	---	RO	Pin 47
13	P1_LNK	---	RO	Pin 43
12	P0_LNK	---	RO	Pin 42
11	P4_SET0	---	RO	Pin 98
10	CFG4	---	RO	Pin 62
9	P4_SET1	---	RO	Pin 100
8	RESERVED	---	RO	Reserved
7	RESERVED	---	RO	Reserved
6	RESERVED	---	RO	Reserved
5	NC3	---	RO	Pin 115
4	NC4	---	RO	Pin 117
3	RESERVED	---	RO	Reserved
2	RESERVED	---	RO	Reserved
1	RESERVED	---	RO	Reserved
0	PHY_MDC	---	RO	Pin 68

5.4.14 System Clock Select Register (338H)

Bit	Name	ROM	Default	Description
15:8	RESERVED	---	P0,RO	Reserved
7	RESERVED	---	PS0,RO	Reserved
6:3	RESERVED	---	P0,RO	Reserved
2:0	CLK_TYPE	---	PS0,RW	Select system speed when internal system clock used 000 = 50MHz 001 = 66MHz 010 = 83MHz 011 = 100MHz 1XX = 25MHz

5.4.15 Serial Bus Error Check Register (339H)

Bit	Name	ROM	Default	Description
15:9	RESERVED	---	P0,RO	Reserved
8	SMI_ERR	---	PS0,RO	SMI Bus Error Status(Read only) 1 = Checksum check error 0 = Checksum check correct
7:0	SMI_CSUM	---	PS0,RW	SMI Bus Command Checksum for Error Check Calculated Checksum value by HW

5.4.16 Serial Bus Control Register (33AH)

Bit	Name	ROM	Default	Description
15:1	RESERVED	---	P0,RO	Reserved
0	SMI_ECE	---	PS0,RW	SMI Bus Error Check Enable(Default: 1'b0) 1 = Enable 0 = Disable

5.4.17 Virtual PHY Control Register (33DH)

Bit	Name	ROM	Default	Description
15:13	RESERVED	---	P0,RO	Reserved
12	VPHY_LNK_AND_RD	---	PS0,RO	Read Value of Virtual PHY Link Operation Mode 1 = AND operation 0 = Ignore, no operation
11	VPHY_LNK_OR_RD	---	PS0,RO	Read Value of Virtual PHY Link Operation Mode 1 = OR operation 0 = Ignore, no operation
10	RESERVED	---	P0,RO	Reserved
9	VPHY_LNK_AND_WR	---	P0,WO	Virtual PHY Link Operation Mode 1 = AND operation 0 = Ignore, no operation
8	VPHY_LNK_OR_WR	---	P0,WO	Virtual PHY Link Operation Mode 1 = OR operation 0 = Ignore, no operation
7:6	RESERVED	---	P0,RO	Reserved
5:0	VPHY_MPP	---	PS0,RW	Port Map [05]: Port 5 [04]: Port 4 [03]: Port 3 [02]: Port 2 [01]: Port 1 [00]: Port 0 Note: Valid if Reg33DH.[9] or Reg33DH.[8] is enabled

5.4.18 PHY Control Test Register (33EH)

Bit	Name	ROM	Default	Description
15	AT_MDIX0	7[15]	P0,RW	Port 0 Auto-Mdix Control 1 = OFF 0 = ON
14	AT_MDIX1	7[14]	P0,RW	Port 1 Auto-Mdix Control 1 = OFF 0 = ON
13	AT_MDIX2	7[13]	P0,RW	Port 2 Auto-Mdix Control 1 = OFF 0 = ON
12	AT_MDIX3	7[12]	P0,RW	Port 3 Auto-Mdix Control 1 = OFF 0 = ON
11	AT_MDIX4	7[11]	P0,RW	Port 4 Auto-Mdix Control 1 = OFF 0 = ON
10:0	RESERVED	---	P3,RW	Reserved

6 EEPROM Format

6.1 EEPROM Words 4K (256 x 16)

EEPROM Words 4K (256 x 16)

Name	Word	Description
Signature	0	EEPROM Signature = 1049H This value must be pre-programmed into EEPROM in order for EEPROM auto detection to work
RESERVED	1~2	Reserved, set to ZEROs
Auto Load Control #1	3	Bit [1:0] = 01: Load EEPROM's Vendor ID and Product ID into switch's Vendor ID and Product ID registers Bit [3:2] = 01: Load EEPROM word 6[9:0] into switch's respective registers Bit [5:4] = 01: Load EEPROM word 7 and 8 into switch's respective registers Bit [7:6] = 01: Load EEPROM's PHY ID #1 and PHY ID #2 into switch's respective registers Bit [9:8] = 01: Load EEPROM's Port 4 MAC Control, word 12 and Port 5 MAC Control, word 13, into switch register 314H and 315H, respectively Bit [15:10] = Reserved, set to ZEROs
Vendor ID	4	2 byte Vendor ID, default value in switch register, 310H, is 0A46H and it is overwriten by this word when Auto Load is enabled. This word can be customized to show different ID per application
Product ID	5	2 byte Product ID, default value in switch register, 311H, is 8606H and it is overwriten by this word when Auto Load is enabled. This word can be customized to show different ID per application
Pin control	6	Interrupt Pin Control This word will be loaded into register 317H in its entirety
PHY control	7	Bit [10:0] : Reserved, set ZEROs Bit [11] = Port 4 AUTO-MDIX, 1 = enable, 0 = disable (default = enable) Bit [12] = Port 3 AUTO-MDIX, 1 = enable, 0 = disable (default = enable) Bit [13] = Port 2 AUTO-MDIX, 1 = enable, 0 = disable (default = enable) Bit [14] = Port 1 AUTO-MDIX, 1 = enable, 0 = disable (default = enable) Bit [15] = Port 0 AUTO-MDIX, 1 = enable, 0 = disable (default = enable)
Reserved	8	Reserved, set ZEROs
PHY ID #1	9	This word will be load into Port 0 ~ 4's PHY ID register #1 (042H, 062H, 082H, 0A2H and 0C2H).
PHY ID #2	10	This word will be load into Port 0 ~ 4's PHY ID register #2 (043H, 063H, 083H, 0A3H and 0C3H)
RESERVED	11	Reserved, set ZEROs
Port 4 MAC Control	12	This word will be loaded into Port 4 MAC Control register 314H in its entirety
Port 5 MAC Control	13	This word will be loaded into Port 5 MAC Control register 315H in its entirety
Auto Load Control #2 Switch Chip Control	14	Bit [1:0] = 01: Load EEPROM word 18 ~ 22 for switch status & control Bit [3:2] = 01: Load EEPROM word 23 ~ 24 for IGMP Snooping Control Bit [5:4] = 01: Load EEPROM word 28 ~ 36 for priority mapping Bit [7:6] = Reserved, set ZEROs Bit [9:8] = 01: Load EEPROM word 48 ~ 93 for VLAN setting Bit [15:10] = Reserved, set ZEROs
Auto Load Control #3 Per-Port Control	15	Bit [1:0] = 01: Load EEPROM word 128 ~ 143 for port 0 setting Bit [3:2] = 01: Load EEPROM word 144 ~ 159 for port 1 setting Bit [5:4] = 01: Load EEPROM word 160 ~ 175 for port 2 setting Bit [7:6] = 01: Load EEPROM word 176 ~ 191 for port 3 setting Bit [9:8] = 01: Load EEPROM word 192 ~ 207 for port 4 setting Bit [11:10] = 01: Load EEPROM word 208 ~ 223 for port 5 setting Bit [15:12] = Reserved, set ZEROs
RESERVED	16~17	Reserved, set ZEROs
Switch Control	18	Bit [6:0] of this word will be loaded to Switch Control register 212H bit [6:0], respectively

CPU Port & Mirror Control	19	This word will be loaded into CPU Port & Mirror Control register 213H in its entirety
Special Tag Ether-Type	20	This word will be loaded into Special Tag Ether-Typel register 214H in its entirety
Global Learning & Aging Control	21	Bit [5:0] of this word will be loaded to Global Learning & Aging Control register 215H bit [5:0], respectively
MIB Counter Disable	22	Bit [5:0] of this word will be loaded to register 230H bit [5:0], respectively
Snooping Control 0	23	Bit [13:0] of this word will be loaded to register 29BH bit [13:0], respectively
Snooping Control 1	24	Bit [13:1] of this word will be loaded to register 29CH bit [13:1], respectively
RESERVED	25~27	Reserved, set ZEROs
VLAN Priority Map Register	28	This word will be loaded into register 217H in its entirety
TOS Priority Map 0	29	This word will be loaded into register 218H in its entirety
TOS Priority Map 1	30	This word will be loaded into register 219H in its entirety
TOS Priority Map 2	31	This word will be loaded into register 21AH in its entirety
TOS Priority Map 3	32	This word will be loaded into register 21BH in its entirety
TOS Priority Map 4	33	This word will be loaded into register 21CH in its entirety
TOS Priority Map 5	34	This word will be loaded into register 21DH in its entirety
TOS Priority Map 6	35	This word will be loaded into register 21EH in its entirety
TOS Priority Map 7	36	This word will be loaded into register 21FH in its entirety
RESERVED	37~47	Reserved, set ZEROs
QinQ TPID Register	48	This word will be loaded into register 23DH in its entirety
VLAN Mode & Rule Control	49	This word will be loaded into register 23EH in its entirety
VLAN Table - Valid Control	50	This word will be loaded into register 23FH in its entirety
VLAN Table - ID_0H	51	This word will be loaded into register 250H in its entirety
VLAN Table - ID_1H	52	This word will be loaded into register 251H in its entirety
VLAN Table - ID_2H	53	This word will be loaded into register 252H in its entirety
VLAN Table - ID_3H	54	This word will be loaded into register 253H in its entirety
VLAN Table - ID_4H	55	This word will be loaded into register 254H in its entirety
VLAN Table - ID_5H	56	This word will be loaded into register 255H in its entirety
VLAN Table - ID_6H	57	This word will be loaded into register 256H in its entirety
VLAN Table - ID_7H	58	This word will be loaded into register 257H in its entirety
VLAN Table - ID_8H	59	This word will be loaded into register 258H in its entirety
VLAN Table - ID_9H	60	This word will be loaded into register 259H in its entirety
VLAN Table - ID_AH	61	This word will be loaded into register 25AH in its entirety
VLAN Table - ID_BH	62	This word will be loaded into register 25BH in its entirety
VLAN Table - ID_CH	63	This word will be loaded into register 25CH in its entirety
VLAN Table - ID_DH	64	This word will be loaded into register 25DH in its entirety
VLAN Table - ID_EH	65	This word will be loaded into register 25EH in its entirety
VLAN Table - ID_FH	66	This word will be loaded into register 25FH in its entirety
VLAN Table - MEMBER_0H	67	Bit [13:0] of this word will be loaded to register 270H bit [13:0], respectively
VLAN Table - MEMBER_1H	68	Bit [13:0] of this word will be loaded to register 271H bit [13:0], respectively
VLAN Table - MEMBER_2H	69	Bit [13:0] of this word will be loaded to register 272H bit [13:0], respectively
VLAN Table - MEMBER_3H	70	Bit [13:0] of this word will be loaded to register 273H bit [13:0], respectively
VLAN Table - MEMBER_4H	71	Bit [13:0] of this word will be loaded to register 274H bit [13:0], respectively
VLAN Table - MEMBER_5H	72	Bit [13:0] of this word will be loaded to register 275H bit [13:0], respectively

VLAN Table - MEMBER_6H	73	Bit [13:0] of this word will be loaded to register 276H bit [13:0], respectively
VLAN Table - MEMBER_7H	74	Bit [13:0] of this word will be loaded to register 277H bit [13:0], respectively
VLAN Table - MEMBER_8H	75	Bit [13:0] of this word will be loaded to register 278H bit [13:0], respectively
VLAN Table - MEMBER_9H	76	Bit [13:0] of this word will be loaded to register 279H bit [13:0], respectively
VLAN Table - MEMBER_AH	77	Bit [13:0] of this word will be loaded to register 27AH bit [13:0], respectively
VLAN Table - MEMBER_BH	78	Bit [13:0] of this word will be loaded to register 27BH bit [13:0], respectively
VLAN Table - MEMBER_CH	79	Bit [13:0] of this word will be loaded to register 27CH bit [13:0], respectively
VLAN Table - MEMBER_DH	80	Bit [13:0] of this word will be loaded to register 27DH bit [13:0], respectively
VLAN Table - MEMBER_EH	81	Bit [13:0] of this word will be loaded to register 27EH bit [13:0], respectively
VLAN Table - MEMBER_FH	82	Bit [13:0] of this word will be loaded to register 27FH bit [13:0], respectively
VLAN Table - Priority Enable	83	This word will be loaded into register 290H in its entirety
RESERVED	84	Reserved
VLAN Table - STP Index Enable	85	This word will be loaded into register 292H in its entirety
VLAN Table - Misc_0	86	This word will be loaded into register 293H in its entirety
VLAN Table - Misc_1	87	This word will be loaded into register 294H in its entirety
VLAN Table - Misc_2	88	This word will be loaded into register 295H in its entirety
VLAN Table - Misc_3	89	This word will be loaded into register 296H in its entirety
VLAN Table - Misc_4	90	This word will be loaded into register 297H in its entirety
VLAN Table - Misc_5	91	This word will be loaded into register 298H in its entirety
VLAN Table - Misc_6	92	This word will be loaded into register 299H in its entirety
VLAN Table - Misc_7	93	This word will be loaded into register 29AH in its entirety
RESERVED	94~127	Reserved, set ZEROs
P0 Basic Control 0	128	Bit [14:0] of this word will be loaded to register 111H bit [14:0], respectively
P0 Basic Control 1	129	Bit [15:0] of this word will be loaded to register 112H bit [15:0], respectively
P0 Block Contrl 0	130	Bit [13:0] of this word will be loaded to register 113H bit [13:0], respectively
P0 Block Contrl 1	131	Bit [13:0] of this word will be loaded to register 114H bit [13:0], respectively
P0 Bandwidth Control	132	Bit [15:0] of this word will be loaded to register 115H bit [15:0], respectively
P0 VLAN Tag Infomation	133	Bit [15:0] of this word will be loaded to register 116H bit [15:0], respectively
P0 Priority & VLAN Control	134	Bit [15:0] of this word will be loaded to register 117H bit [15:0], respectively
P0 Security Control	135	Bit [14:0] of this word will be loaded to register 118H bit [14:0], respectively
P0 Advanced Control	136	Bit [15:0] of this word will be loaded to register 119H bit [15:0], respectively
P0 Memory Configuration	137	Bit [15:0] of this word will be loaded to register 11AH bit [15:0], respectively
P0 Discard packet limitation	138	Bit [15:0] of this word will be loaded to register 11BH bit [15:0], respectively
RESERVED	139~143	Reserved, set ZEROs
P1 Basic Control 0	144	Bit [14:0] of this word will be loaded to register 131H bit [14:0], respectively
P1 Basic Control 1	145	Bit [15:0] of this word will be loaded to register 132H bit [15:0], respectively
P1 Block Contrl 0	146	Bit [13:0] of this word will be loaded to register 133H bit [13:0], respectively
P1 Block Contrl 1	147	Bit [13:0] of this word will be loaded to register 134H bit [13:0], respectively
P1 Bandwidth Control	148	Bit [15:0] of this word will be loaded to register 135H bit [15:0], respectively

P1 VLAN Tag Infomation	149	Bit [15:0] of this word will be loaded to register 136H bit [15:0], respectively
P1 Priority & VLAN Control	150	Bit [15:0] of this word will be loaded to register 137H bit [15:0], respectively
P1 Security Control	151	Bit [14:0] of this word will be loaded to register 138H bit [14:0], respectively
P1 Advanced Control	152	Bit [15:0] of this word will be loaded to register 139H bit [15:0], respectively
P1 Memory Configuration	153	Bit [15:0] of this word will be loaded to register 13AH bit [15:0], respectively
P1 Discard packet limitation	154	Bit [15:0] of this word will be loaded to register 13BH bit [15:0], respectively
RESERVED	155~159	Reserved, set ZEROs
P2 Basic Control 0	160	Bit [14:0] of this word will be loaded to register 151H bit [14:0], respectively
P2 Basic Control 1	161	Bit [15:0] of this word will be loaded to register 152H bit [15:0], respectively
P2 Block Contrl 0	162	Bit [13:0] of this word will be loaded to register 153H bit [13:0], respectively
P2 Block Contrl 1	163	Bit [13:0] of this word will be loaded to register 154H bit [13:0], respectively
P2 Bandwidth Control	164	Bit [15:0] of this word will be loaded to register 155H bit [15:0], respectively
P2 VLAN Tag Infomation	165	Bit [15:0] of this word will be loaded to register 156H bit [15:0], respectively
P2 Priority & VLAN Control	166	Bit [15:0] of this word will be loaded to register 157H bit [15:0], respectively
P2 Security Control	167	Bit [14:0] of this word will be loaded to register 158H bit [14:0], respectively
P2 Advanced Control	168	Bit [15:0] of this word will be loaded to register 159H bit [15:0], respectively
P2 Memory Configuration	169	Bit [15:0] of this word will be loaded to register 15AH bit [15:0], respectively
P2 Discard packet limitation	170	Bit [15:0] of this word will be loaded to register 15BH bit [15:0], respectively
RESERVED	171~175	Reserved, set ZEROs
P3 Basic Control 0	176	Bit [14:0] of this word will be loaded to register 171H bit [14:0], respectively
P3 Basic Control 1	177	Bit [15:0] of this word will be loaded to register 172H bit [15:0], respectively
P3 Block Contrl 0	178	Bit [13:0] of this word will be loaded to register 173H bit [13:0], respectively
P3 Block Contrl 1	179	Bit [13:0] of this word will be loaded to register 174H bit [13:0], respectively
P3 Bandwidth Control	180	Bit [15:0] of this word will be loaded to register 175H bit [15:0], respectively
P3 VLAN Tag Infomation	181	Bit [15:0] of this word will be loaded to register 176H bit [15:0], respectively
P3 Priority & VLAN Control	182	Bit [15:0] of this word will be loaded to register 177H bit [15:0], respectively
P3 Security Control	183	Bit [14:0] of this word will be loaded to register 178H bit [14:0], respectively
P3 Advanced Control	184	Bit [15:0] of this word will be loaded to register 179H bit [15:0], respectively
P3 Memory Configuration	185	Bit [15:0] of this word will be loaded to register 17AH bit [15:0], respectively
P3 Discard packet limitation	186	Bit [15:0] of this word will be loaded to register 17BH bit [15:0], respectively
RESERVED	187~191	Reserved, set ZEROs
P4 Basic Control 0	192	Bit [14:0] of this word will be loaded to register 191H bit [14:0], respectively
P4 Basic Control 1	193	Bit [15:0] of this word will be loaded to register 192H bit [15:0], respectively
P4 Block Contrl 0	194	Bit [13:0] of this word will be loaded to register 193H bit [13:0], respectively
P4 Block Contrl 1	195	Bit [13:0] of this word will be loaded to register 194H bit [13:0], respectively
P4 Bandwidth Control	196	Bit [15:0] of this word will be loaded to register 195H bit [15:0], respectively
P4 VLAN Tag Infomation	197	Bit [15:0] of this word will be loaded to register 196H bit [15:0], respectively
P4 Priority & VLAN Control	198	Bit [15:0] of this word will be loaded to register 197H bit [15:0], respectively
P4 Security Control	199	Bit [14:0] of this word will be loaded to register 198H bit [14:0], respectively

P4 Advanced Control	200	Bit [15:0] of this word will be loaded to register 199H bit [15:0], respectively
P4 Memory Configuration	201	Bit [15:0] of this word will be loaded to register 19AH bit [15:0], respectively
P4 Discard packet limitation	202	Bit [15:0] of this word will be loaded to register 19BH bit [15:0], respectively
RESERVED	203~207	Reserved, set ZEROs
P5 Basic Control 0	208	Bit [14:0] of this word will be loaded to register 1B1H bit [14:0], respectively
P5 Basic Control 1	209	Bit [15:0] of this word will be loaded to register 1B2H bit [15:0], respectively
P5 Block Contrl 0	210	Bit [13:0] of this word will be loaded to register 1B3H bit [13:0], respectively
P5 Block Contrl 1	211	Bit [13:0] of this word will be loaded to register 1B4H bit [13:0], respectively
P5 Bandwidth Control	212	Bit [15:0] of this word will be loaded to register 1B5H bit [15:0], respectively
P5 VLAN Tag Infomation	213	Bit [15:0] of this word will be loaded to register 1B6H bit [15:0], respectively
P5 Priority & VLAN Control	214	Bit [15:0] of this word will be loaded to register 1B7H bit [15:0], respectively
P5 Security Control	215	Bit [14:0] of this word will be loaded to register 1B8H bit [14:0], respectively
P5 Advanced Control	216	Bit [15:0] of this word will be loaded to register 1B9H bit [15:0], respectively
P5 Memory Configuration	217	Bit [15:0] of this word will be loaded to register 1BAH bit [15:0], respectively
P5 Discard packet limitation	218	Bit [15:0] of this word will be loaded to register 1BBH bit [15:0], respectively
RESERVED	219~255	Reserved, set ZEROs

7 Function Description

7.1 Switch Function

7.1.1 Address Learning

The DM8606C/DM8606CI stores MAC addresses, port number and time stamp information in the Hash-based Address Table. The table can learn up to 2K unicast address entries. The DM8606C/DM8606CI provides two methods to learn address in the table, self-learning and manual learning.

Self-learning

The self-learning mechanism means the DM8606C/DM8606CI learn the MAC addresses of incoming packets in real time without CPU's assistance.

The switch engine creates a new entry if incoming packet's Source Address (SA) does not exist and the packet is valid (error-free). If SA was found and incoming port mismatch with port number in table, update the entry with SA and incoming port number. Those entries will be created, updated or aged dynamically. Besides, the DM8606C/DM8606CI has an option to disable address learning for individual port. This feature can be set by bit 12 of per port register 11h (i.e. 111h, 131h, 151h, 171h, 191h, and 1B1h).

Manual Learning

The DM8606C/DM8606CI also provides manual learning mechanism with CPU's assistance. The CPU can create, update or delete entry for flexible management. In addition to above, the entry can be set as static one that will not be aged-out.

7.1.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time. The period can be programmed or disabled through bit 0 & 1 of register 215h

7.1.3 Packet Forwarding

The DM8606C/DM8606CI forwards the incoming packet according to following decision:

- If Destination Address (DA) is multicast/broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.
- Switch engine would look up address table based on DA when incoming packets is uni-cast. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.
- Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM8606C/DM8606CI will filter incoming packets under following conditions:

- Error packets, including CRC errors, alignment errors, illegal size errors.
- IEEE 802.3X PAUSE packets.
- If incoming packet is uni-cast and its destination port number is equal to source port number

7.1.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

7.1.5 Back-off Algoruthm

The DM8606C/DM8606CI implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

7.1.6 Late Collision

The DM8606C/DM8606CI implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

7.1.7 Half Duplex Flow Control

The DM8606C/DM8606CI supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM8606C/DM8606CI sends jam pattern and results in a collision.

7.1.8 Full Duplex Flow Control

The DM8606C/DM8606CI supports IEEE standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, The DM8606C/DM8606CI will defer transmitting next normal frames, if it receives a pause frame from link partner.

On the transmit side, The DM8606C/DM8606CI issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM8606C/DM8606CI sends out a pause frame with zero pause time allows traffic to resume immediately.

7.1.9 Partition Mode

The DM8606C/DM8606CI provides a partition mode for each port. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

Entering Partition State
A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

While in Partition state
The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

Exiting from Partition State
The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

7.1.10 Broadcast Storm Filtering

The DM8606C/DM8606CI has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two types of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through bit 12 of per port register 12h.

The broadcast storm threshold can be programmed by EEPROM or per port register 5h, the default setting is no broadcast storm protecting.

7.1.11 Bandwidth Control

The DM8606C/DM8606CI supports two types of bandwidth control for each port. One is the ingress and egress bandwidth rate can be controlled separately, the other is combined together, this function can be set through bit 14 of per port register 12h. The bandwidth control is disabled by default.

To separate bandwidth control mode, the threshold rate is defined in per port register 5h. For combined mode, it is defined in bit 3~0 of per port register 15h.

The behavior of bandwidth control as below:

- For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.
- For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.
- In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

7.1.12 Port Monitoring Support

The DM8606C/DM8606CI supports “Port Monitoring” function on per port base, detail as below:

Sniffer Port and Monitor Port
There is only one port can be selected as “sniffer port” by bit 5~3 of register 213h, multiple ports can be set as “receive monitor port” or “transmit monitor port” in per-port register 11h.

Receive monitor
All packets received on the “receive monitor port” are send a copy to “sniffer port”. For example, port 0 is set as “receive monitor port” and port 2 is selected as a “sniffer port”. If a packet is received form port 0 and predestined to port 1 after forwarding decision, the DM8606C/DM8606CI will forward it to port 1 and port 2 in the end.

Transmit monitor
All packets transmitted on the “transmit monitor port” are send a copy to “sniffer port”. For example, port 1 is set as “transmit monitor port” and port 2 is selected as “sniffer port”. If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM8606C/DM8606CI will forward it to port 1 and port 2 in the end.

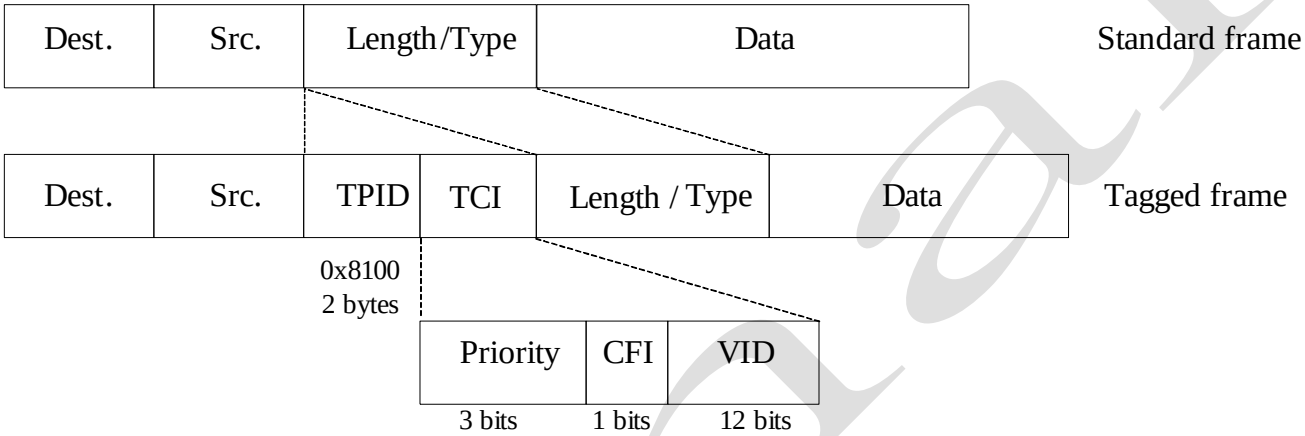
Exception
The DM8606C/DM8606CI has an optional setting that broadcast/multicast packets are not monitored (see bit 11 of per port register 12h). It’s useful to avoid unnecessary bandwidth.

7.1.13 VLAN Support
7.1.13.1 Port-Based VLAN

The DM8606C/DM8606CI supports port-based VLAN as default, up to 16 groups. Each port has a default VID called PVID (Port VID, in bit 11~0 of per port register 16H). The DM8606C/DM8606CI used 12 bits PVID as index and mapped with registers 250H~25FH to define the VLAN groups.

7.1.13.2 802.1q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).



The DM8606C/DM8606CI also supports 16 802.1Q-based VLAN groups, as specified in bit 0 of register 23Eh. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM8606C/DM8606CI used full 12 bits VID of received packet with VLAN tag and VLAN table ID registers (250h~25Fh) and then define members by VLAN Group Mapping Register (270h~27Fh) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.

7.1.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by bit 14 of per port register 17h in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

Receive untagged packet and forward to Un-tag port.
Received packet will forward to destination port without modification.

Receive tagged packet and forward to Un-tag port.
The DM8606C/DM8606CI will remove the tag from the packet and recalculate CRC before sending it out.

Receive untagged packet and forward to Tag port.
The DM8606C/DM8606CI will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

Receive tagged packet and forward to Tag port.
Received packet will forward to destination port without modification.

7.1.14 Special Tag

The Special Tag function provided by the DM8606C/DM8606CI is used to exchange control and status information between Switch and CPU within frame. An extra 4-bytes tag is added into frame to carry different content according to direction of special tag frame. Received special tag (CPU Switch) specifies the desired port mapping of packet sent by CPU and some configurations about frame handle rules. Transmitted special tag (Switch CPU) indicates the source port number of incoming frame.

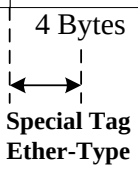
The following figure shows special tag frame format. In left 2 bytes of special tag field, there is an identifier called Special Tag Ether-Type that can use to recognize special tag frame. The value of this field can be set by REG 23DH.

Frame without VLAN Tag

DMAC	SMAC	Special Tag	Type / Length	DATA	CRC

Frame with VLAN Tag

DMAC	SMAC	Special Tag	VLAN Tag	Type / Length	DATA	CRC



The detail information carried by received special tag is described as below. Through received special tag, CPU can tell switch the handle rule per frame over the internal setting. This feature can be enabled through REG 213H bit 6.

Received Special Tag(CPU → Switch) 4-byte Format:

Byte 0/1	[15:0]	Special Tag Ether-Type (Default: 0x8086)
Byte 2	[7]	Reserved
Byte 2	[6]	ST_PMAP_en, ST_PMAP Enable
Byte 2	[5:0]	ST_PMAP, Force to assign forwarding port map
Byte 3	[7]	Reserved
Byte 3	[6]	ST_CVLAN, Cross VLAN 1: This frame can cross VLAN boundary. 0: This frame obeys VLAN boundary.
Byte 3	[5]	ST_LRN_DIS, Disable learning 1: This frame will not be learned 0: This frame will be learned
Byte 3	[4]	ST_PRI_EN, ST_PRI Enable
Byte 3	[3:2]	ST_PRI, Priority Queue Number (0~3) 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3
Byte 3	[1:0]	ST_TAG 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved

Beside, transmitted special tag is used to indicate source port number. CPU can use this message to judge the incoming port number of the frame. REG 213H bit 7 can enable this feature by setting to 1.

Transmitted Special Tag (Switch → CPU) 4-byte Format:

Byte 0/1	[15:0]	Special Tag Ether-Type (Default: 0x8086)
Byte 2	[7:3]	Reserved
Byte 2	[2:0]	ST_SPORT, Source Port Number (0~5)
Byte 3	[7:0]	Reserved

7.1.15 Priority Support

The DM8606C/DM8606CI supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM8606C/DM8606CI provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM8606C/DM8606CI offers four level queues for transmit on per-port based.

The DM8606C/DM8606CI provides two packet scheduling algorithms: Weighted Fair Queuing and Strict Priority Queuing. Weighted Fair Queuing (WFQ) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The Packet on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in bit 5 of per port register 17H.

7.1.15.1 Port-Based Priority

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in bit 1~0 of per port register 17H.

7.1.15.2 802.1p-Based Priority

The DM8606C/DM8606CI extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers 217H to determine which transmit queue is designated. The VLAN Priority Map is programmable.

7.1.15.3 DiffServ-Based Priority

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (218H~21FH) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see bit 7 of register 23EH.

7.1.16 Address Table Accessing

7.1.16.1 Type of Address Table

There are three types of address table in the DM8606C/DM8606CI. The description is represented below:

Unicast Address Table

This table is used for destination MAC address lookup and source MAC address learning. The table can have up to 2048 entries. If the table is full, the latest one will kick out the eldest one. The programming method can refer to next section.

Multicast Address Table

The table that stores multicast addresses shares with unicast address table and can be maintained by host CPU for custom filtering and forwarding multicast packets. If the table is full, the latest one will kick out the eldest one. All of entries in multicast address table are static one. In addition to host CPU, multicast address table can be manipulated by internal switch engine, if hardware-based IGMP Snooping function is enabled.

IGMP Membership Table

This table is used to establish IPv4 multicast forwarding rule under IGMP protocol if hardware-based IGMP Snooping function is enabled. It is automatic maintained by internal engine according to snooping IGMP control packets, and can only support to read out by the host CPU. The maximum of entries of table is 32. If the table is full, never join anymore

7.1.16.2 Access Rules of Address Table

In DM8606C/DM8606CI, unicast and multicast address table support “Write”, “Delete”, ”Search”, “Read” and “Clear” commands. However, for IGMP membership table, there are only three different type commands such as “Write”, “Delete” and “Read”. The DM8606C/DM8606CI procedure and flow chart of Entry Access is described as following:

Entry Write

- Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.
- Write the MAC address to the Address Table Data 1~3 Registers (Reg2B2H~2B4H).
- Write the Port Number or Port Map to Address Table Data 0 Register (Reg2B1.[2:0]).
- If need, write the entry’s attribute such as static to Address Table Data 4 Register (Reg2B5H.0).
- Write the “WRITE” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.
- Check the busy bit again, wait for available.
- Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13])

Entry Delete

- Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.
- Write the MAC address to the Address Table Data 1~3 Registers (Reg2B2H~2B4H).
- Write the “DELETE” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation
- Check the busy bit again, wait for available.
- Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13]).

Entry Search

- Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.
- Write the MAC address to the Address Table Data 1~3 Registers (Reg2B2H~2B4H).
- Write the “SEARCH” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.
- Check the busy bit again, wait for available.
- Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13]).
- Read the Port Number or Port Map to Address Table Data 0 Register (Reg2B1.[2:0]).
- If need, read the entry sequence (the sequence number of entry in address table) from Address Table Data 1 Register (Reg2B2H).
- If need, read the entry’s attributes that include static (unicast address table only) and IGMP Entry (multicast address table only) from Address Table Data 4 Register (Reg2B5H.0 for static and Reg2B5h.12 for IGMP Entry).

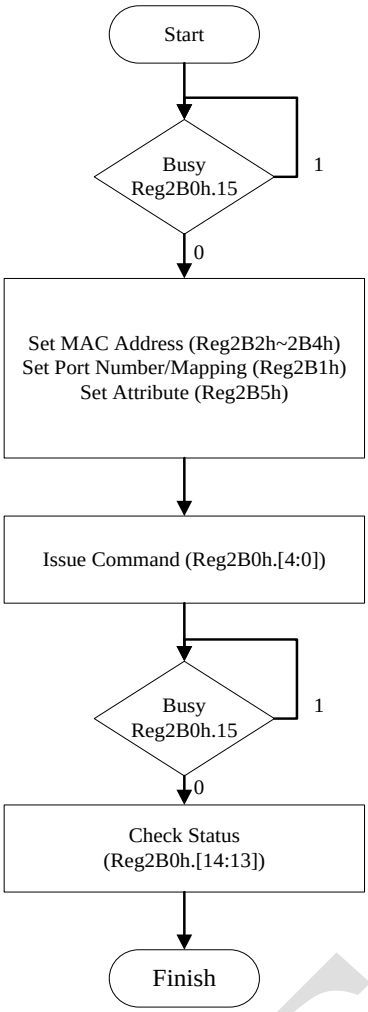
Entry Read

- Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.
- Write the entry sequence to the Address Table Data 1 Register (Reg2B2H).
- Write the “READ” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.
- Check the busy bit again, wait for available.
- Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13]).
- Read the Port Number or Port Map to Address Table Data 0 Register (Reg2B1.[2:0]).
- If target is unicast or multicast address table, read the entry’s MAC address from Address Table Data 1~3 Register (Reg2B2H~2B4H). If target is IGMP membership table, read the real memory address from Address Table Data 1 Register (Reg2B2H.[10:0]).
- If target is unicast address table, read the entry’s attributes such as static from Address Table Data 4 Register (Reg2B5H.0). For multicast address table, IGMP Entry can be read from Address Table Data 4 Register (Reg2B5H.[12]). For IGMP membership table, IGMP valid signal and per-port aged timer can be read from Address Table Data 2~3 Register (Reg2B3H.[2:0], Reg2B4H.[5:0]).

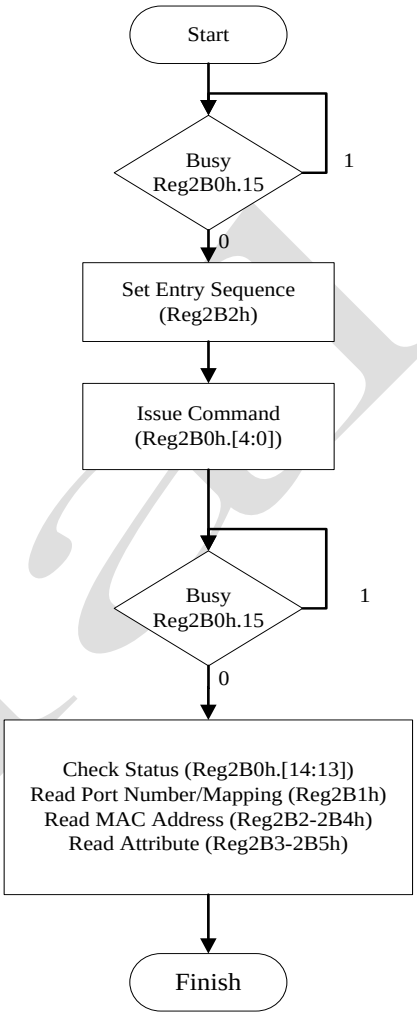
Entry Clear

- Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.
- Write the “Clear” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.
- Wait at least 4.5ms for clear procedure is done.
- Check the busy bit again, wait for available.

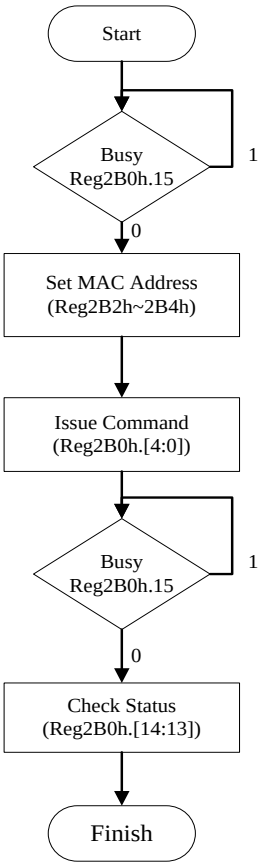
Entry Write



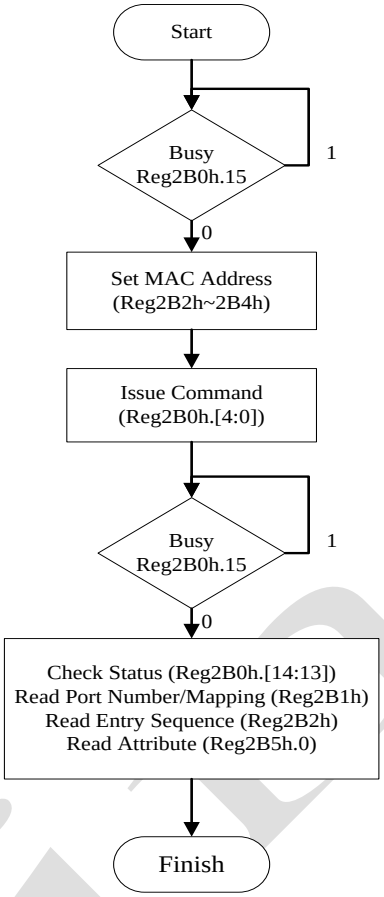
Entry Read



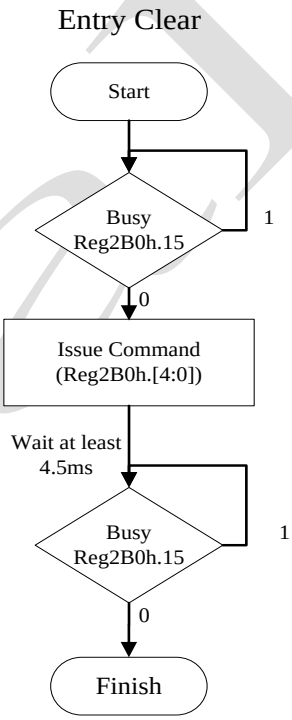
Entry Delete



Entry Search



Entry Clear



7.1.17 IGMP Snooping

The Internet Group Management Protocol (IGMP) is a communications protocol used to manage the membership of Internet Protocol multicast groups. IGMP is used by IP hosts and adjacent multicast routers to establish multicast group memberships. There are three versions of IGMP, as defined by "Request for Comments" (RFC) documents of the Internet Engineering Task Force (IETF). IGMP v1 is defined by RFC 1112, IGMP v2 is defined by RFC 2236 and IGMP v3 is defined by RFC 3376.

IGMP snooping is a feature that allows the switch to "listen in" on the IGMP protocol conversation between hosts and routers. The IGMP snooping switch hears an IGMP report from a host with a given multicast group address. It adds the host's port number to the multicast list for that group, and when the switch hears an IGMP Leave, it removes the host's port from the table entry. Finally, switch will only forward multicast traffic to the hosts interested in that traffic. Therefore, this function can effectively reduce multicast traffic.

DM8606C/DM8606CI supports two types of IGMP Snooping, software-based and hardware-based.

7.1.17.1 Software-Based IGMP Snooping

If packet that is IGMP packet (the protocol field is 02H in the header of IPv4 packet) would be forward to CPU port when IGMP Snooping is enabled and in software-based mode. In this mode, the supported version of IGMP and the maximal entries depend on software implementation. CPU receives and parses the IGMP packets, and then set the MAC address and port map in Multicast Address Table.

For example:

- If receiving V1REPORT or V2REPORT (i.e. Join), translate the Multicast IP address to MAC address first, and then write the MAC address and source port number to Multicast Address Table.
- If receiving LEAVE and Fast Leave function is enabled, translate the Multicast IP and delete the entry directly.
- If the time (Query Interval * Robust Variable + Max Response Time, 260sec default) is expired which means the entry never be updated, delete the entry in Multicast Address Table.
- Entry delete may mean to clear the owned port bit on the port map when there are other occupied. Otherwise, delete the entry via delete command.

7.1.17.2 Hardware-Based IGMP Snooping

The DM8606C/DM8606CI supports IGMP v1/v2 snooping and the maximal group is 32 without any software effort in this mode. The DM8606C/DM8606CI automatically manipulates and updates IGMP membership table and Multicast table according to IGMP control packets, such as membership report and leave.

If IGMP membership table is full, the later incoming IGMP Membership Report (Join) packet will be ignored and the group address won't be registered into multicast address table. After that, the unregistered IP multicast packets (the destination MAC address can not be found in the multicast address table) will be treated as normal multicast packets by default. The additional forwarding control method can see the register Reg29BH.[3:2].

The DM8606C/DM8606CI supports router ports auto-detect and auto-aging mechanism. The port which receives IGMP Query packets will be treated as router port by default. The router port also can be define as static one by user (see Reg29BH.7) and the port map of the router port can be programmed at Reg29BH.[10:8]. Keep in mind that the CPU port is never treated as router port. The DM8606C/DM8606CI leaves the router port if the time (Router Present Timeout, 400sec by default) is expired that the port never receives IGMP Query during this period.

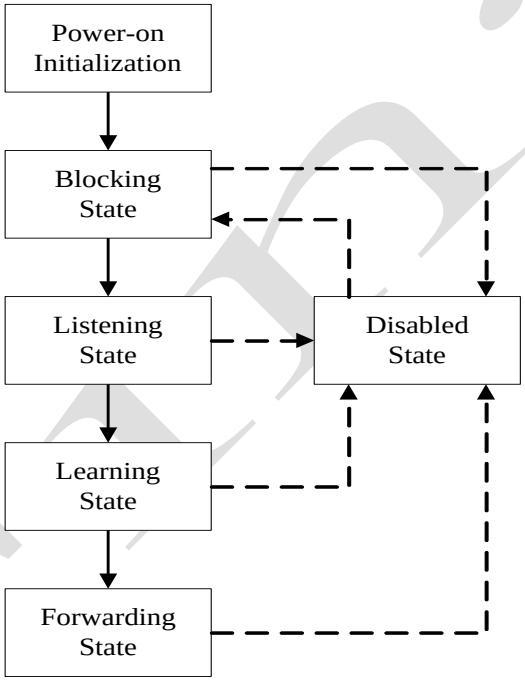
7.1.18 IPv6 MLD Snooping

The DM8606C/DM8606CI forwards the IPv6 Multicast Listener Discovery (MLD) packets to the processor port when MLD Snooping is enabled and the MLD packets meet following scenario:

- IPv6 Multicast packets.
- The Hop Limit in IPv6 header is 1.
- The Next Header in IPv6 header is 0x3A (ICMPv6) or 0x00 (and next header of hop-by-hop option header is 0x3A).
- The Type in ICMP header is 0x82 (Multicast Listener Query), 0x83 (Multicast Listener Report) or 0x84 (Multicast Listener Done).

7.1.19 STP / RSTP Support

DM8606C/DM8606CI supports both Spanning Tree Protocol (STP) and Rapid Spanning Tree Protocol(RSTP). There are five types of STP Port State (Disabled, Blocking, Listening, Learning and Forwarding state) and three types of RSTP Port State (Discarding, Learning and Forwarding) for these two protocols. The following figure is the port state diagram of STP.



But in RSTP, there are only three port states. The port states comparison between STP and RSTP are listed as below.

STP Port State	RSTP Port State
Disabled	Discarding
Blocking	Discarding
Listening	Discarding
Learning	Learning
Forwarding	Forwarding

For compatibility and design consideration, this function needs the cooperation with external CPU. Moreover, the behavior of Disabled/Blocking/Listening states in STP must be equal to the behavior of Discarding state in RSTP in DM8606C/DM8606CI. The difference between STP and RSTP should be implemented by CPU. The following statement describes the STP/RSTP port state behavior and software action in DM8606C/DM8606CI.

Disable State:

- Drop all packets including BPDUs

  → Implemented by transmitting BPDUs to CPU and CPU drops BPDUs.
- Learning is disabled.
- Does not transmit BPDUs received from CPU

  → Implemented by CPU does not send BPDUs to this port

Blocking State:

- Drop all packets except BPDUs and transmit received BPDUs to CPU.
- Learning is disabled.
- Does not transmit BPDUs received from CPU

Listening State:

- Drop all packets except BPDUs and tranmit received BPDUs to CPU
- Learning is disabled.
- Forward BPDUs received from CPU

  → Implemented by CPU uses special tag function to send BPDUs to decided port

Learning State:

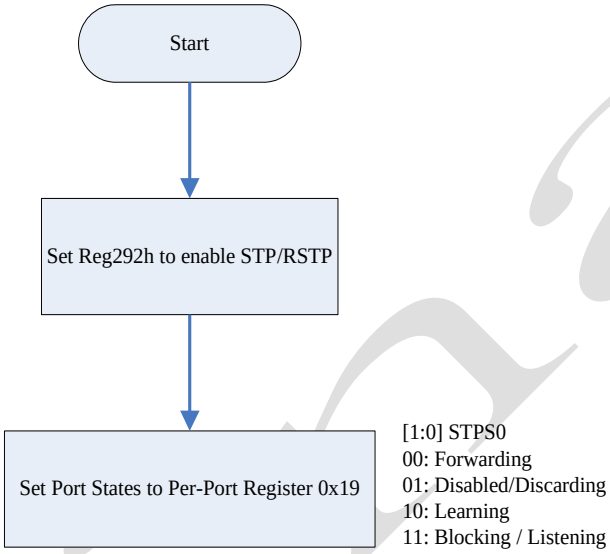
- Drop all packets except BPDUs and transmit received BPDUs to CPU
- Learning is enabled
- Forward BPDUs received from CPU

Forwarding State:

Base on the behavior of different states described above, DM8606C/DM8606CI has a port states setting for both STP and RSTP in per-port register 19h, . The register setting is：

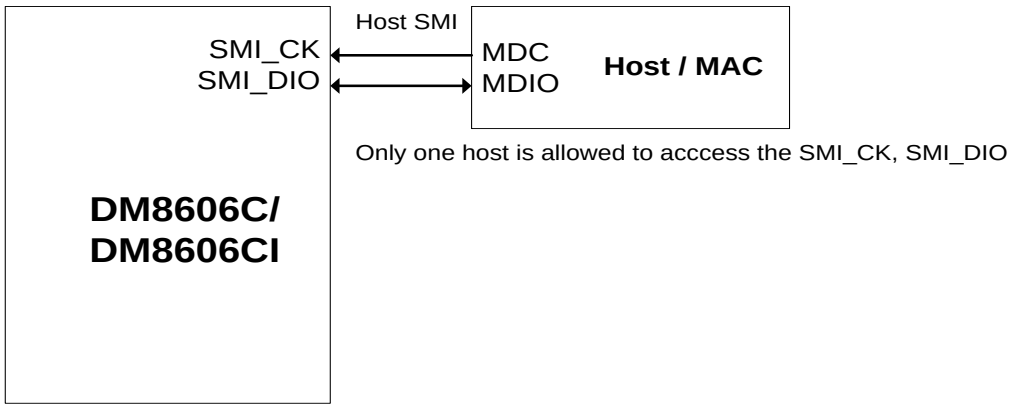
i. 00： Forwarding
ii. 01： Disabled / Discarding
iii. 10： Learning
iv. 11： Blocking / Listening

The following flow diagram shows how to configure STP/RSTP function.

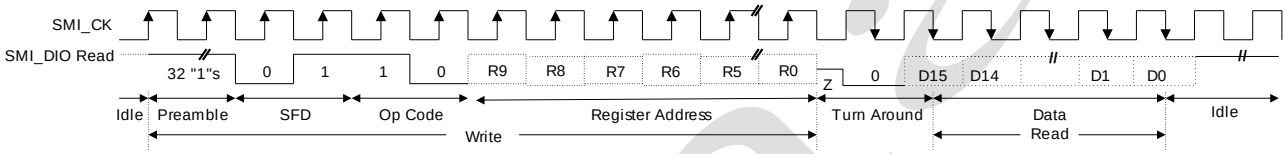


STP/RSTP Setting

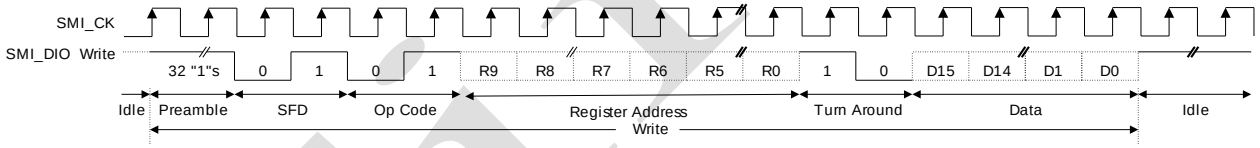
7.2 Host SMI Interface



Host SMI - Read Frame Structure



Host SMI - Write Frame Structure



The internal registers of DM8606C/DM8606CI can be accessed by Host Serial Management Interface (SMI). The application of SMI illustrated as below.

The Host SMI consists of two pins, one is SMI_CK and another is SMI_DIO. User can access DM8606C/DM8606CI's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI. The format is following. 32 bit "1" preamble field, "01" <SFD> field, <OpCode> field ("10" for read, ""01" for write), the <Register Address> field of the frame is mapped to address of control and status register set of DM8606C/DM8606CI, and the 16-bit <Data> field for read/writ data.

7.2.1 Host SMI Bus Error Check Function

To prevent the host SMI bus to be interfered by noise on board-level. This function is used to check the command validity to suppress the mistaken command. In write procedure, the written value in register will be applied until the correct checksum is written (error proofing) and user can read status for validation (error detecting). In read procedure, user can compare hardware calculated checksum with software calculated one to validate the result.

For example:
Write Procedure

- Set register 33AH.[0] = 1 to enable SMI Bus Error Check function
- Write data to DM8606C/DM8606CI's register (general write command)
- CPU calculate checksum (CSUM[7:0]) and write it to register 339H.[7:0]
- Check function status in register 339H.[8]

Read Procedure

- Set register 33AH.[0] = 1 to enable SMI Bus Error Check function
- Read data from DM8606C/DM8606CI's register (general read command)
- Read hardware calculated checksum from register 339H.[7:0] and compare it with CPU calculated one (CSUM[7:0])

Checksum calculate formula:

CSUM[0] = D[0] ^ D[8] ^ R[0] ^ R[8]
CSUM[1] = D[1] ^ D[9] ^ R[1] ^ R[9]
CSUM[2] = D[2] ^ D[10] ^ R[2] ^ OP[0]
CSUM[3] = D[3] ^ D[11] ^ R[3] ^ OP[1]
CSUM[4] = D[4] ^ D[12] ^ R[4]
CSUM[5] = D[5] ^ D[13] ^ R[5]
CSUM[6] = D[6] ^ D[14] ^ R[6]
CSUM[7] = D[7] ^ D[15] ^ R[7]

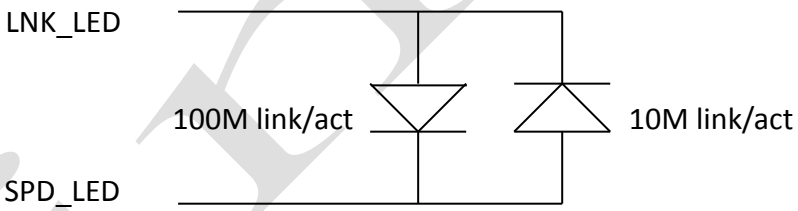
Note:

D[15:0] = <Data> field of SMI frame
R[9:0] = <Register Address> field of SMI frame
OP[1:0] = <Op Code> field of SMI frame

7.3 LED Mode Control

LED mode	
Bit [1:0] of register 317H	"00" : LED mode 0 "01" : LED mode 1, dual color mode "10" : LED mode 2 "11" : LED mode 3 (default)

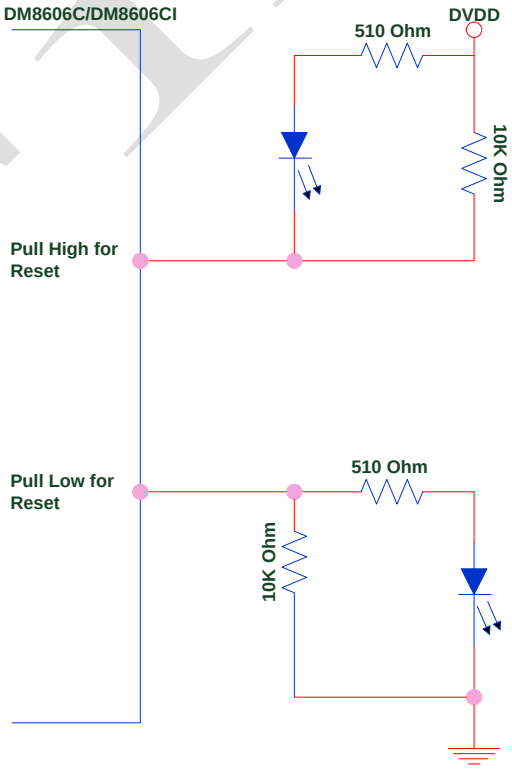
LED mode 0	
P0~4_LNK_LED	100M link + Activity OFF: 100M link fail ON : 100M link ok and no TX/RX activity BLINK: 100M link ok and TX/RX activity
P0~4_SPD_LED	Collision OFF: no collision BLINK: collision
P0~4_FDX_LED	10M link + Activity OFF: 10M link fail ON: 10M link ok and no TX/RX activity BLINK: 10M link ok and TX/RX activity

LED mode 1 (Dual color mode)			
P0~4_LNK_LED P0~4_SPD_LED	Application circuit : 		
		LNK_LED	SPD_LED
	link off	HI	HI
	100M link	HI	LO
	100M link / activity	BLINK	LO
	10M link	LO	HI
	10M link / activity	LO	BLINK
P0~4_FDX_LED	Full / half duplex mode OFF: half-duplex ON: full-duplex BLINK: half-duplex and collision		

LED mode 2	
P0~4_LNK_LED	100M link + Activity OFF: 100M link fail ON: 100M link ok and no TX/RX activity BLINK: 100M link ok and TX/RX activity
P0~4_SPD_LED	Full / half duplex mode OFF: half-duplex ON: full-duplex BLINK: half-duplex and collision
P0~4_FDX_LED	10M link + Activity OFF: 10M link fail ON: 10M link ok and no TX/RX activity BLINK: 10M link ok and TX/RX activity

LED mode 3 (Default)	
P0~4_LNK_LED	link + Activity OFF: link fail ON,: link ok and no TX/RX activity BLINK: link ok and TX/RX activity
P0~4_SPD_LED	Speed OFF: 10M mode or link OFF ON: 100M mode link
P0~4_FDX_LED	Full / half duplex mode OFF: half-duplex ON: full-duplex BLINK: half-duplex and collision

Where OFF means in floating state
ON means in ground state if LED is low active, or in high voltage state if LED is high active
BLINK means in toggle state with ON 20ms and OFF 80ms
HI means in high voltage state
LO means in ground state



7.4 Internal PHY functions

7.4.1 100Base-TX Operation

The transmitter section contains the following functional blocks:
- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

7.4.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

7.4.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.
By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

7.4.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

7.4.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

7.4.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic one event.

7.4.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

7.4.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

7.4.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

7.4.2.1 Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

7.4.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

7.4.2.3 MLT-3 to NRZI Decoder

The DM8606C/DM8606CI decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

7.4.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

7.4.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

7.4.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

7.4.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

7.4.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

7.4.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols). The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

7.4.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM8606C/DM8606CI is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

7.4.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

7.4.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only when receiving operations.

7.4.6 Auto-Negotiation

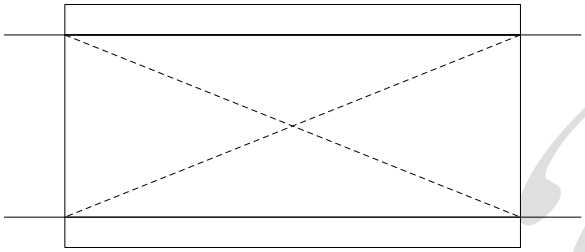
The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

7.4.7 Auto-MDIX Functional Description

The DM8606C/DM8606CI supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over) for internal port 0 ~ 4 PHY. A manual configuration by register bit for MDI or MDIX is still accepted.

When set to automatic, the polarity of MDI/MDIX controlled timing is generated by a 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX,
This feature is able to detect the required cable connection type.(straight through or crossed over) and make correction automatically

RX + /- from DM8606C/DM8606CI RX+/- to RJ45



TX + /- from DM8606C/DM8606CI TX+/- to RJ45

* MDI : _____
* MDIX : - - - - - - - - -

8 DC and AC Electrical Characteristics

8.1 Absolute Maximum Ratings (DM8606CI support -40°C~+85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VDD33	3.3V Supply Voltage	3.135	3.6	V	
VDD18	1.8V core power supply	1.71	1.95	V	
AVDD33	Analog power supply 3.3V	3.135	3.6	V	
AVDD18	Analog power supply 1.8V	1.71	1.95	V	
VIN	DC Input Voltage (VIN)	3.135	3.6	V	
TSTG	Storage Temperature range	-65	+150	°C	
TA	Ambient Temperature	0	+70	°C	
TA	Ambient Temperature	-40	+85	°C	DM8606CI
LT	Lead Temperature (TL, soldering, 10 sec.).	-	+245	°C	

8.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD33	3.3V Supply Voltage	3.135	3.30	3.465	V	
DVDD18	1.8V core power supply	1.71	1.80	1.89	V	
AVDD33	Analog power supply 3.3V	3.135	3.30	3.465	V	
AVDD18	Analog power supply 1.8V	1.71	1.80	1.89	V	
P_D (Power Dissipation)	5 ports 100BASE-TX	-	380	-	mA	1.8V only
		-	180	-	mA	3.3V only
	5 ports10BASE-TX		440		mA	TX idle, 1.8V only
			530		mA	100% utilization, 1.8V only
			70		mA	3.3V only
	5 ports Auto-negotiation or cable off		210		mA	1.8V only
			180		mA	3.3V only

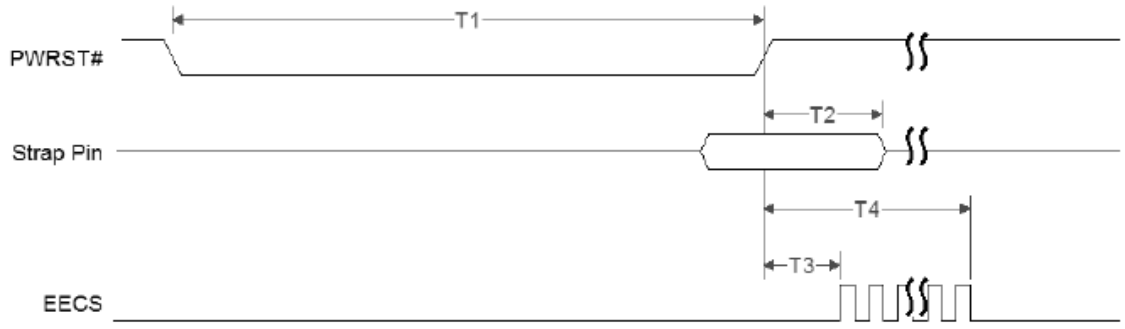
8.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

Note: Vcond1 = DVDD3 = 3.3V, DVDD18 = 1.8V, AVDD3 = 3.3V, AVDD18 = 1.8V.

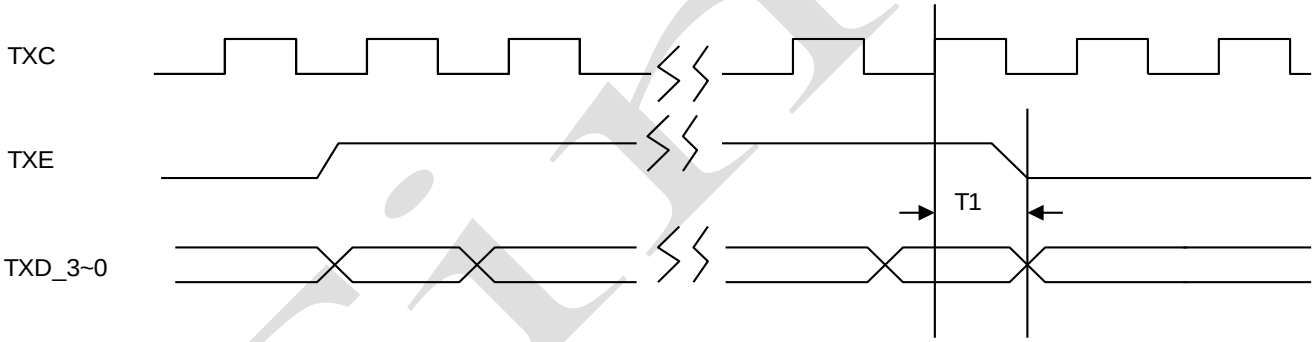
8.4 AC Characteristics

8.4.1 Power On Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PWRST# Low Period	1	-	-	ms	-
T2	Strap pin hold time with PWRST#	40	-	-	ns	-
T3	PWRST# high to EECS high	-	5	-	us	
T4	PWRST# high to EECS burst end	-	--	4	ms	

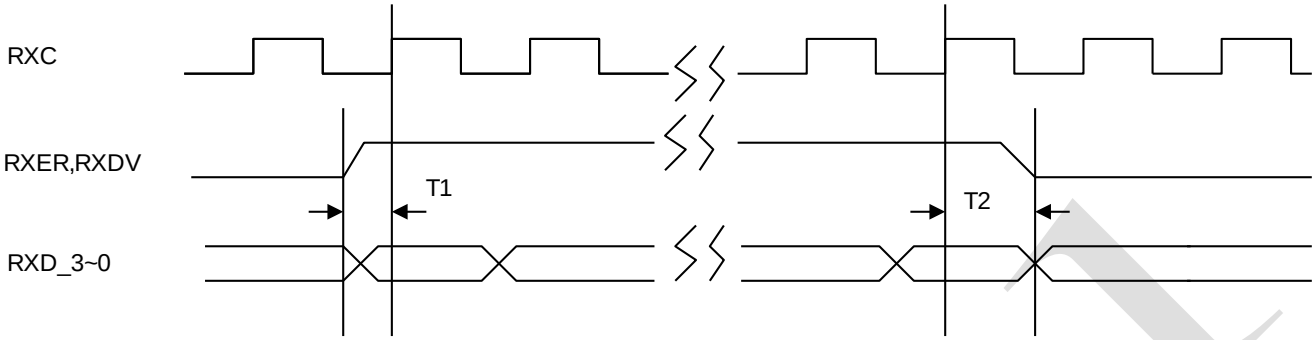
8.4.2 Port 4,5 MII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	TXE,TXD to TXC Rising Output Delay		8		ns

Note: TXC stand for pin P4_TXC in port 4 and pin P5_TXC in port 5
TXE stand for pin P4_TXE in port 4 and pin P5_TXE in port 5
TXD_3~0 stand for pin P4_TXD[3:0] in port 4 and pin P5_TXD[3:0] in port 5

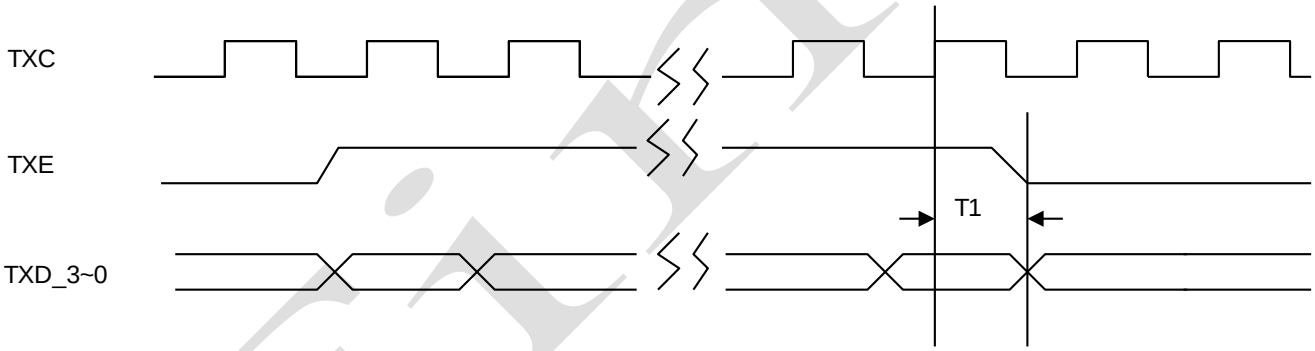
8.4.3 Port 4,5 MII Interface Receive Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RXER, RXDV and RXD to RXC Setup Time	5	-	-	ns
T2	RXER, RXDV and RXD to RXC Hold Time	5	-	-	ns

Note: RXC stand for pin P4_RXC in port 4 and pin P5_RXC in port 5
RXDV stand for pin P4_RXDV in port 4 and pin P5_RXDV in port 5
RXD_3~0 stand for pin P4_RXD[3:0] in port 4 and pin P5_RXD[3:0] in port 5

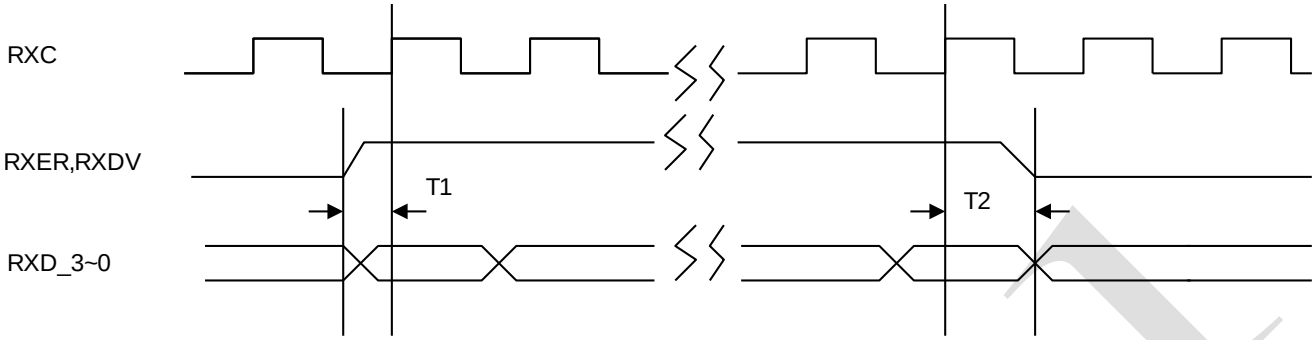
8.4.4 Port 4,5 RevMII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T0	100M MII Transmit Clock Period	-	40	-	ns
T0	10M MII Transmit Clock Period	-	400	-	ns
T1	TXE,TXD to TXC Rising Output Delay		8		ns

Note: TXC stand for pin P4_TXC in port 4 and pin P5_TXC in port 5
TXE stand for pin P4_TXE in port 4 and pin P5_TXE in port 5
TXD_3~0 stand for pin P4_TXD[3:0] in port 4 and pin P5_TXD[3:0] in port 5

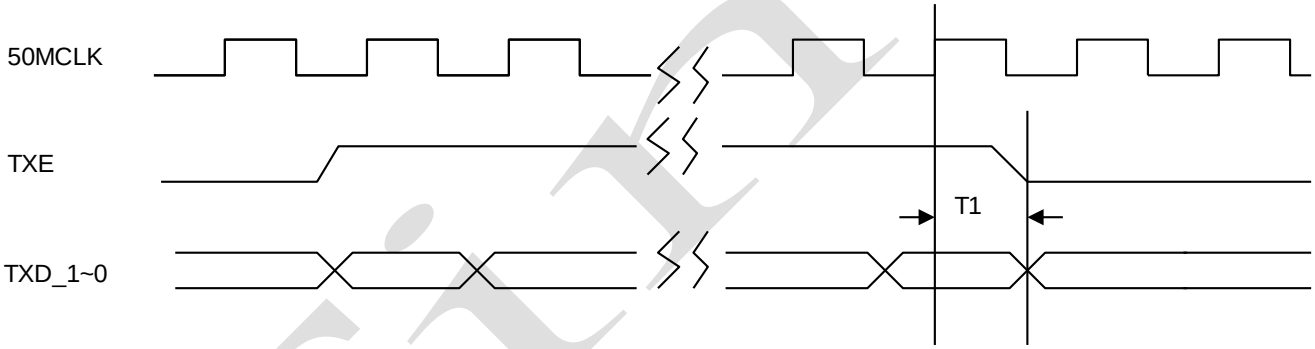
8.4.5 Port 4,5 RevMII Interface Receive Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RXER, RXDV and RXD to RXC Setup Time	5	-	-	ns
T2	RXER, RXDV and RXD to RXC Hold Time	5	-	-	ns

Note: RXC stand for pin P4_RXC in port 4 and pin P5_RXC in port 5
RXDV stand for pin P4_RXDV in port 4 and pin P5_RXDV in port 5
RXD_3~0 stand for pin P4_RXD[3:0] in port 4 and pin P5_RXD[3:0] in port 5

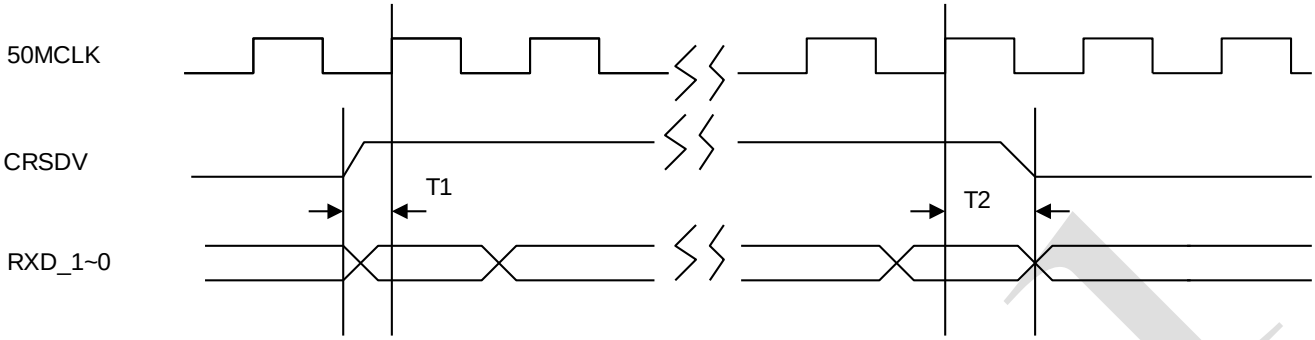
8.4.6 Port 4,5 RMII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	TXE,TXD to 50MCLK Rising Output Delay		8		ns

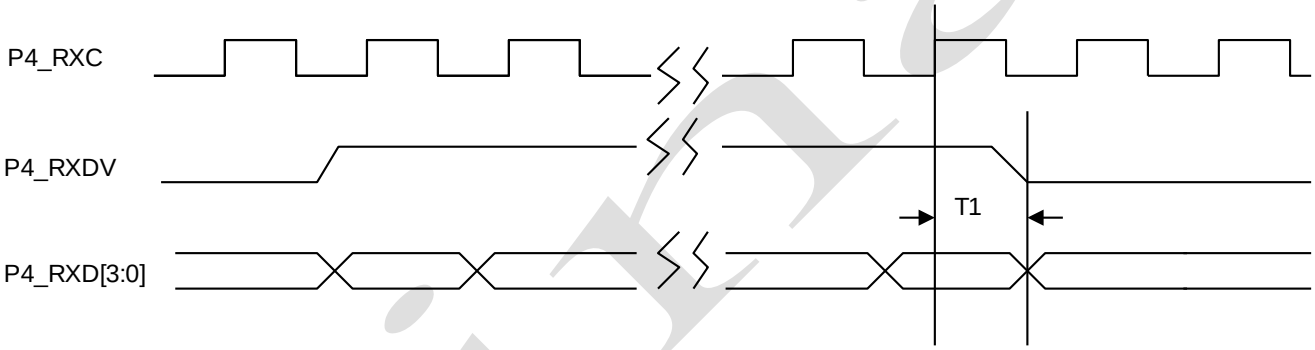
Note: 50MCLK stand for pin 50MCLK4 in port 4 and pin 50MCLK5 in port 5
TXE stand for pin P4_TXE in port 4 and pin P5_TXE in port 5
TXD_1~0 stand for pin P4_TXD[1:0] in port 4 and pin P5_TXD[1:0] in port 5

8.4.7 Port 4,5 RMII Interface Receive Timing



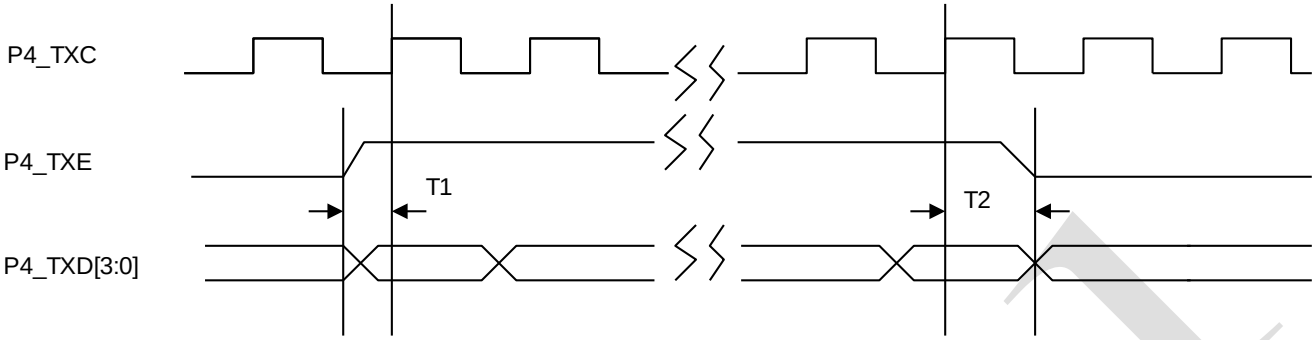
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CRSDV, RXD to 50MCLK Setup Time	4	-	-	ns
T2	CRSDV, RXD to 50MCLK Hold Time	2	-	-	ns

8.4.8 Port 4 PHY MII Interface Receive Timing



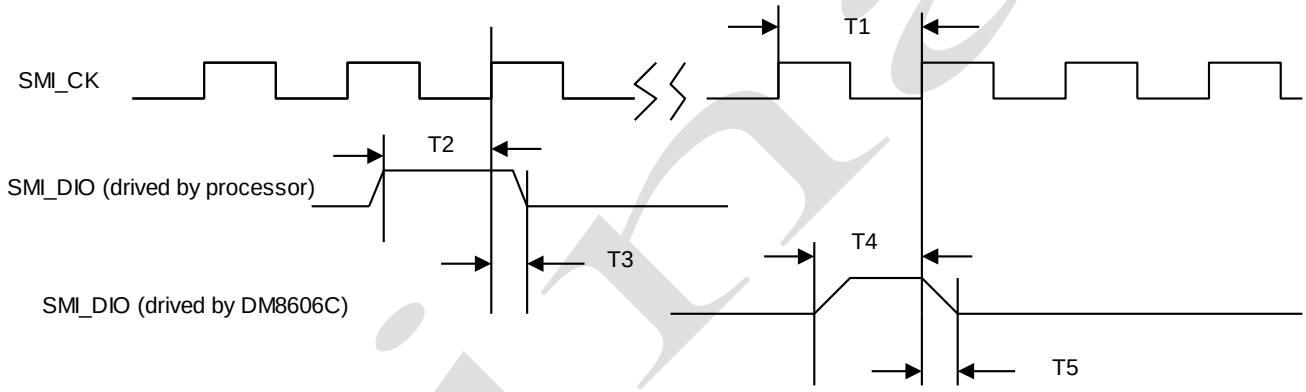
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	P4_RXDV,P4_RXD[3:0] to P4_RXC Rising Output Delay		8		ns

8.4.9 Port 4 PHY MII Interface Transmit Timing



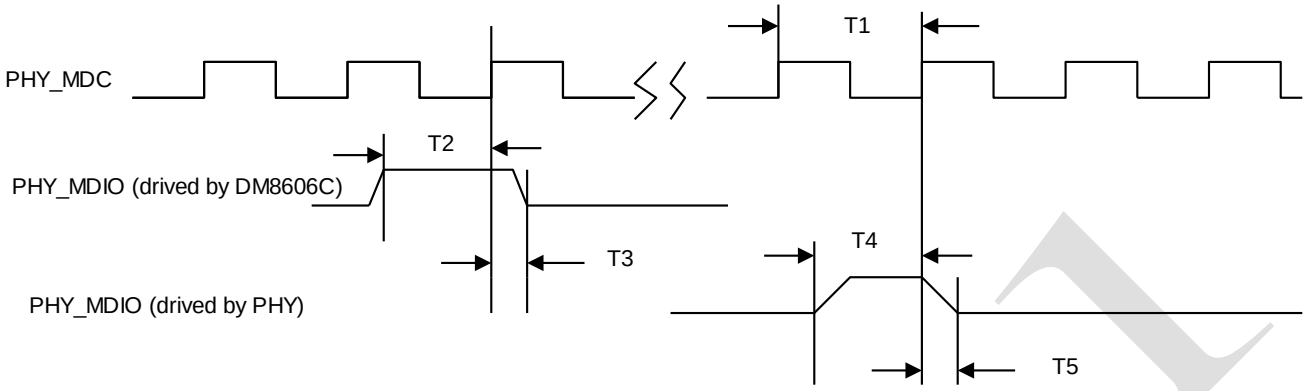
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	P4_TXE and P4_TXD[3:0] to P4_TXC Setup Time	5	-	-	ns
T2	P4_TXE and P4_TXD[3:0] to P4_TXC Hold Time	5	-	-	ns

8.4.10 Host SMI Interface Timing



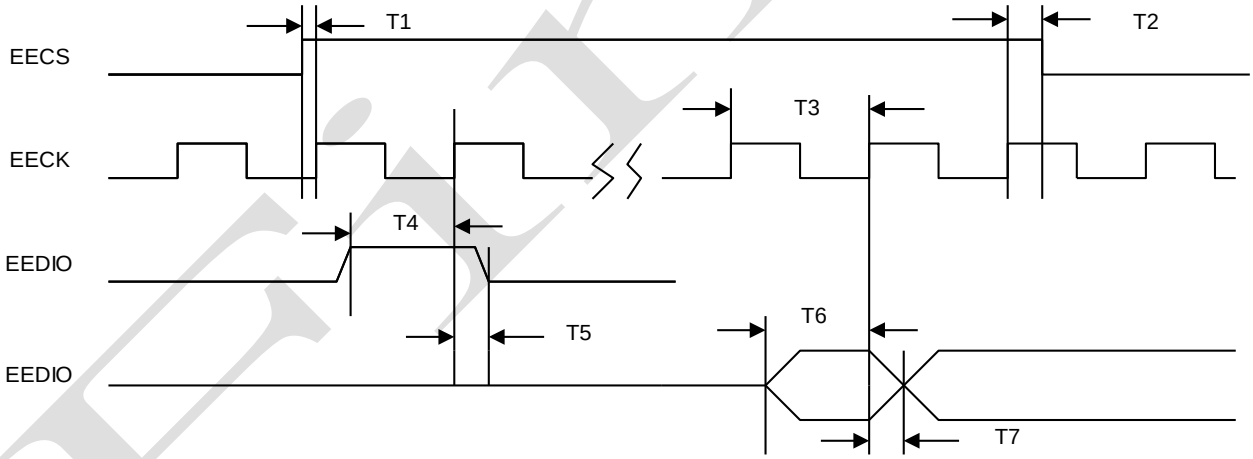
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SMI_CK Period	80	-	-	ns
T2	SMI_DIO by processor Setup Time	40	-	-	ns
T3	SMI_DIO by processor Hold Time	40	-	-	ns
T4	SMI_DIO by DM8606C/DM8606CI Setup Time	70			ns
T5	SMI_DIO by DM8606C/DM8606CI Hold Time		5		ns

8.4.11 PHY SMI Interface Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	PHY_MDC Period		1920	-	ns
T2	PHY_MDIO drived by DM8606C/DM8606CI Setup Time		960	-	ns
T3	PHY_MDIO drived by DM8606C/DM8606CI Hold Time		960	-	ns
T4	PHY_MDIO drived by PHY Setup Time	5		920	ns
T5	PHY_MDIO drived by PHY Hold Time	5		920	ns

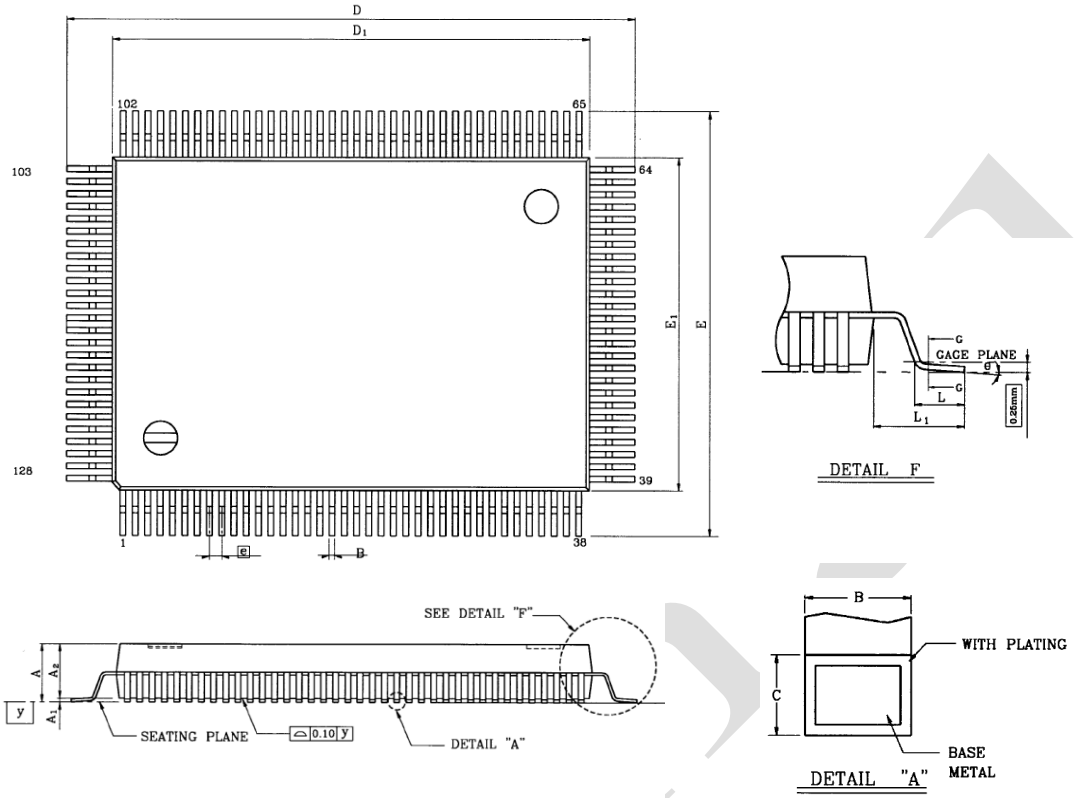
8.4.12 EEPROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECS Setup Time		480		ns
T2	EECS Hold Time		2080		ns
T3	EECK Frequency		0.39		MHz
T4	EEDIO Setup Time drive by DM8606C/DM8606CI		460		ns
T5	EEDIO Hold Time drive by DM8606C/DM8606CI		2100		ns
T6	EEDIO Setup Time drive by EEPROM	8			ns
T7	EEDIO Hold Time drive by EEPROM	8			ns

9 Package Information

128 Pins QFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	—	—	3.40		—	—	0.134
A_1	0.25	—	—		0.010	—	—
A_2	2.73	2.85	2.97		0.107	0.112	0.117
B	0.17	0.22	0.27		0.007	0.009	0.011
C	0.09	—	0.20		0.004	—	0.008
D	23.00	23.20	23.40		0.906	0.913	0.921
D_1	19.90	20.00	20.10		0.783	0.787	0.791
E	17.00	17.20	17.40		0.669	0.677	0.685
E_1	13.90	14.00	14.10		0.547	0.551	0.555
e	0.50 BSC				0.020 BSC		
L	0.73	0.88	1.03		0.029	0.035	0.041
L_1	1.60 BSC				0.063 BSC		
y	—	—	0.10		—	—	0.004
θ	0^0	—	7^0		0^0	—	7^0

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

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10 Ordering Information

Part Number	Pin Count	Package
DM8606CFP	128	QFP (Pb-Free)
DM8606CIFP	128	QFP (Pb-Free)

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