DAVICOM Semiconductor, Inc.

DM8806/DM8806I

6-Port 10/100Mb Fast Ethernet Smart Switch

DATA SHEET

Preliminary
Version: DM8806-14-3-DS-P02
January 9, 2013

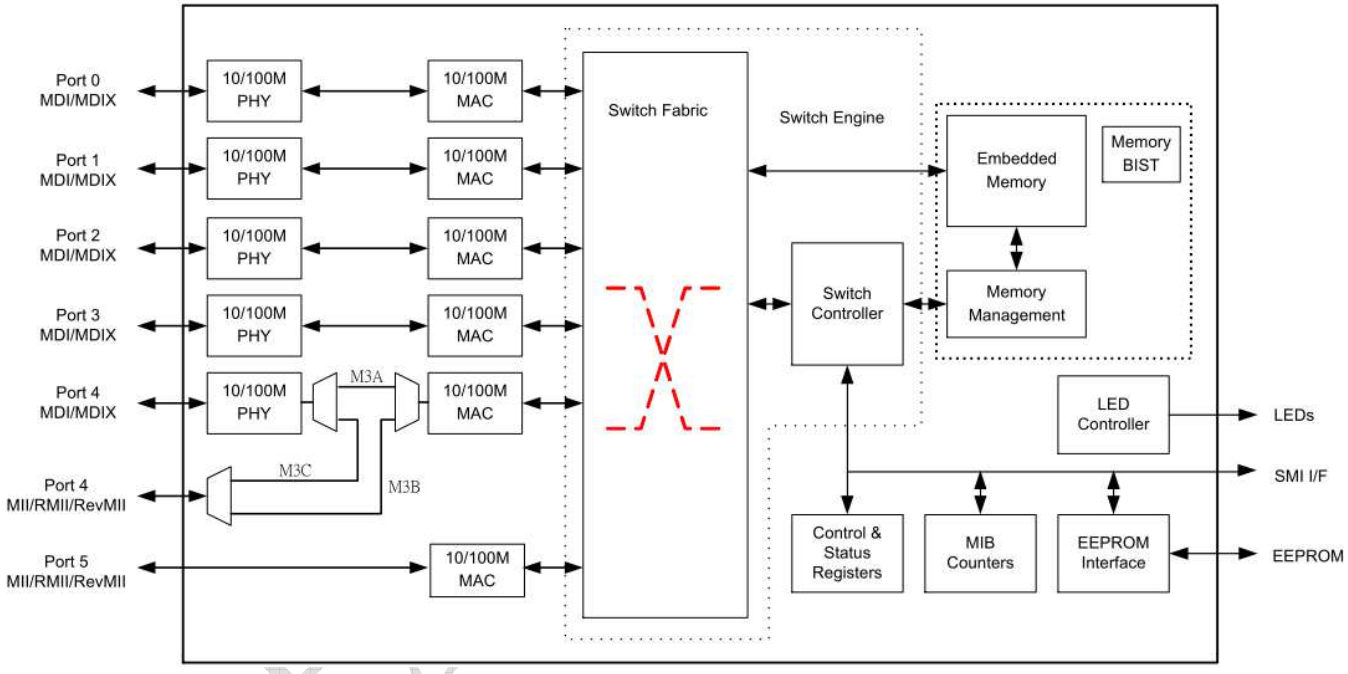
CONTENT

1. General Description

The DM8806 is a fully integrated and cost-effective industrial-temperature (DM8806I only) fast Ethernet switch controller with five 10/100Mb PHY, and five 10/100Mb MAC plus one 10/100Mb MAC with MII/RevMII/RMII.

The controller provides basic Layer-2 switch functions and advance IEEE 802.1Q VLAN, priority queuing scheme, IEEE 802.3az Energy Efficient Ethernet, IGMP snooping protocol, Spanning Tree protocol. The integrated 5 ports PHY are compliant with IEEE 802.3u standards. The MII/RMII/Reverse MII interface provides the flexibility to connect Ethernet 10/100M PHY devices.

2. Block Diagram



3. Features

- **Ethernet Switch Ports:**
  - Five 10/100Mb PHY built-in, that can be used for Copper or Fiber application
  - Port 4 support MII/RMII/RevMII interface to MAC or MII/RMII interface to internal PHY
  - Port 5 support MII/RMII/RevMII interface to MAC
- **Supports auto crossover function - HP Auto-MDIX**
- **Supports auto-polarity for 10Mbps**
- **Supports Store-and-Forward and Cut-Through switching approach**
- **Supports up to 2K accessible MAC address table**
- **Automatic aging scheme**
- **Flow control fully supported:**
  - IEEE 802.3x flow control in full-duplex mode
  - Back Pressure flow control in half-duplex mode
- **Supports packet length up to 1536(default)/1552/1800/2032 bytes**
- **Supports bandwidth control. Ingress and egress rate limit on each port.**
- **Supports broadcast storming filter function for broadcast, multicast and unknown unicast packets**
- **Supports source address filtering**
- **Supports high performance QoS function on each port:**
  - 4-level priority queues
  - Two type queue scheduling: Weighted Round Robin(WRR) and Strict Priority(SP)
  - Port-based, 802.1p, IPv6 ToS Priority
- **Supports up to 16 VLAN groups:**
  - 802.1Q port-base and tag-based VLAN
  - Full 12-bit VID, 4-bit FID
  - Shared VLAN Learning (SVL) and Independent VLAN Learning(IVL)
- **VLAN tag Insert/Remove function**
- **Leaky VLAN for unicast packets**
- **VLAN priority replace function**
- **Supports double tag (QinQ)**
- **Supports trunk ports**
- **Supports port-based and MAC-based mirror**

- **Supports hardware IGMP v1,v2 Snooping**
- **Supports hardware MLD v1 Snooping**
- **Supports IEEE 802.3az Energy Efficient Ethernet (EEE)**
- **Supports Link Fault Pass-through (LFP) and Far End Fault (FEF)**
- **Supports spanning tree function:**
  - IEEE 802.1D Spanning Tree Protocol (STP)
  - IEEE 802.1w Rapid STP (RSTP)
  - IEEE 802.1s Multiple STP (MSTP)
- **Supports 802.1x security function**
- **Supports WOL standby mode**
- **Supports Turbo RevMII mode on Port 4**
- **Supports internal generated RMII 50MHz clock output**
- **Supports optional EEPROM interface for configuration**
- **Supports 64-bit MIB counters for diagnostic**
- **Supports Serial Management Interface (SMI) for programming and diagnostics**
- **Supports interrupt pin for CPU application**
- **Supports special tag to carry control and status between Switch and CPU**
- **Supports four type LED display mode**
- **Commercial temperature range: -0°C to +70°C**
- **Industrial temperature range: -40°C to +85°C**
- **25MHz Crystal**
- **3.3V I/O with 5V tolerant**
- **0.18um technology, 1.8/3.3V power supply**
- **128-pin QFP package**

4. Pin Configuration

4.1 Pin Diagram

4.2 Pin Description

Buffer type:

I = Input,
I/O = Input / Output,
ANA = Analog,
PU = Internal pull-up (about 50K Ohm),
PUR= Internal pull-up during PWRST# period,
# = Asserted Low

O = Output,
O/D = Open Drain,
P = Power,
PD = Internal pull-down,
PDR = Internal pull-down during PWRST# period,

4.2.1 LED Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
42	P0_LNK_LED	PU 6mA	O	PHY 0 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 0 Link/Active status.
105	P0_SPD_LED	PUR 6mA	O	PHY 0 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 0 Speed status.
113	P0_FDX_LED	PUR 6mA	O	PHY 0 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 0 Duplex status.
43	P1_LNK_LED	PUR 6mA	O	PHY 1 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 1 Link/Active status.
104	P1_SPD_LED	PUR 6mA	O	PHY 1 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 1 Speed status.
112	P1_FDX_LED	PDR 6mA	O	PHY 1 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 1 Duplex status.
47	P2_LNK_LED	PUR 6mA	O	PHY 2 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 2 Link/Active status.
103	P2_SPD_LED	PUR 6mA	O	PHY 2 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 2 Speed status.
111	P2_FDX_LED	PUR 6mA	O	PHY 2 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 2 Duplex status.
48	P3_LNK_LED	PUR 6mA	O	PHY 3 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 3 Link/Active status.

102	P3_SPD_LED	PUR 6mA	O	PHY 3 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 3 Speed status.
110	P3_FDX_LED	PUR 6mA	O	PHY 3 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 3 Duplex status.
51	P4_LNK_LED	PUR 6mA	O	PHY 4 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 4 Link/Active status.
101	P4_SPD_LED	PUR 6mA	O	PHY 4 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 4 Speed status.
107	P4_FDX_LED	PUR 6mA	O	PHY 4 LED (output after reset) LED behavior can be configurable, see the LED Control Register 317h. By default, this pin is used to indicate Port 4 Duplex status.

4.2.2 EEPROM Interface

Pin No.	Pin Name	Buffer Type	I/O	Description
79	EEDIO	PD 4mA	I/O	EEPROM Data In/Output Drive/Read data to/from EEPROM
81	EECK	PDR 4mA	O	EEPROM Serial Clock Drive clock to EEPROM
80	EECS	PD 4mA	O	EEPROM Chip Selection. Drive chip selection to EEPROM

4.2.3 Clock Interface

Pin No.	Pin Name	Buffer Type	I/O	Description
120	X1	ANA	I	25 MHz Crystal /Oscillator Input Variation is limited to +/- 50 ppm.
121	X2	ANA	O	25 MHz Crystal Output When X1 is connected to oscillator, this pin should be left unconnected.

4.2.4 Network Interface

Pin No.	Pin Name	Buffer Type	I/O	Description
2 3	P0_TX- P0_TX+	ANA	I/O	Port 0 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
6 7	P0_RX- P0_RX+	ANA	I/O	Port 0 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
10 11	P1_TX- P1_TX+	ANA	I/O	Port 1 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
14 15	P1_RX- P1_RX+	ANA	I/O	Port 1 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
18 19	P2_TX- P2_TX+	ANA	I/O	Port 2 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
21 22	P2_RX- P2_RX+	ANA	I/O	Port 2 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
25 26	P3_TX- P3_TX+	ANA	I/O	Port 3 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
29 30	P3_RX- P3_RX+	ANA	I/O	Port 3 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
32 33	P4_RX+ P4_RX-	ANA	I/O	Port 4 TP RX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
36 37	P4_TX+ P4_TX-	ANA	I/O	Port 4 TP TX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
127	BGRES	ANA	I/O	Bandgap Pin Connect a 6.8K±1% precision resistor to AGND in application.
124	VCNTL	ANA	I/O	1.8V Voltage control to control external BJT
125	VREF	ANA	O	Voltage Reference Connect a 0.1u capacitor to ground in application.

4.2.5 Port 4 MAC MII/RevMII/RMII and PHY MII/RMII Interfaces

Port4 MAC MII Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
73 74	P4M_TXD3 P4M_TXD2	PDR 4mA	O	Transmit Data (bit 3 and 2)
77 78	P4M_TXD1 P4M_TXD0	PDR 4mA	O	Transmit Data (bit 1 and 0)
96	P4M_TXE	PDR 4mA	O	Transmit Enable
92	P4M_TXC	PDR	I	Transmit Clock.
91	P4M_CRS	PD	I	Carrier Sense
97	P4M_COL	PDR	I	Collision Detect.
95	P4M_RXC	PDR	I	Receive Clock
85	P4M_RXDV	-	I	Receive Data Valid
90 89	P4M_RXD3 P4M_RXD2	PD	I	Receive Data (bit 3 and 2)
86 84	P4M_RXD1 P4M_RXD0	PU	I	Receive Data (bit 1 and 0)

Port 4 MAC Reverse MII (RevMII) Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
73 74	P4M_TXD3 P4M_TXD2	PDR 4mA	O	Transmit Data (bit 3 and 2)
77 78	P4M_TXD1 P4M_TXD0	PDR 4mA	O	Transmit Data (bit 1 and 0)
96	P4M_TXE	PDR 4mA	O	Transmit Enable
92	P4M_TXC	PDR 4mA	O	Transmit Clock.
91	P4M_CRS	PD 4mA	O	Carrier Sense
97	P4M_COL	PDR 4mA	O	Collision Detect.
95	P4M_RXC	PDR	I	Receive Clock
85	P4M_RXDV	-	I	Receive Data Valid
90 89	P4M_RXD3 P4M_RXD2	PD	I	Receive Data (bit 3 and 2)
86 84	P4M_RXD1 P4M_RXD0	PU	I	Receive Data (bit 1 and 0)

Port 4 MAC Reduced MII (RMII) Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
73 74	P4M_TXD3 P4M_TXD2	PDR 4mA	O	Reserved (No connection)
77 78	P4M_TXD1 P4M_TXD0	PDR 4mA	O	Port4 RMII Transmit Data
96	P4M_TXE	PDR 4mA	O	Transmit Enable
92	P4M_REFCLK_O	PDR 4mA	O	Reference Clock 50MHz Output
91	P4M_CRS	PD	I	Reserved (No connection)
97	P4M_COL	PDR	I	Reserved (No connection)
95	P4M_REFCLK_I	PDR	I	Reference Clock 50MHz Input
85	P4M_CRSDV	-	I	Receive Data Valid
90 89	P4M_RXD3 P4M_RXD2	PD	I	Reserved (No connection)
86 84	P4M_RXD1 P4M_RXD0	PU	I	Receive Data

Port 4 PHY MII Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
90 89	P4P_TXD3 P4P_TXD2	PD	I	Transmit Data (bit 3 and 2)
86 84	P4P_TXD1 P4P_TXD0	PU	I	Transmit Data (bit 1 and 0)
85	P4P_TXE	-	I	Transmit Enable
92	P4P_TXC	PDR 4mA	O	Transmit Clock.
91	P4P_CRS	PD 4mA	O	Carrier Sense
97	P4P_COL	PDR 4mA	O	Collision Detect.
95	P4P_RXC	PDR 4mA	O	Receive Clock
96	P4P_RXDV	PDR 4mA	O	Receive Data Valid
73 74	P4P_RXD3 P4P_RXD2	PDR 4mA	O	Receive Data (bit 3 and 2)
77 78	P4P_RXD1 P4P_RXD0	PDR 4mA	O	Receive Data (bit 1 and 0)

Port 4 PHY Reduced MII (RMII) Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
90	P4P_REFCLK_I	PD	I	50MHz Input for Reference Clock
89	P4P_TXD2	PD	I	Reserved (No connection)
86 84	P4P_TXD1 P4P_TXD0	PU	I	Transmit Data
85	P4P_TXE	-	I	Transmit Enable
92	P4P_TXC	PDR 4mA	O	Reserved (No connection)
91	P4P_CRS	PD 4mA	O	Reserved (No connection)
97	P4P_COL	PDR 4mA	O	Reserved (No connection)
95	P4P_REFCLK_O	PDR 4mA	O	50MHz Output for Reference Clock
96	P4P_CRSDV	PDR 4mA	O	Receive Data Valid
73 74	P4P_RXD3 P4P_RXD2	PDR 4mA	O	Reserved (No connection)
77 78	P4P_RXD1 P4P_RXD0	PDR 4mA	O	Receive Data

4.2.6 Port 5 MAC Interfaces

Port 5 MII Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
59 60 61 63	P5_TXD3 P5_TXD2 P5_TXD1 P5_TXD0	PDR 4mA	O	Transmit Data
66	P5_TXE	PDR 4mA	O	Transmit Enable
67	P5_TXC	PDR	I	Transmit Clock.
57	P5_CRS	PDR	I	Carrier Sense
58	P5_COL	PDR	I	Collision Detect.
72	P5_RXC	PDR	I	Receive Clock
52	P5_RXDV	PD	I	Receive Data Valid
56 55 54 53	P5_RXD3 P5_RXD2 P5_RXD1 P5_RXD0	PD	I	Receive Data

Port 5 Reverse MII (RevMII) Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
59 60 61 63	P5_TXD3 P5_TXD2 P5_TXD1 P5_TXD0	PDR 4mA	O	Transmit Data
66	P5_TXE	PDR 4mA	O	Transmit Enable
67	P5_TXC	PDR 4mA	O	Transmit Clock Output.
57	P5_CRS	PDR 4mA	O	Carrier Sense Output
58	P5_COL	PDR 4mA	O	Collision Detect Output.
72	P5_RXC	PDR	I	Receive Clock
52	P5_RXDV	PD	I	Receive Data Valid
56 55 54 53	P5_RXD3 P5_RXD2 P5_RXD1 P5_RXD0	PD	I	Receive Data

Port 5 Reduced MII (RMII) pins

Pin No.	Pin Name	Buffer Type	I/O	Description
59 60	P5_TXD3 P5_TXD2	PDR	I	Reserved (No connection)
61 63	P5_TXD1 P5_TXD0	PDR 4mA	O	Transmit Data
66	P5_TXE	PDR 4mA	O	Transmit Enable
67	P5_REFCLK_O	PDR 4mA	O	50MHz Output for Reference Clock
57	P5_CRS	PDR	I	Reserved (No connection)
58	P5_COL	PDR	I	Reserved (No connection)
72	P5_REFCLK_I	PDR	I	50MHz Input for Reference Clock
52	P5_CRSDV	PD	I	Receive Data Valid
56 55	P5_RXD3 P5_RXD2	PD	I	Reserved (No connection)
54 53	P5_RXD1 P5_RXD0	PD	I	Receive Data

4.2.7 Miscellaneous Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
40	SMI_DIO	PD 4mA	I/O	Serial Management Data Input/output as CPU interface
44	SMI_CK	PD	I	Serial Management Data Clock as CPU interface
39	PHY_MDIO	PD 4mA	I/O	MII Serial Management Data Input/output as External PHY interface
68	PHY_MDC	PDR 4mA	O	MII Serial Management Data Clock as External PHY interface
65	INTR	-	O	Interrupt signals to external CPU
93	STRAP_DIS	PD	I	Strap pins disabled 0: Strap pins enabled 1: No strap pin function
62 100 98	P4_CFG P4_SET1 P4_SET0	PD PDR PUR	I I I	Port 4 operation mode { P4_CFG, P4_SET1, P4_SET0} 0 0 0 Use internal PHY (M3A) 0 0 1 MAC MII/RMII/RevMII (M3B) 1 X X PHY MII/RMII (M3C)
119	PWRST#	-	I	Power on Reset Low active with minimum 10ms
41 69 108	TEST3 TEST2 TEST1	PD PD PD	I I I	Test pins Tie TEST3 to ground in application Tie TEST2 and TEST1 to DVDD33 in application
114	VP_EN	PDR	I	Virtual PHY Enable 0: Disable 1: Enable
106	WOL_EN	PDR	I	Wake on Lan Standby 0: Disable 1: Enable to detect WoL Magic Packet event
115 117	GPIO0 GPIO1	PDR 4mA	I/O	GPIO Pin

4.2.8 Power Pins

Pin No.	Pin Name	Buffer Type	I/O	Description
49, 71 88, 109	DVDD33	PWR	P	Digital 3.3V power
46, 75 82, 94 116	DVDD18	PWR	P	Digital 1.8V power
45, 50 64, 70 76, 83 87, 99 118	DGND	GND	P	Digital GND
8, 16 23, 31 128	AVDD33	PWR	P	Analog 3.3V power
1, 9 17, 24 38, 122	AVDD18	PWR	P	Analog 1.8V power
4, 5 12, 13 20, 27 28, 34 35, 123 126	AGND	GND	P	Analog GND

4.3 Strap Pins Table

1: pull-up with 1K~10K, 0: pull-down with 1K~10K

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>51</td><td>P4_LNK_LED</td><td>Port 4 PHY TP mode in M3A or M3C mode
0: Fiber mode
1: Copper mode (default)</td></tr>
<tr><td>43</td><td>P1_LNK_LED</td><td>802.3az Energy Efficient Ethernet function of all ports.
0 : Disable, output high to active LED
1 : Enable, output low to active LED (default)</td></tr>
<tr><td>101</td><td>P4_SPD_LED</td><td>When in M3B and Port4 force mode
0 : Link OFF
1 : Link ON (default)</td></tr>
<tr><td>102
103</td><td>P3_SPD_LED
P2_SPD_LED</td><td>Port 4 in M3B Mode
{P3_SPD_LED, P2_SPD_LED}
<table>
<tr><td>0</td><td>0</td><td>RevMII with TXC4 turbo clock</td></tr>
<tr><td>0</td><td>1</td><td>RMII</td></tr>
<tr><td>1</td><td>0</td><td>MII</td></tr>
<tr><td>1</td><td>1</td><td>RevMII with TXC4 25MHz/2.5MHz clock (default)</td></tr>
</table>
Port 4 in M3C Mode
{P3_SPD_LED, P2_SPD_LED}
<table>
<tr><td>0</td><td>X</td><td>TP_RMII</td></tr>
<tr><td>1</td><td>X</td><td>TP_MII (default)</td></tr>
</table></td></tr>
<tr><td>104</td><td>P1_SPD_LED</td><td>When in M3B,Port4 in force mode and (P3_SPD_LED,P2_SPD_LED)≠(0,0)
0 : 10M mode
1 : 100M mode (default)

If (P3_SPD_LED, P2_SPD_LED) = (0,0), it can be used to set P4_TXC frequency.
{P1_SPD_LED, P0_SPD_LED}
<table>
<tr><td>0</td><td>0</td><td>125MHz</td></tr>
<tr><td>0</td><td>1</td><td>100MHz</td></tr>
<tr><td>1</td><td>0</td><td>50MHz</td></tr>
<tr><td>1</td><td>1</td><td>25MHz (default)</td></tr>
</table></td></tr>
<tr><td>105</td><td>P0_SPD_LED</td><td>When in M3B,Port4 in force mode and
(P3_SPD_LED, P2_SPD_LED)≠(0,0)
0 : Half-duplex mode
1 : Full-duplex mode (default)

If (P3_SPD_LED, P2_SPD_LED) = (0,0)
See description of P1_SPD_LED</td></tr>
<tr><td>107</td><td>P4_FDX_LED</td><td>When Port5 in force mode and (P3_FDX_LED, P2_FDX_LED) ≠(0,0)
0 : Link OFF
1 : Link ON (default)</td></tr>
</table>

<table>
<tr><td>110
111</td><td>P3_FDX_LED,
P2_FDX_LED</td><td>Port 5 Operation Mode
{P3_FDX_LED, P2_FDX_LED}
<table>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>RMII</td></tr>
<tr><td>1</td><td>0</td><td>MII</td></tr>
<tr><td>1</td><td>1</td><td>RevMII (default)</td></tr>
</table></td></tr>
<tr><td>112</td><td>P1_FDX_LED</td><td>When Port5 in force mode and (P3_FDX_LED, P2_FDX_LED)≠(0,0)
0 : 10M mode (default)
1 : 100M mode</td></tr>
<tr><td>113</td><td>P0_FDX_LED</td><td>When Port5 in force mode and (P3_FDX_LED, P2_FDX_LED)≠(0,0)
0 : Half-duplex mode
1 : Full-duplex mode (default)</td></tr>
<tr><td>115</td><td>GPIO0</td><td>Flow Control in PHY Register 4 bit 10
0: Enable PHY flow control (default)
1: Disable PHY flow control</td></tr>
<tr><td>80</td><td>EECS</td><td>Port 5 link/duplex/speed mode in MII/RMII
0: Force mode (default)
1: PHY_MDC/PHY_MDIO polling mode</td></tr>
<tr><td>81</td><td>EECK</td><td>When in M3B and Port 4 link/duplex/speed mode in MII/RMII
0: Force mode (default)
1: MDC_EXT/MDIO_EXT polling mode

When in M3B and Port 4 link/duplex/speed mode in RevMII
X: force mode</td></tr>
<tr><td>68</td><td>PHY_MDC</td><td>Only Port0 and Port1 support Trunk Ports Function
0: Disable (default)
1: Enable

More trunk setting details please refer to bit 11~8 of REG 212h</td></tr>
</table>

5. Control and Status Register Set

The DM8806 implements several control and status registers (CSRs), which can be accessed by the host SMI interface via SMI_CK and SMI_DIO pins. The serial format of host SMI can be referenced in Section 7.3. The absolute address in the following register table is the 10-bit R9~R0 field in the SMI format. For easy to understanding, the 10-bit **absolute address** can be divided to 5-bit **PHY address** plus 5-bit **register address** like used in general MII serial format. All CSRs are set to their default values by hardware or software reset unless specified

5.1 Register Table

Register Name	PHY Address	Register Address	Absolute Address
Internal PHY Registers			
Port 0 PHY Basic Mode Control	02h	00h	040h
Port 0 PHY Basic Mode Status	02h	01h	041h
Port 0 PHY ID 1	02h	02h	042h
Port 0 PHY ID 2	02h	03h	043h
Port 0 PHY Auto-N Advertisement	02h	04h	044h
Port 0 PHY Auto-N Link Partner Ability	02h	05h	045h
Port 0 PHY Auto-N Expansion	02h	06h	046h
Port 0 PHY Standard Reserved	02h	07h~0Fh	047h~04Fh
Port 0 PHY Vendor Specific	02h	10h~1Fh	050h~05Fh
Port 1 PHY Control	03h	00h	060h
Port 1 PHY Status	03h	01h	061h
Port 1 PHY ID 1	03h	02h	062h
Port 1 PHY ID 2	03h	03h	063h
Port 1 PHY Auto-N Advertisement	03h	04h	064h
Port 1 PHY Auto-N Link Partner Ability	03h	05h	065h
Port 1 PHY Auto-N Expansion	03h	06h	066h
Port 1 PHY Standard Reserved	03h	07h~0Fh	067h~06Fh
Port 1 PHY Vendor Specific	03h	10h~1Fh	070h~07Fh
Port 2 PHY Control	04h	00h	080h
Port 2 PHY Status	04h	01h	081h
Port 2 PHY ID 1	04h	02h	082h
Port 2 PHY ID 2	04h	03h	083h
Port 2 PHY Auto-N Advertisement	04h	04h	084h
Port 2 PHY Auto-N Link Partner Ability	04h	05h	085h
Port 2 PHY Auto-N Expansion	04h	06h	086h
Port 2 PHY Standard Reserved	04h	07h~0Fh	087h~08Fh
Port 2 PHY Vendor Specific	04h	10h~1Fh	090h~09Fh
Port 2 PHY Control	05h	00h	0A0h
Port 3 PHY Status	05h	01h	0A1h
Port 3 PHY ID 1	05h	02h	0A2h
Port 3 PHY ID 2	05h	03h	0A3h
Port 3 PHY Auto-N Advertisement	05h	04h	0A4h
Port 3 PHY Auto-N Link Partner Ability	05h	05h	0A5h
Port 3 PHY Auto-N Expansion	05h	06h	0A6h
Port 3 PHY Standard Reserved	05h	07h~0Fh	0A7h~0AFh
Port 3 PHY Vendor Specific	05h	10h~1Fh	0B0h~0BFh
Port 3 PHY Control	06h	00h	0C0h
Port 4 PHY Status	06h	01h	0C1h
Port 4 PHY ID 1	06h	02h	0C2h

Port 4 PHY ID 2	06h	03h	0C3h
Port 4 PHY Auto-N Advertisement	06h	04h	0C4h
Port 4 PHY Auto-N Link Partner Ability	06h	05h	0C5h
Port 4 PHY Auto-N Expansion	06h	06h	0C6h
Port 4 PHY Standard Reserved	06h	07h~0Fh	0C7h~0CFh
Port 4 PHY Vendor Specific	06h	10h~1Fh	0D0h~0DFh
Reserved	07h	00h~1Fh	0F0h~10Fh
Switch Per-Port Registers			
Port 0 Port Status	08h	10h	110h
Port 0 Basic Control 0	08h	11h	111h
Port 0 Basic Control 1	08h	12h	112h
Port 0 Block Contrl 0	08h	13h	113h
Port 0 Block Contrl 1	08h	14h	114h
Port 0 Bandwidth Control	08h	15h	115h
Port 0 VLAN Tag Infomation	08h	16h	116h
Port 0 Priority & VLAN Control	08h	17h	117h
Port 0 Security Control	08h	18h	118h
Port 0 Spanning Tree state Control	08h	19h	119h
Port 0 Memory Configuration	08h	1Ah	11Ah
Port 0 Discard packet limitation	08h	1Bh	11Bh
Reserved	08h	1Ch	11Ch
Reserved	08h	1Dh	11Dh
Port 0 Energy Efficient Ethernet Control	08h	1Eh	11Eh
Reserved	08h~09h	1Fh~0Fh	11Fh~12Fh
Port 1 Port Status	09h	10h	130h
Port 1 Basic Control 0	09h	11h	131h
Port 1 Basic Control 1	09h	12h	132h
Port 1 Block Contrl 0	09h	13h	133h
Port 1 Block Contrl 1	09h	14h	134h
Port 1 Bandwidth Control	09h	15h	135h
Port 1 VLAN Tag Infomation	09h	16h	136h
Port 1 Priority & VLAN Control	09h	17h	137h
Port 1 Security Control	09h	18h	138h
Port 1 Spanning Tree state Control	09h	19h	139h
Port 1 Memory Configuration	09h	1Ah	13Ah
Port 1 Discard packet limitation	09h	1Bh	13Bh
Reserved	09h	1Ch	13Ch
Reserved	09h	1Dh	13Dh
Port 1 Energy Efficient Ethernet Control	09h	1Eh	13Eh
Reserved	09h~0Ah	1Fh~0Fh	13Fh~14Fh
Port 2 Port Status	0Ah	10h	150h
Port 2 Basic Control 0	0Ah	11h	151h
Port 2 Basic Control 1	0Ah	12h	152h
Port 2 Block Contrl 0	0Ah	13h	153h
Port 2 Block Contrl 1	0Ah	14h	154h
Port 2 Bandwidth Control	0Ah	15h	155h
Port 2 VLAN Tag Infomation	0Ah	16h	156h
Port 2 Priority & VLAN Control	0Ah	17h	157h
Port 2 Security Control	0Ah	18h	158h
Port 2 Spanning Tree state Control	0Ah	19h	159h
Port 2 Memory Configuration	0Ah	1Ah	15Ah
Port 2 Discard packet limitation	0Ah	1Bh	15Bh

Reserved	0Ah	1Ch	15Ch
Reserved	0Ah	1Dh	15Dh
Port 2 Energy Efficient Ethernet Control	0Ah	1Eh	15Eh
Reserved	0Ah~0Bh	1Fh~0Fh	15Fh~16Fh
Port 3 Port Status	0Bh	10h	170h
Port 3 Basic Control 0	0Bh	11h	171h
Port 3 Basic Control 1	0Bh	12h	172h
Port 3 Block Contrl 0	0Bh	13h	173h
Port 3 Block Contrl 1	0Bh	14h	174h
Port 3 Bandwidth Control	0Bh	15h	175h
Port 3 VLAN Tag Infomation	0Bh	16h	176h
Port 3 Priority & VLAN Control	0Bh	17h	177h
Port 3 Security Control	0Bh	18h	178h
Port 3 Spanning Tree state Control	0Bh	19h	179h
Port 3 Memory Configuration	0Bh	1Ah	17Ah
Port 3 Discard packet limitation	0Bh	1Bh	17Bh
Reserved	0Bh	1Ch	17Ch
Reserved	0Bh	1Dh	17Dh
Port 3 Energy Efficient Ethernet Control	0Bh	1Eh	17Eh
Reserved	0Bh~0Ch	1Fh~0Fh	17Fh~18Fh
Port 4 Port Status	0Ch	10h	190h
Port 4 Basic Control 0	0Ch	11h	191h
Port 4 Basic Control 1	0Ch	12h	192h
Port 4 Block Contrl 0	0Ch	13h	193h
Port 4 Block Contrl 1	0Ch	14h	194h
Port 4 Bandwidth Control	0Ch	15h	195h
Port 4 VLAN Tag Infomation	0Ch	16h	196h
Port 4 Priority & VLAN Control	0Ch	17h	197h
Port 4 Security Control	0Ch	18h	198h
Port 4 Spanning Tree state Control	0Ch	19h	199h
Port 4 Memory Configuration	0Ch	1Ah	19Ah
Port 4 Discard packet limitation	0Ch	1Bh	19Bh
Reserved	0Ch	1Ch	19Ch
Reserved	0Ch	1Dh	19Dh
Port 4 Energy Efficient Ethernet Control	0Ch	1Eh	19Eh
Reserved	0Ch~0Dh	1Fh~0Fh	19Fh~1AFh
Port 5 Port Status	0Dh	10h	1B0h
Port 5 Basic Control 0	0Dh	11h	1B1h
Port 5 Basic Control 1	0Dh	12h	1B2h
Port 5 Block Contrl 0	0Dh	13h	1B3h
Port 5 Block Contrl 1	0Dh	14h	1B4h
Port 5 Bandwidth Control	0Dh	15h	1B5h
Port 5 VLAN Tag Infomation	0Dh	16h	1B6h
Port 5 Priority & VLAN Control	0Dh	17h	1B7h
Port 5 Security Control	0Dh	18h	1B8h
Port 5 Spanning Tree state Control	0Dh	19h	1B9h
Port 5 Memory Configuration	0Dh	1Ah	1BAh
Port 5 Discard packet limitation	0Dh	1Bh	1BBh
Reserved	0Dh	1Ch~1Dh	1BCh~1BDh
Port 5 Energy Efficient Ethernet Control	0Dh	1Eh	1BEh
Reserved	0Dh	1Fh	1BFh
Reserved	0Eh~0Fh	00h~1Fh	1C0h~20Fh

Switch Engine Registers			
Switch Status	10h	10h	210h
Switch Reset	10h	11h	211h
Switch Control	10h	12h	212h
CPU Port & Mirror Control	10h	13h	213h
Special Tag Ether-Type	10h	14h	214h
Global Learning & Aging Control	10h	15h	215h
Reserved	10h	16h	216h
VLAN Priority Map	10h	17h	217h
TOS Priority Map 0	10h	18h	218h
TOS Priority Map 1	10h	19h	219h
TOS Priority Map 2	10h	1Ah	21Ah
TOS Priority Map 3	10h	1Bh	21Bh
TOS Priority Map 4	10h	1Ch	21Ch
TOS Priority Map 5	10h	1Dh	21Dh
TOS Priority Map 6	10h	1Eh	21Eh
TOS Priority Map 7	10h	1Fh	21Fh
MIB Counter Disable	11h	10h	230h
MIB Counter Control	11h	11h	231h
MIB Counter Data Low	11h	12h	232h
MIB Counter Data High	11h	13h	233h
Special Packet Control 0	11h	14h	234h
Special Packet Control 1	11h	15h	235h
Special Packet Control 2	11h	16h	236h
Special Packet Control 3	11h	17h	237h
Special Packet Control 4	11h	18h	238h
Special Packet Control 5	11h	19h	239h
Special Packet Control 6	11h	1Ah	23Ah
Special Packet Control 7	11h	1Bh	23Bh
Special Packet Control 8	11h	1Ch	23Ch
QinQ TPID	11h	1Dh	23Dh
VLAN Mode & Rule Control	11h	1Eh	23Eh
VLAN Table – Valid Control	11h	1Fh	23Fh
VLAN Table – ID_0H	12h	10h	250h
VLAN Table – ID_1H	12h	11h	251h
VLAN Table – ID_2H	12h	12h	252h
VLAN Table – ID_3H	12h	13h	253h
VLAN Table – ID_4H	12h	14h	254h
VLAN Table – ID_5H	12h	15h	255h
VLAN Table – ID_6H	12h	16h	256h
VLAN Table – ID_7H	12h	17h	257h
VLAN Table – ID_8H	12h	18h	258h
VLAN Table – ID_9H	12h	19h	259h
VLAN Table – ID_AH	12h	1Ah	25Ah
VLAN Table – ID_BH	12h	1Bh	25Bh
VLAN Table – ID_CH	12h	1Ch	25Ch
VLAN Table – ID_DH	12h	1Dh	25Dh
VLAN Table – ID_EH	12h	1Eh	25Eh
VLAN Table – ID_FH	12h	1Fh	25Fh
VLAN Table – MEMBER_0H	13h	10h	270h
VLAN Table – MEMBER_1H	13h	11h	271h
VLAN Table – MEMBER_2H	13h	12h	272h

VLAN Table – MEMBER_3H	13h	13h	273h
VLAN Table – MEMBER_4H	13h	14h	274h
VLAN Table – MEMBER_5H	13h	15h	275h
VLAN Table – MEMBER_6H	13h	16h	276h
VLAN Table – MEMBER_7H	13h	17h	277h
VLAN Table – MEMBER_8H	13h	18h	278h
VLAN Table – MEMBER_9H	13h	19h	279h
VLAN Table – MEMBER_AH	13h	1Ah	27Ah
VLAN Table – MEMBER_BH	13h	1Bh	27Bh
VLAN Table – MEMBER_CH	13h	1Ch	27Ch
VLAN Table – MEMBER_DH	13h	1Dh	27Dh
VLAN Table – MEMBER_EH	13h	1Eh	27Eh
VLAN Table – MEMBER_FH	13h	1Fh	27Fh
VLAN Table – Priority Enable	14h	10h	290h
VLAN Table – Priority Replace Enable	14h	11h	291h
VLAN Table – STP Index Enable	14h	12h	292h
VLAN Table – Misc_0	14h	13h	293h
VLAN Table – Misc_1	14h	14h	294h
VLAN Table – Misc_2	14h	15h	295h
VLAN Table – Misc_3	14h	16h	296h
VLAN Table – Misc_4	14h	17h	297h
VLAN Table – Misc_5	14h	18h	298h
VLAN Table – Misc_6	14h	19h	299h
VLAN Table – Misc_7	14h	1Ah	29Ah
Snooping Control 0	14h	1Bh	29Bh
Snooping Control 1	14h	1Ch	29Ch
Reserved	14h~15h	1Dh~0Fh	29Dh~2AFh
Address Table Control & Status	15h	10h	2B0h
Address Table Data 0	15h	11h	2B1h
Address Table Data 1	15h	12h	2B2h
Address Table Data 2	15h	13h	2B3h
Address Table Data 3	15h	14h	2B4h
Address Table Data 4	15h	15h	2B5h
Reserved	15h	16h~17h	2B6h~2B7h
Address Registers for Magic Packet	15h	18h~1Ah	2B8h~2BAh
WoL Control Register	15h	1Bh	2BBh
Reserved	15h~16h	1Ch~0Fh	2BCh~2CFh
General Purpose I/O Control	16h	10h	2D0h
Reserved	16h~18h	11h~0Fh	2D1h~30Fh
Vendor ID	18h	10h	310h
Product ID	18h	11h	311h
Reserved	18h	12h~13h	312h~313h
Port 4 MAC Control	18h	14h	314h
Port 5 MAC Control	18h	15h	315h
Fiber Control	18h	16h	316h
IRQ and LED Control	18h	17h	317h
Interrupt Status Register	18h	18h	318h
Interrupt Mask & Control Register	18h	19h	319h
EEPROM Control & Address	18h	1Ah	31Ah
EEPROM Data	18h	1Bh	31Bh
Monitor Register 0	18h	1Ch	31Ch
Monitor Register 1	18h	1Dh	31Dh

Monitor Register 2	18h	1Eh	31Eh
Monitor Register 3	18h	1Fh	31Fh
Memory Access Enable	19h	10h	330h
Memory Address	19h	11h	331h
Memory Read Data (Dummy Read)	19h	12h	332h
Memory Read Data	19h	13h	333h
Memory Write Data Bit 15~0 Register	19h	14h	334h
Memory Write Data Bit 7~0 Register	19h	15h	335h
Memory Write Data Bit 15~8 Register	19h	16h	336h
Reserved	19h	17h	337h
System clock Select Register	19h	18h	338h
Serial Bus Error Check Register	19h	19h	339h
Reserved	19h	1Ah~1Dh	33Ah~33Ch
Virtual PHY Control	19h	1Dh	33Dh
PHY Control Test	19h	1Eh	33Eh
Reserved	19h	1Fh	33Fh
Reserved	1Ah~1Ch	00h~0Fh	340h~38Fh
Reserved	1Ch~1Fh	10h~1Fh	390h~3FFh

Note:

PHY_ADR = <PHY Address> fields of SMI frame

REG_ADR = <Register Address> fields of SMI frame

ABS_ADR = { PHY_ADR[4:0], REG_ADR[4:0] }

Key to Default

In the register description that follows, the default column takes the form: <Reset Value>, <Access Type>

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
?H	Bits set to hex. value
X	No default value

P	Power on reset default value
S	Software reset, by Reg. 211H bit 1, default value
Y	Default value from PHY software reset by per port PHY register 0 bit 15
E	Default value from EEPROM setting
T	Default value from strap pin

<Access Type>:

RO	Read only
RW	Read/Write
R/C	Read and Clear
RW/C1	Read/Write and Cleared by write 1
WO	Write only
R/WC	Read/Write and auto-cleared

Reserved bits should be written with 0.
Reserved bits are undefined on read access.

5.2 Internal PHY Registers

5.2.1 Port 0~4 PHY Control Register

P0(040H), P1(060H), P2(080H), P3(0A0H), P4(0C0H)

Bit	Bit Name	Default	Description
15	Reset	P0 RW/SC	Reset This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed 0: Normal operation 1: Software reset
14	Loopback	PY0 RW	Loopback Loop-back control enable When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs 0: Normal operation 1: Loop-back enabled
13	Speed selection	PY1 RW	Speed Select Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled (bit 12 is set), this bit will return auto-negotiation selected medium type 0: 10Mbps 1: 100Mbps
12	Auto-negotiation enable	PT1 RW	Auto-negotiation Enable Enable the ability of auto-negotiation process. 0: Disable 1: Enable
11	Power down	PY0 RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 0: Normal operation 1: Power down
10	Isolate	PY0 RW	Isolate Force to 0 in application.
9	Restart Auto-negotiation	PY0 RW/SC	Restart Auto-negotiation Re-initiates the auto-negotiation process. If the auto-negotiation ability is disabled, this bit has no function and it should be cleared. This bit is self-clearing. 0: Normal operation 1: Restart auto-negotiation process
8	Duplex mode	PY1 RW	Duplex Mode If auto-negotiation ability is disabled, this bit can be set manually (Read/Write). If auto-negotiation ability is enabled, this bit reflects the result of auto-negotiation (Read only). 0: Half duplex operation 1: Full duplex operation
7:0	Reserved	P0 RO	Reserved Read as 0, ignore on write

5.2.2 Port 0~4 PHY Status Register

P0(041H), P1(061H), P2(081H), P3(0A1H), P4(0C1H)

Bit	Bit Name	Default	Description
15	100BASE-T4	P0 RO	100BASE-T4 Capable 0: No 100BASE-T4 capable 1: 100BASE-T4 capable
14	100BASE-TX full-duplex	P1 RO	100BASE-TX Full Duplex Capable 0: No 100BASE-TX full duplex capable 1: 100BASE-TX full duplex capable
13	100BASE-TX half-duplex	P1 RO	100BASE-TX Half Duplex Capable 0: No 100BASE-TX half duplex capable 1: 100BASE-TX half duplex capable
12	10BASE-T full-duplex	P1 RO	10BASE-T Full Duplex Capable 0: No 10BASE-TX full duplex capable 1: 10BASE-T full duplex capable
11	10BASE-T half-duplex	P1 RO	10BASE-T Half Duplex Capable 0: No 10BASE-T half duplex capable 1: 10BASE-T half duplex capable
10:7	Reserved	P0 RO	Reserved Read as 0, ignore on write
6	MF preamble suppression	PY1 RO	MII Frame Preamble Suppression 0: PHY doesn't accept management frames with preamble suppressed 1: PHY accept management frames with preamble suppressed
5	Auto-negotiation Complete	PY0 RO	Auto-negotiation Complete 0: Auto-negotiation process not completed 1: Auto-negotiation process completed
4	Remote fault	PY0 RO	Remote Fault 0: No remote fault condition detected 1: Remote fault condition detected
3	Auto-negotiation ability	P1 RO	Auto-Negotiation Ability 0: No auto-negotiation capable 1: Auto-negotiation capable
2	Link status	PY0 RO	Link Status The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface 0: Link is not established 1: Link is established
1	Jabber detect	PY0 RO	Jabber Detect This bit works only in 10Mbps mode 0: No jabber 1: Jabber condition detected
0	Extended capability	P1 RO	Extended Capability 0: Basic register capable only 1: Extended register capable

5.2.3 Port 0~4 PHY Identifier 1 Register

P0(042H), P1(062H), P2(082H), P3(0A2H), P4(0C2H)

Bit	Bit Name	Default	Description
15:0	OUI_MSB	PE 0181h RO	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

5.2.4 Port 0~4 PHY Identifier 2 Register

P0(043H), P1(063H), P2(083H), P3(0A3H), P4(0C3H)

Bit	Bit Name	Default	Description
15:10	OUI_LSB	PE 101110 RO	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9:4	VNDR_MDL	PE 001011 RO	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3:0	MDL_REV	PE 0001 RO	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM8806. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

5.2.5 Port 0~4 PHY Auto-Negotiation Advertisement Register

P0(044H), P1(064H), P2(084H), P3(0A4H), P4(0C4H)

Bit	Bit Name	Default	Description
15	NP	P0 RO	Next page Indication The DM8806 has no next page, so this bit is permanently set to 0 0: No next page 1: Next page available
14	ACK	PY0 RO	Acknowledge The DM8806's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit. 0: Not acknowledged 1: Link partner ability data reception acknowledged
13	RF	PY0 RW	Remote Fault 0: No fault detected 1: Local device senses a fault condition
12:11	Reserved	P0 RO	Reserved Write as 0, ignore on read
10	FCS	PT0 RW	Flow Control Support 0: Controller chip doesn't support flow control ability 1: Controller chip supports flow control ability
9	T4	P0 RO	100BASE-T4 Support The DM8806 does not support 100BASE-T4 so this bit is permanently set to 0 0: 100BASE-T4 is not supported 1: 100BASE-T4 is supported by the local device
8	TX_FDX	PY1 RW	100BASE-TX Full Duplex Support 0: 100BASE-TX full duplex is not supported 1: 100BASE-TX full duplex is supported by the local device
7	TX_HDX	PY1 RW	100BASE-TX Support 0: 100BASE-TX half duplex is not supported 1: 100BASE-TX half duplex is supported by the local device
6	10_FDX	PY1 RW	10BASE-T Full Duplex Support 0: 10BASE-T full duplex is not supported 1: 10BASE-T full duplex is supported by the local device
5	10_HDX	PY1 RW	10BASE-T Support 0: 10BASE-T half duplex is not supported 1: 10BASE-T half duplex is supported by the local device
4:0	Selector	PY 00001 RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

5.2.6 Port 0~4 PHY Auto-Negotiation Link Partner Ability Register

P0(045H), P1(065H), P2(085H), P3(0A5H), P4(0C5H)

Bit	Bit Name	Default	Description
15	NP	PY0 RO	Next Page Indication 0: Link partner, no next page available 1:Link partner, next page available
14	ACK	PY0 RO	Acknowledge The DM8806's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit 0: Not acknowledged 1: Link partner ability data reception acknowledged
13	RF	PY0 RO	Remote Fault 0: No remote fault indicated by link partner 1: Remote fault indicated by link partner
12:11	Reserved	PY0 RO	Reserved Read as 0, ignore on write
10	FCS	PY0 RO	Flow Control Support 0: Controller chip doesn't support flow control ability by link partner 1: Controller chip supports flow control ability by link partner
9	T4	PY0 RO	100BASE-T4 Support 0: 100BASE-T4 is not supported by the link partner 1:100BASE-T4 is supported by the link partner
8	TX_FDX	PY0 RO	100BASE-TX Full Duplex Support 0: 100BASE-TX full duplex is not supported by the link partner 1:100BASE-TX full duplex is supported by the link partner
7	TX_HDX	PY0 RO	100BASE-TX Support 0: 100BASE-TX half duplex is not supported by the link partner 1: 100BASE-TX half duplex is supported by the link partner
6	10_FDX	PY0 RO	10BASE-T Full Duplex Support 0: 10BASE-T full duplex is not supported by the link partner 1: 10BASE-T full duplex is supported by the link partner
5	10_HDX	PY0 RO	10BASE-T Support 0: 10BASE-T half duplex is not supported by the link partner 1: 10BASE-T half duplex is supported by the link partner
4:0	Selector	PY 00000 RO	Protocol Selection Bits Link partner's binary encoded protocol selector

5.2.7 Port 0~4 PHY Auto-Negotiation Expansion Register

P0(046H), P1(066H), P2(086H), P3(0A6H), P4(0C6H)

Bit	Bit Name	Default	Description
15:5	Reserved	P0 RO	Reserved Read as 0, ignore on write
4	PDF	PY0 RO	Local Device Parallel Detection Fault 0: No fault detected via parallel detection function 1: A fault detected via parallel detection function
3	LP_NP_EN	PY0 RO	Link Partner Next Page Able 0: Link partner, no next page 1: Link partner, next page available
2	NP_ABLE	P0 RO	Local Device Next Page Able DM8806 does not support this function, so this bit is always 0 0: No next page 1: Next page available
1	PAGE_RX	PY0 RO	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_EN	PY0 RO	Link Partner Auto-negotiation Able 0: Link partner do not support Auto-negotiation 1: Link partner supports Auto-negotiation

5.2.8 Port 0~4 PHY Specific Control 1 Register

P0(050H), P1(070H), P2(090H), P3(0B0H), P4(0D0H)

Bit	Bit Name	Default	Description
15	BP_4B5B	PY0 RW	Bypass 4B5B Encoding and 5B4B Decoding 0: Normal 4B5B and 5B4B operation 1: 4B5B encoder and 5B4B decoder function bypassed
14	BP_SCR	PY0 RW	Bypass Scrambler/Descrambler Function 0: Normal scrambler and descrambler operation 1: Scrambler and descrambler function bypassed
13	BP_ALIGN	PY0 RW	Bypass Symbol Alignment Function 0: Normal operation 1: Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed
12:11	Reserved	PY0 RW	Reserved
10	TX	PY1 RW	100BASE-TX Mode Control 0: 100BASE-FX operation (Fiber mode) 1: 100BASE-TX operation
9:5	Reserved	PY0 RW	Reserved
4	Reserved	PY1 RW	Reserved
3	Reserved	PY0 RW	Reserved
2	Reserved	PY1 RW	Reserved
1:0	Reserved	PY0 RW	Reserved

5.2.9 Port 0~4 PHY Specific Control 2 Register

P0(054H), P1(074H), P2(094H), P3(0B4H), P4(0D4H)

Bit	Bit Name	Default	Description
15:12	RESERVED	PY0 RW	Reserved
11	PREAMBLEX	PY0 RW	Preamble Saving Control When bit 11 of per port PHY register 1DH is set, 12-bit preamble bit is reduced; otherwise 22-bit preamble bit is reduced. 0: If bit 10 is set, the 10M TX preamble count is reduced 1: 10M TX preamble bit count is normal
10	TX10M_PWR	PY0 RW	10M TX Power Saving Control Enable 0: Disable 1: Enable
9	NWAY_PWR	PY0 RW	N-Way Power Saving Control Disalbe 0: Enable 1: Disable
8	Reserved	P0 RO	Reserved Read as 0, ignore on write
7	MDIX_CNTL	PYX RO	The polarity of MDI/MDIX value 0: MDI mode 1: MDIX mode
6	AutoNeg_dpbk	PY0 RW	Auto-negotiation Loopback 0: Normal operation 1: Test internal digital auto-negotiation Loopback
5	Mdix_fix Value	PY0 RW	MDIX_CNTL force value: When MDIX_DOWN = 1, MDIX_CNTL value depend on the register value.
4	MDIX_DOWN	PY0 RW	MDIX Down Disable HP Auto-MDIX. Force MDI/MDIX function manually. 0: Enable HP Auto-MDIX 1: Disable HP Auto-MDIX, MDIX_CNTL value depend on bit 5
3:0	Reserved	PY0 RW	Reserved

5.2.10 Port 0~4 PHY Power Saving Control Register

P0(05DH), P1(07DH), P2(09DH), P3(0BDH), P4(0DDH)

Bit	Bit Name	Default	Description
15:12	RESERVED	P0 RO	Reserved
11	PREAMBLEX	PY0 RW	Preamble Saving Control When bit 10 of per port PHY register 14H is cleared and bit 11 of per port PHY register 14H is set, the 10M TX preamble count is reduced. 0: 20-bit preamble bits is reduced 1: 10-bit preamble bit is reduced
10	RESERVED	PY0 RW	Reserved
9	TX_PWR	PY0 RW	TX Power Saving Control Disabled 0: when cable is unconnected with link partner, the driving current of transmit is reduced for power saving 1: disable TX driving power saving function
8:0	RESERVED	P0 RO	Reserved

5.3 Switch Per-Port Registers

5.3.1 Per Port Status Data Register

P0(110h), P1(130h), P2(150h), P3(170h), P4(190h), P5(1B0h)

Bit	Name	ROM	Default	Description
15:5	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
4	LP_FCS	—	P0 RO	Link Partner Flow Control Enable Status 0: Link partner don't support IEEE 802.3x flow control 1: Link partner support IEEE 802.3x flow control
3:2	SPEED	—	P0 RO	PHY Speed Status 00: 10Mbps 01: 100Mbps 1x: 1000Mbps
1	FDX	—	P0 RO	PHY Duplex Status 0: Half-duplex 1: Full-duplex
0	LINK	—	P0 RO	PHY Link Status 0: Link off 1: Link on

5.3.2 Per Port Basic Control 0 Register

P0(111h), P1(131h), P2(151h), P3(171h), P4(191h), P5(1B1h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14	UNPLUG_CLS	80h.[14] 90h.[14] A0h.[14] B0h.[14] C0h.[14] D0h.[14]	PSE0 RW	Unplug Clear Address Enable Enable to automatically clear address record in address table after unplug 0: Disable, retaining address record 1: Enable, clearing address record
13	AGE_DIS	80h.[13] 90h.[13] A0h.[13] B0h.[13] C0h.[13] D0h.[13]	PSE0 RW	Address Table Aging 0: Age function is enabled 1: Age function is disabled
12	ADRLRN_DIS	80h.[12] 90h.[12] A0h.[12] B0h.[12] C0h.[12] D0h.[12]	PSE0 RW	Address Learning Disabled 0: Address learning function is enabled 1: Address learning function is disabled
11	DIS_PAUSE	80h.[11] 90h.[11] A0h.[11] B0h.[11] C0h.[11] D0h.[11]	PSE0 RW	Maximum PAUSE Packet from Link Partner 0: Always care PAUSE packet from link partner 1: PAUSE packet by passed after 7 continued PAUSE packet from link partner

10	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
9	HOB_DIS	80h.[9] 90h.[9] A0h.[9] B0h.[9] C0h.[9] D0h.[9]	PSE0 RW	Head-of-Line Blocking Prevent Control 0: Disable 1: Enable
8	LOOPBACK	—	PSE0 RW	Loop-Back Mode The transmitted packet will be forward to this port itself 0: Look-back is disabled 1: Look-back is enabled
7	PAUSE_CON	80h.[7] 90h.[7] A0h.[7] B0h.[7] C0h.[7] D0h.[7]	PSE0 RW	Send PAUSE Continuously If buffer congestion occur on full duplex, switch will send PAUSE frames: 0: Up to 8-times 1: Continuously until alleviation
6	PARTI_EN	80h.[6] 90h.[6] A0h.[6] B0h.[6] C0h.[6] D0h.[6]	PSE0 RW	Partition Detection Enable 0: Disable 1: Enable
5	FCBP_DIS	80h.[5] 90h.[5] A0h.[5] B0h.[5] C0h.[5] D0h.[5]	PSE0 RW	Backpressure Flow-Control in Half Duplex Disable 0: Backpressure is enabled 1: Backpressure is disabled
4	FC3X_DIS	80h.[4] 90h.[4] A0h.[4] B0h.[4] C0h.[4] D0h.[4]	PSE0 RW	IEEE 802.3x Flow Control in Full Duplex Mode 0: 802.3x flow-control is enabled 1: 802.3x flow-control is disabled
3:2	MAX_PKTLEN	80h.[3:2] 90h.[3:2] A0h.[3:2] B0h.[3:2] C0h.[3:2] D0h.[3:2]	PSE0 RW	Max accept packet length by RX from this port 00: 1536-bytes 01: 1552-bytes 10: 1800-bytes 11: 2032-bytes
1	RX_DIS	—	PSE0 RW	Packet Receive Disable 0: Receive ability is enabled 1: Receive ability is disabled
0	TX_DIS	—	PSE0 RW	Packet Transmit Disable 0: Transmit ability is enabled 1: Transmit ability is disabled

5.3.3 Per Port Basic Control 1 Register

P0(112h), P1(132h), P2(152h), P3(172h), P4(192h), P5(1B2h)

Bit	Name	ROM	Default	Description
15	NO_DIS_RX	81h.[15] 91h.[15] A1h.[15] B1h.[15] C1h.[15] D1h.[15]	PSE0 RW	Don't Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control. 0: Don't discard packet 1: Discard packet
14	BANDWIDTH	81h.[14] 91h.[14] A1h.[14] B1h.[14] C1h.[14] D1h.[14]	PSE0 RW	Bandwidth Control Mode 0: Separated mode. Rate control of ingress and egress is separate. 1: Combined mode. Combining the rate of ingress and egress
13	STORM_UUP	81h.[13] 91h.[13] A1h.[13] B1h.[13] C1h.[13] D1h.[13]	PSE0 RW	Broadcast Storm Enable for Unlearned Unicast Packets 0: Disable 1: Enable
12	STORM_MP	81h.[12] 91h.[12] A1h.[12] B1h.[12] C1h.[12] D1h.[12]	PSE0 RW	Broadcast Storm Filtering for Multicast Packets Treat multicast packet as source of storm 0: Disable 1: Enable
11	MIRR_DBP	81h.[11] 91h.[11] A1h.[11] B1h.[11] C1h.[11] D1h.[11]	PSE0 RW	Don't Mirror Broadcast/Multicast Packets If Mirror Function is Enabled 0: Broadcast/Multicast would be mirrored 1: Broadcast/Multicast would not be mirrored
10	FIR_SPEC	81h.[10] 91h.[10] A1h.[10] B1h.[10] C1h.[10] D1h.[10]	PSE0,RW	Specific MAC Filtering Control Enable Enable to filter packet that is specified in the address table. 0: Disable 1: Enable
9	FIR_UUSMAC	81h.[9] 91h.[9] A1h.[9] B1h.[9] C1h.[9] D1h.[9]	PSE0 RW	Filter Packets with Unlearned Unicast SMAC 0: Disable 1: Enable
8	FIR_UUDMAC	81h.[8] 91h.[8] A1h.[8] B1h.[8] C1h.[8] D1h.[8]	PSE0 RW	Filter Packets with Unlearned Unicast DMAC 0: Disable 1: Enable

7	FIR_UMDMAC	81h.[7] 91h.[7] A1h.[7] B1h.[7] C1h.[7] D1h.[7]	PSE0 RW	Filter Packets with Unlearned Multicast DMAC 0: Disable 1: Enable
6	FIR_BDMAC	81h.[6] 91h.[6] A1h.[6] B1h.[6] C1h.[6] D1h.[6]	PSE0 RW	Filter Packets with Broadcast DMAC 0: Disable 1: Enable
5	FIR_MDMAC	81h.[5] 91h.[5] A1h.[5] B1h.[5] C1h.[5] D1h.[5]	PSE0 RW	Filter Packets with Multicast DMAC 0: Disable 1: Enable
4	FIR_MSMAC	81h.[4] 91h.[4] A1h.[4] B1h.[4] C1h.[4] D1h.[4]	PSE0 RW	Filter Packets with Multicast SMAC 0: Disable 1: Enable
3:2	MIRR_TX	81h.[3:2] 91h.[3:2] A1h.[3:2] B1h.[3:2] C1h.[3:2] D1h.[3:2]	PSE0 RW	TX Packet is Mirrored. The egress packet on this port also be forward to sniffer port. Port TX Mirror Option 00: TX mirror function is disabled 01: All transmitted packets is mirrored 10: Packet is mirrored if (DMAC search result is hit & ATB_MIRR==1 & Transmit from this port) 11: Packet is mirrored if (SMAC search result is hit & ATB_MIRR==1 & Transmit from this port)
1:0	MIRR_RX	81h.[1:0] 91h.[1:0] A1h.[1:0] B1h.[1:0] C1h.[1:0] D1h.[1:0]	PSE0 RW	RX Packet is Mirrored. The ingress packet on this port also be forward to sniffer port. Port RX Mirror Option 00: RX mirror function is disabled 01: All received packets is mirrored 10: Packet is mirrored if (DMAC search result is hit & ATB_MIRR==1 & Receive from this port) 11: Packet is mirrored if (SMAC search result is hit & ATB_MIRR==1 & Receive from this port)

5.3.4 Per Port Block Control 0 Register

P0(113h), P1(133h), P2(153h), P3(173h), P4(193h), P5(1B3h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
13:8	BLK_MP	82h.[13:8] 92h.[13:8] A2h.[13:8] B2h.[13:8] C2h.[13:8] D2h.[13:8]	PSE0 RW	Block Packet with Multicast DMAC [13]: Forward to port 5 is blocked [12]: Forward to port 4 is blocked [11]: Forward to port 3 is blocked [10]: Forward to port 2 is blocked [09]: Forward to port 1 is blocked [08]: Forward to port 0 is blocked 0: Disable 1: Enable
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	BLK_BP	82h.[5:0] 92h.[5:0] A2h.[5:0] B2h.[5:0] C2h.[5:0] D2h.[5:0]	PSE RW	Block Packet with Broadcast DMAC [05]: Forward to port 5 is blocked [04]: Forward to port 4 is blocked [03]: Forward to port 3 is blocked [02]: Forward to port 2 is blocked [01]: Forward to port 1 is blocked [00]: Forward to port 0 is blocked 0: Disable 1: Enable

5.3.5 Per Port Block Control 1 Register

P0(114h, P1(134h), P2(154h), P3(174h), P4(194h), P5(1B4h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
13:8	BLK_UKP	83h.[13:8] 93h.[13:8] A3h.[13:8] B3h.[13:8] C3h.[13:8] D3h.[13:8]	PSE0 RW	Block Packet with Unlearned Unicast DMAC [13]: Forward to port 5 is blocked [12]: Forward to port 4 is blocked [11]: Forward to port 3 is blocked [10]: Forward to port 2 is blocked [09]: Forward to port 1 is blocked [08]: Forward to port 0 is blocked 0: Disable 1: Enable
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	BLK_UP	83h.[5:0] 93h.[5:0] A3h.[5:0] B3h.[5:0] C3h.[5:0] D3h.[5:0]	PSE0 RW	Block Packet with Unicast DMAC [05]: Forward to port 5 is blocked [04]: Forward to port 4 is blocked [03]: Forward to port 3 is blocked [02]: Forward to port 2 is blocked [01]: Forward to port 1 is blocked [00]: Forward to port 0 is blocked 0: Disable 1: Enable

5.3.6 Per Port Bandwidth Control Register

P0(115h), P1(135), P2(155h), P3(175h), P4(195h), P5(1B5h)

Bit	Name	ROM	Default	Description
15:12	INGRESS	84h.[15:12] 94h.[15:12] A4h.[15:12] B4h.[15:12] C4h.[15:12] D4h.[15:12]	PSE0 RW	Ingress Rate Control (Separated mode) These bits define the bandwidth threshold that received packets over the threshold are discarded. 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps
11:8	EGRESS	84h.[11:8] 94h.[11:8] A4h.[11:8] B4h.[11:8] C4h.[11:8] D4h.[11:8]	PSE0 RW	Egress Rate Control These bits define the bandwidth threshold that transmitted packets over the threshold are discarded. 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

7:4	BSTH	84h.[7:4] 94h.[7:4] A4h.[7:4] B4h.[7:4] C4h.[7:4] D4h.[7:4]	PSE0 RW	Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control
3:0	BW_CTRL	84h.[3:0] 94h.[3:0] A4h.[3:0] B4h.[3:0] C4h.[3:0] D4h.[3:0]	PSE0 RW	Ingress and Egress Rate Control (Combined mode) Received and Transmitted Bandwidth Control These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

5.3.7 Per Port VLAN Tag Infomation Register

P0(116h), P1(136h), P2(156h), P3(176h), P4(196h), P5(1B6h)

Bit	Name	ROM	Default	Description
15:13	PPRI	85h.[15:13] 95h.[15:13] A5h.[15:13] B5h.[15:13] C5h.[15:13] D5h.[15:13]	PSE0 RW	Port VLAN Priority
12	PCFI	85h.[12] 95h.[12] A5h.[12] B5h.[12] C5h.[12] D5h.[12]	PSE0 RW	Port VLAN CFI
11:0	PVID	85h.[3:0] 95h.[3:0] A5h.[3:0] B5h.[3:0] C5h.[3:0] D5h.[3:0]	PSE1 RW	Port VLAN Identification

5.3.8 Per Port Priority and VLAN Control Register

P0(117H), P1(137H), P2(157H), P3(177H), P4(197H), P5(1B7H)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14	TAG_OUT	86h.[14] 96h.[14] A6h.[14] B6h.[14] C6h.[14] D6h.[14]	PSE0 RW	Output Tagging Enable Force output tagging regardless of VLAN table setting. 0: Disable 1: Enable
13	FIR_VPKT	86h.[13] 96h.[13] A6h.[13] B6h.[13] C6h.[13] D6h.[13]	PSE0 RW	Filter VLAN Packet To filter incoming packet if its port does not exist in VLAN member set 0: Disable 1: Enable
12	UNTAG_IN	86h.[12] 96h.[12] A6h.[12] B6h.[12] C6h.[12] D6h.[12]	PSE0 RW	Input Force No Tag Assume all received frame are untagged 0: Disable 1: Enable
11:10	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
9:8	VLAN_IAC	86h.[9:8] 96h.[9:8] A6h.[9:8] B6h.[9:8] C6h.[9:8] D6h.[9:8]	PSE0 RW	VLAN Ingress Admit Only Control 00: Accept all frames 01: Accept VLAN-tagged frames only Untagged or priority tagged(VID=0) frames will be dropped 10: Accept untagged frames only 11: Accept frame's VID equal to ingress PVID
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6	PRI_DIS	86h.[6] 96h.[6] A6h.[6] B6h.[6] C6h.[6] D6h.[6]	PSE0 RW	Priority Queue Disable 0: Priority Queue is enabled 1: Priority Queue is disabled
5	WFQUE	86h.[5] 96h.[5] A6h.[5] B6h.[5] C6h.[5] D6h.[5]	PSE0 RW	Priority Scheduling Method 0: Strict (Queue 3 > 2 > 1 > 0). Always highest priority queue first. 1: Weighted Round-Robin with 8:4:2:1 ratio
4	TOS_PRI	86h.[4] 96h.[4] A6h.[4] B6h.[4] C6h.[4] D6h.[4]	PSE0 RW	Priority Classification IP ToS over VLAN 0: Priority Classification base on VLAN 1: Priority Classification base on IP ToS field

3	TOS_OFF	86h.[3] 96h.[3] A6h.[3] B6h.[3] C6h.[3] D6h.[3]	PSE0 RW	IP ToS Priority Classification Disable 0: Classification is enabled 1: Classification is disabled
2	PRI_OFF	86h.[2] 96h.[2] A6h.[2] B6h.[2] C6h.[2] D6h.[2]	PSE0 RW	VLAN Priority Classification Disable 0: Classification is enabled 1: Classification is disabled
1:0	PB_PQ	86h.[1:0] 96h.[1:0] A6h.[1:0] B6h.[1:0] C6h.[1:0] D6h.[1:0]	PSE0 RW	Port-based Priority Queue Number 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3

5.3.9 Per Port Security Control Register

P0(118h), P1(138h), P2(158h), P3(178h), P4(198h), P5(1B8h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:10	MAX_LRN	87h.[14:10] 97h.[14:10] A7h.[14:10] B7h.[14:10] C7h.[14:10] D7h.[14:10]	PSE0 RW	Learning Restriction. Limited number of learned MAC address 1~31, 0: Limitless
9	P_UNAUTH	87h.[9] 97h.[9] A7h.[9] B7h.[9] C7h.[9] D7h.[9]	PSE0 RW	Port in Unauthorized State 0: Port is in authorized state (normal mode). TX/RX and learning capability is enabled. 1: Port is in unauthorized state (disable mode). TX/RX and learning capability is disabled. Only EAPoL packet can be forwarded.
8:2	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
1:0	PLOCK_M	87h.[1:0] 97h.[1:0] A7h.[1:0] B7h.[1:0] C7h.[1:0] D7h.[1:0]	PSE0 RW	Port Locking Mode 00: Port Lock is disabled 01: First Lock 10: First Link Lock 11: Assign Lock

5.3.10 Per Port Advanced Control Register

P0(119h), P1(139h), P2(159h), P3(179h), P4(199h), P5(1B9h)

Bit	Name	ROM	Default	Description
15:13	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
12	CT_DHLF	88h.[12] 98h.[12] A8h.[12] B8h.[12] C8h.[12] D8h.[12]	PSE0 RW	Disable Cut-Through Mode in Half-duplex 0: Enable cut-through in half-duplex 1: Disable cut-through in half-duplex
11:10	CT_MODE	88h.[11:10] 98h.[11:10] A8h.[11:10] B8h.[11:10] C8h.[11:10] D8h.[11:10]	PSE0 RW	Cut-Through Mode Cut-Through launch after how much byte of packet was received. 00: 64-bytes 01: 64-bytes 10: 128-bytes 11: 256-bytes
9	CT_EN	88h.[9] 98h.[9] A8h.[9] B8h.[9] C8h.[9] D8h.[9]	PSE0 RW	Cut-Through Mode Enable 0: Disable (Store-and-Forward) 1: Enable

8	FAST_LEAVE	88h.[9] 98h.[9] A8h.[9] B8h.[9] C8h.[9] D8h.[9]	PSE R0	IGMP Snooping Fast Leave Enable 0: Disable 1: Enable
7:6	STP_INDEX3	–	PS0 RW	STP/RSTP Port State associate with STP index 3 There are 4 port states for supporting STP, and 3 port states for supporting RSTP. 00: Forwarding State, The port transmits and receives packets normally & learning is enabled. 01: Disabled State/Discarding, The port will only forward the packets that are to and from uP port (span packets) & learning is disabled. 10: Learning State, The port will only forward the packets tha are to and from uP port (span packets) & leaning is enabled. 11: Blocking/Listening State, The port will only forward the packets that are to and from uP port (span packets) & learning is disabled.
5:4	STP_INDEX2	–	PS0 RW	STP/RSTP Port State associate with STP index 2
3:2	STP_INDEX1	–	PS0 RW	STP/RSTP Port State associate with STP index 1
1:0	STP_INDEX0	–	PS0 RW	STP/RSTP Port State associate with STP index 0

5.3.11 Per Port Memory Control Register

P0(11Ah), P1(13Ah), P2(15Ah), P3(17Ah), P4(19Ah), P5(1BAh)

Bit	Name	ROM	Default	Description
15:8	TDRQ_TH	89h.[15:8] 99h.[15:8] A9h.[15:8] B9h.[15:8] C9h.[15:8] D9h.[15:8]	PSE 19h RW	TDR output queue block threshold value, the block unit is “128bytes”. It is used generally when Head-of-Line Blocking, per port register 1 bit 19h, is set.
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:0	RV_BLKSIZ	89h.[6:0] 99h.[6:0] A9h.[6:0] B9h.[6:0] C9h.[6:0] D9h.[6:0]	PSE 3Ah RW	Per port receive buffer reserved block size, the block unit is “128bytes”. Use software to programming this field, the Maximum value is 3Eh

5.3.12 Per Port Discard Limitation Register

P0(11Bh), P1(13Bh), P2(15Bh), P3(17Bh), P4(19BH), P5(1BBh)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:8	RV_HI_TH	8Ah.[14:8] 9Ah.[14:8] AAh.[14:8] BAh.[14:8] CAh.[14:8] DAh.[14:8]	PSE 20h RW	Per port receive buffer reserved block high water threshold, the block unit is “128bytes”
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:0	RV_LO_TH	8Ah.[6:0] 9Ah.[6:0] AAh.[6:0] BAh.[6:0] CAh.[6:0] DAh.[6:0]	PSE0 RW	Per port receive buffer reserved block Low water threshold, the block unit is “128bytes”

5.3.13 Per Port Energy Efficient Ethernet Control Register

P0(11Eh), P1(13Eh), P2(15Eh), P3(17Eh), P4(19Eh)

Bit	Name	ROM	Default	Description
15	EEE_EN	8Bh.[15] 9Bh.[15] ABh.[15] BBh.[15] CBh.[15] DBh.[15]	PS0 RW	802.3az Energy Efficient Ethernet enable 0: Disable 1: Enable * The default value comes from the strap P1_LNK_LED (pin 43) and EEPROM loading sequentially.
14:8	EEE_EXIT	8Bh.[14:8] 9Bh.[14:8] ABh.[14:8] BBh.[14:8] CBh.[14:8] DBh.[14:8]	PS0 RW	Timer to leave EEE state before transmit packet Unit: 2us (default: 30us)
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:0	EEE_IN	8Bh.[6:0] 9Bh.[6:0] ABh.[6:0] BBh.[6:0] CBh.[6:0] DBh[6:0]	PS0 RW	Timer to enter EEE state after transmit idle Unit: 2us (default: 10us)

5.4 Switch Engine Registers

5.4.1 Switch Status Register (210h)

Bit	Name	ROM	Default	Description
15:4	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
3	RV_NonEmpty	–	RO	Receive Buffer Status (Debug Only) 0: No packet in buffer 1: There are packets in buffer
2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1	BIST_1	–	RO	Memory 1 BIST Status (25K) 0:Pass 1:Fail
0	BIST_0	–	RO	Memory 0 BIST Status (48K) 0:Pass 1:Fail

5.4.2 Switch Reset Register (211h)

Bit	Name	ROM	Default	Description
15:3	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
2	PD_ANLG	–	P0 RW	Power down all analog PHY 0: Power On 1: Power Down
1	RST_ANLG	–	P0 RW	Analog PHY Core Reset Write 1 to reset, and auto-clear after 10us
0	RST_SW	–	P0 RW	Switch Core Reset Write 1 to reset, and auto-clear after 10us

5.4.3 Switch Control Register Register (212h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14	MAC_1X	12h.[14]	PS0, RW	MAC-based 802.1x Security 0: Port-based 1: MAC-based
13:12	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
11:8	TRUNK_EN	12h.[11:8]	PSE0 RW	Trunk Enable {P3,P2,P1,P0} [11] 1: Port 3 trunk is enabled 0: Port 3 trunk is disabled [10] 1: Port 2 trunk is enabled 0: Port 2 trunk is disabled [09] 1: Port 1 trunk is enabled 0: Port 1 trunk is disabled [08] 1: Port 0 trunk is enabled 0: Port 0 trunk is disabled
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5	FDX_FLOW	12h.[5]	PSE0 RW	Flow Control Option In full duplex operation, the flow control ability is decided according to the result of Auto-Negotiation if this bit is asseted. Otherwise, flow control ability is controlled by bit 4 of register 111H (131H,151H,171H,191H,1B1H). 0: Forced PAUSE 1: Symmetric PAUSE
4	NO_REG	12h.[4]	PE0 RW	Don't Initialize Registers When Software Reset Command is Launched 0: Initialize registers 1: Don't initialize registers
3	AUTO_RST	12h.[3]	PE0 RW	Disable RV Buffer Count Checking (internal use) 0: auto switch reset if per port's RV buffer error RV buffer count > 31 and not changed for 40ms. 1: disable checking
2	DIS_CRCC	12h.[2]	PSE0 RW	CRC Checking Disable 0: CRC checking is enabled 1: CRC checking is disabled
1:0	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read

5.4.4 CPU Port & Mirror Control Register (213h)

Bit	Name	ROM	Default	Description
15:11	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
10	MIRR_PAIR	13h.[10]	PSE0 RW	Mirror RX/TX Pair Mode Enable 0: Disable 1: Enable
9:8	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
7	STAG_TXE	13h.[7]	PSE0 RW	Special Tag Transmit Enable for CPU Port 0: Don't insert the Special Tag for outgoing packets 1: Insert the Special Tag for outgoing packets
6	STAG_RXE	13h.[6]	PSE0 RW	Special Tag Receive Enable for CPU Port 0: Don't identify the Special Tag for incoming packets 1: Identifies the Special Tag for incoming packets
5:3	SNF_PORT	13h.[5:3]	PSE0 RW	Sniffer Port Number 000: Sniffer Port is Port 0 001: Sniffer Port is Port 1 010: Sniffer Port is Port 2 011: Sniffer Port is Port 3 100: Sniffer Port is Port 4 101: Sniffer Port is Port 5 110: Reserved 111: Reserved
2:0	CPU_PORT	13h.[2:0]	PE5 RW	Select CPU Port Number 000: Port 0 001: Port 1 010: Port 2 011: Port 3 100: Port 4 101: Port 5 110: Port 5 111: Port 5

5.4.5 Special Tag Ether-Type Register (214h)

Bit	Name	ROM	Default	Description
15:0	STAG_ETH	14h.[15:0]	PSE RW 8606h	Special Tag Ether-Type

5.4.6 Global Learning & Aging Control Register (215h)

Bit	Name	ROM	Default	Description
15:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5	LRN_PAUSE	15h.[3]	PSE0 RW	Learn PAUSE Frame 0: Disable 1: Enable
4	LRN_VLAN	15h.[2]	PSE0 RW	Address Learning Consider VLAN Member 0: Address learning despite VLAN member 1: Address learning is disabled if incoming port doesn't exist in its member set.
3	ATB_KEY	15h.[1]	PSE0 RW	Address Table Hash Key 0: Use (DMAC) for searching and (SMAC) for learning 1: Use (DMAC+FID) for searching and (SMAC+FID) for learning Note: Must clear address table after this bit is changed.
2	ATB_MODE	15h.[0]	PSE0 RW	Address Table Mode 0: Mixed mode, 2K address table for unicast or multicast 1: Separated mode, 1K for unicast and 1K for multicast Note: Must clear address table after this bit is changed.
1:0	AGE_TIME	15h.[1:0]	PSE0 RW	Aging Time Value 00: 512 sec ±256 sec 01: 256 sec ±128 sec 10: 128 sec ± 64 sec 11: 64 sec ± 32 sec

5.4.7 VLAN Priority Map Register (217H)

Bit	Name	ROM	Default	Description
15:14	VLAN_PM7	1Ch.[15:14]	PSE3 RW	If packet's VLAN tag priority value is equal to 07H, the output priority queue is decided according to this field. 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3
13:12	VLAN_PM6	1Ch.[13:12]	PSE3 RW	VLAN tag priority value is equal to 06H.
11:10	VLAN_PM5	1Ch.[11:10]	PSE2 RW	VLAN tag priority value is equal to 05H.
9:8	VLAN_PM4	1Ch.[09:08]	PSE2 RW	VLAN tag priority value is equal to 04H
7:6	VLAN_PM3	1Ch.[07:06]	PSE1 RW	VLAN tag priority value is equal to 03H.
5:4	VLAN_PM2	1Ch [05:04]	PSE1 RW	VLAN tag priority value is equal to 02H
3:2	VLAN_PM1	1Ch.[03:02]	PSE0 RW	VLAN tag priority value is equal to 01H.
1:0	VLAN_PM0	1Ch.[01:00]	PSE0 RW	VLAN tag priority value is equal to 00H

5.4.8 TOS Priority Map 0 Register (218h)

Bit	Name	ROM	Default	Description
15:14	TOS_PM07	1Dh.[15:14]	PSE0 RW	If packet's IP ToS value is equal to 07H, the output priority queue is decided according to this field. 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3
13:12	TOS_PM06	1Dh.[13:12]	PSE0 RW	ToS value is equal to 06H
11:10	TOS_PM05	1Dh.[11:10]	PSE0 RW	ToS value is equal to 05H
9:8	TOS_PM04	1Dh.[09:08]	PSE0 RW	ToS value is equal to 04H
7:6	TOS_PM03	1Dh.[07:06]	PSE0 RW	ToS value is equal to 03H
5:4	TOS_PM02	1Dh.[05:04]	PSE0 RW	ToS value is equal to 02H
3:2	TOS_PM01	1Dh.[03:02]	PSE0 RW	ToS value is equal to 01H
1:0	TOS_PM00	1Dh.[01:00]	PSE0 RW	ToS value is equal to 00H

5.4.9 TOS Priority Map 1 Register (219h)

Bit	Name	ROM	Default	Description
15:14	TOS_PM0F	1Eh.[15:14]	PSE0 RW	ToS value is equal to 0FH
13:12	TOS_PM0E	1Eh.[13:12]	PSE0 RW	ToS value is equal to 0EH
11:10	TOS_PM0D	1Eh.[11:10]	PSE0 RW	ToS value is equal to 0DH
9:8	TOS_PM0C	1Eh.[09:08]	PSE0 RW	ToS value is equal to 0CH
7:6	TOS_PM0B	1Eh.[07:06]	PSE0 RW	ToS value is equal to 0BH
5:4	TOS_PM0A	1Eh.[05:04]	PSE0 RW	ToS value is equal to 0AH
3:2	TOS_PM09	1Eh.[03:02]	PSE0 RW	ToS value is equal to 09H
1:0	TOS_PM08	1Eh.[01:00]	PSE0 RW	ToS value is equal to 08H

5.4.10 TOS Priority Map 2 Register (21Ah)

Bit	Name	ROM	Default	Description
15:14	TOS_PM17	1Fh.[15:14]	PSE1 RW	ToS value is equal to 17H
13:12	TOS_PM16	1Fh.[13:12]	PSE1 RW	ToS value is equal to 16H
11:10	TOS_PM15	1Fh.[11:10]	PSE1 RW	ToS value is equal to 15H
9:8	TOS_PM14	1Fh.[09:08]	PSE1 RW	ToS value is equal to 14H
7:6	TOS_PM13	1Fh.[07:06]	PSE1 RW	ToS value is equal to 13H
5:4	TOS_PM12	1Fh.[05:04]	PSE1 RW	ToS value is equal to 12H
3:2	TOS_PM11	1Fh.[03:02]	PSE1 RW	ToS value is equal to 11H
1:0	TOS_PM10	1Fh.[01:00]	PSE1 RW	ToS value is equal to 10H

5.4.11 TOS Priority Map 3 Register (21Bh)

Bit	Name	ROM	Default	Description
15:14	TOS_PM1F	20h.[15:14]	PSE1 RW	ToS value is equal to 1FH
13:12	TOS_PM1E	20h [13:12]	PSE1 RW	ToS value is equal to 1EH
11:10	TOS_PM1D	20h.[11:10]	PSE1 RW	ToS value is equal to 1DH
9:8	TOS_PM1C	20h.[09:08]	PSE1 RW	ToS value is equal to 1CH
7:6	TOS_PM1B	20h.[07:06]	PSE1 RW	ToS value is equal to 1BH
5:4	TOS_PM1A	20h.[05:04]	PSE1 RW	ToS value is equal to 1AH
3:2	TOS_PM19	20h.[03:02]	PSE1 RW	ToS value is equal to 19H
1:0	TOS_PM18	20h.[01:00]	PSE1 RW	ToS value is equal to 18H

5.4.12 TOS Priority Map 4 Register (21Ch)

Bit	Name	ROM	Default	Description
15:14	TOS_PM27	21h.[15:14]	PSE2 RW	ToS value is equal to 27H
13:12	TOS_PM26	21h.[13:12]	PSE2 RW	ToS value is equal to 26H
11:10	TOS_PM25	21h.[11:10]	PSE2 RW	ToS value is equal to 25H
9:8	TOS_PM24	21h.[09:08]	PSE2 RW	ToS value is equal to 24H
7:6	TOS_PM23	21h.[07:06]	PSE2 RW	ToS value is equal to 23H
5:4	TOS_PM22	21h.[05:04]	PSE2 RW	ToS value is equal to 22H
3:2	TOS_PM21	21h.[03:02]	PSE2 RW	ToS value is equal to 21H
1:0	TOS_PM20	21h.[01:00]	PSE2 RW	ToS value is equal to 20H

5.4.13 TOS Priority Map 5 Register (21Dh)

Bit	Name	ROM	Default	Description
15:14	TOS_PM2F	22h.[15:14]	PSE2 RW	ToS value is equal to 2FH
13:12	TOS_PM2E	22h.[13:12]	PSE2 RW	ToS value is equal to 2EH
11:10	TOS_PM2D	22h.[11:10]	PSE2 RW	ToS value is equal to 2DH
9:8	TOS_PM2C	22h.[09:08]	PSE2 RW	ToS value is equal to 2CH
7:6	TOS_PM2B	22h.[07:06]	PSE2 RW	ToS value is equal to 2BH
5:4	TOS_PM2A	22h [05:04]	PSE2 RW	ToS value is equal to 2AH
3:2	TOS_PM29	22h.[03:02]	PSE2 RW	ToS value is equal to 29H
1:0	TOS_PM28	22h.[01:00]	PSE2 RW	ToS value is equal to 28H

5.4.14 TOS Priority Map 6 Register (21Eh)

Bit	Name	ROM	Default	Description
15:14	TOS_PM37	23h.[15:14]	PSE3 RW	ToS value is equal to 37H
13:12	TOS_PM36	23h.[13:12]	PSE3 RW	ToS value is equal to 36H
11:10	TOS_PM35	23h.[11:10]	PSE3 RW	ToS value is equal to 35H
9:8	TOS_PM34	23h.[09:08]	PSE3 RW	ToS value is equal to 34H
7:6	TOS_PM33	23h.[07:06]	PSE3 RW	ToS value is equal to 33H
5:4	TOS_PM32	23h.[05:04]	PSE3 RW	ToS value is equal to 32H
3:2	TOS_PM31	23h.[03:02]	PSE3 RW	ToS value is equal to 31H
1:0	TOS_PM30	23h.[01:00]	PSE3 RW	ToS value is equal to 30H

5.4.15 TOS Priority Map 7 Register (21Fh)

Bit	Name	ROM	Default	Description
15:14	TOS_PM3F	24h.[15:14]	PSE3 RW	ToS value is equal to 3FH
13:12	TOS_PM3E	24h.[13:12]	PSE3 RW	ToS value is equal to 3EH
11:10	TOS_PM3D	24h.[11:10]	PSE3 RW	ToS value is equal to 3DH
9:8	TOS_PM3C	24h.[09:08]	PSE3 RW	ToS value is equal to 3CH
7:6	TOS_PM3B	24h.[07:06]	PSE3 RW	ToS value is equal to 3BH
5:4	TOS_PM3A	24h.[05:04]	PSE3 RW	ToS value is equal to 3AH
3:2	TOS_PM39	24h.[03:02]	PSE3 RW	ToS value is equal to 39H
1:0	TOS_PM38	24h.[01:00]	PSE3 RW	ToS value is equal to 38H

5.4.16 MIB Counter Disable Register (230h)

Bit	Name	ROM	Default	Description
15:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	MIB_DIS	16h.[5:0]	PSE0 RW	Per-Port MIB Counter Disable [5] 0: Port 5 MIB counter is enabled 1: Port 5 MIB counter is disabled [4] 0: Port 4 MIB counter is enabled 1: Port 4 MIB counter is disabled [3] 0: Port 3 MIB counter is enabled 1: Port 3 MIB counter is disabled [2] 0: Port 2 MIB counter is enabled 1: Port 2 MIB counter is disabled [1] 0: Port 1 MIB counter is enabled 1: Port 1 MIB counter is disabled [0] 0: Port 0 MIB counter is enabled 1: Port 0 MIB counter is disabled

5.4.17 MIB Counter Control Register (231h)

Bit	Name	ROM	Default	Description
15	MIB_READY	—	PS0 RO	Counter Data is Ready 0: Not ready 1: Ready
14:10	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
9:8	MIB_CMD	—	PS0 RW	MIB Command 00: Read & Clear 01: Read only 10: Clear MIB counters of port 11: Clear MIB counters of all ports
7:5	MIB_PORT	—	PS0 RW	Port Index (0~5)
4:0	MIB_OFSET	—	PS0 RW	Counter Offset (0~9)

5.4.18 MIB Counter Data Low Register (232h)

Bit	Name	ROM	Default	Description
15:0	MIB_DL	—	PS0 RW	Counter Data Low Byte (Bit 15:00)

5.4.19 MIB Counter Data High Register (233h)

Bit	Name	ROM	Default	Description
15:0	MIB_DH	—	PS0 RW	Counter Data High Byte (Bit 31:16)

5.4.20 Special Packet Control 0 Register (234h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP01_ACT	26h.[14:13]	PSE0 RW	Forwarding Action for PAUSE 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP01_TAG	26h.[12:11]	PSE0 RW	TX Tag Handle for PAUSE 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP01_OVERRIDE	26h.[10]	PSE0 RW	Override bit for PAUSE 0: Not a overriding packet 1: A Overriding packet
9	SP01_CVLAN	26h.[09]	PSE0 RW	Cross VLAN bit for PAUSE 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP01_EN	26h.[08]	PSE0 RW	Identify Enable for PAUSE DMAC=0180C2-000001 0: Disable 1: Enable
7	RESERVED	–	RO	Reserved Write as 0h, ignore when read
6:5	SP00_ACT	26h.[06:05]	PSE0 RW	Forwarding Action for BPDU 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP00_TAG	26h.[04:03]	PSE0 RW	TX Tag Handle for BPDU 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP00_OVERRIDE	26h.[02]	PSE0 RW	Override bit for BPDU 0: Not a overriding packet 1: A Overriding packet
1	SP00_CVLAN	26h.[01]	PSE0 RW	Cross VLAN bit for BPDU 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP00_EN	26h.[00]	PSE0 RW	Identify Enable for BPDU DMAC=0180C2-000000 0: Disable 1: Enable

5.4.21 Special Packet Control 1 Register (235h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP03_ACT	27h.[14:13]	PSE0 RW	Forwarding Action for EAP(802.1x) 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP03_TAG	27h.[12:11]	PSE0 RW	TX Tag Handle for EAP(802.1x) 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP03_OVERRIDE	27h.[10]	PSE0 RW	Override bit for EAP(802.1x) 0: Not a overriding packet 1: A Overriding packet
9	SP03_CVLAN	27h.[09]	PSE0 RW	Cross VLAN bit for EAP(802.1x) 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP03_EN	27h.[08]	PSE0 RW	Identify Enable for EAP(802.1x) DMAC=0180C2-000003 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP02_ACT	27h.[06:05]	PSE0 RW	Forwarding Action for SlowProtocol 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP02_TAG	27h.[04:03]	PSE0 RW	TX Tag Handle for SlowProtocol 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP02_OVERRIDE	27h.[02]	PSE0 RW	Override bit for SlowProtocol 0: Not a overriding packet 1: A Overriding packet
1	SP02_CVLAN	27h.[01]	PSE0 RW	Cross VLAN bit for SlowProtocol 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP02_EN	27h.[00]	PSE0 RW	Identify Enable for SlowProtocol DMAC=0180C2-000002 0: Disable 1: Enable

5.4.22 Special Packet Control 2 Register (236h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP05_ACT	28h.[14:13]	PSE0 RW	Forwarding Action for LLDP 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP05_TAG	28h.[12:11]	PSE0 RW	TX Tag Handle for LLDP 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP05_OVERRIDE	28h.[10]	PSE0 RW	Override bit for LLDP 0: Not a overriding packet 1: A Overriding packet
9	SP05_CVLAN	28h.[09]	PSE0 RW	Cross VLAN bit for LLDP 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP05_EN	28h.[08]	PSE0 RW	Identify Enable for LLDP DMAC=0180C2-0000E 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP04_ACT	28h.[06:05]	PSE0 RW	Forwarding Action for RESERV_B0 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP04_TAG	28h.[04:03]	PSE0 RW	TX Tag Handle for RESERV_B0 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP04_OVERRIDE	28h.[02]	PSE0 RW	Override bit for RESERV_B0 0: Not a overriding packet 1: A Overriding packet
1	SP04_CVLAN	28h.[01]	PSE0 RW	Cross VLAN bit for RESERV_B0 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP04_EN	28h.[00]	PSE0 RW	Identify Enable for RESERV_B0 DMAC=0180C2-000004 ~ 0180C2-00000D & 0180C2-00000F 0: Disable 1: Enable

5.4.23 Special Packet Control 3 Register (237h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP07_ACT	29h.[14:13]	PSE0 RW	Forwarding Action for RESERV_B1 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP07_TAG	29h.[12:11]	PSE0 RW	TX Tag Handle for RESERV_B1 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP07_OVERRIDE	29h.[10]	PSE0 RW	Override bit for RESERV_B1 0: Not a overriding packet 1: A Overriding packet
9	SP07_CVLAN	29h.[09]	PSE0 RW	Cross VLAN bit for RESERV_B1 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP07_EN	29h.[08]	PSE0 RW	Identify Enable for RESERV_B1 DMAC=0180C2-000011 ~ 0180C2-00001F 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP06_ACT	29h.[06:05]	PSE0 RW	Forwarding Action for ABM 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP06_TAG	29h.[04:03]	PSE0 RW	TX Tag Handle for ABM 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP06_OVERRIDE	29h.[02]	PSE0 RW	Override bit for ABM 0: Not a overriding packet 1: A Overriding packet
1	SP06_CVLAN	29h.[01]	PSE0 RW	Cross VLAN bit for ABM 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP06_EN	29h.[00]	PSE0 RW	Identify Enable for ABM (All LAN Bridge Management Group Address) DMAC=0180C2-000010 0: Disable 1: Enable

5.4.24 Special Packet Control 4 Register (238h)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP09_ACT	2Ah.[14:13]	PSE0 RW	Forwarding Action for RESERV_B2 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP09_TAG	2Ah.[12:11]	PSE0 RW	TX Tag Handle for RESERV_B2 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP09_OVERRIDE	2Ah.[10]	PSE0 RW	Override bit for RESERV_B2 0: Not a overriding packet 1: A Overriding packet
9	SP09_CVLAN	2Ah.[09]	PSE0 RW	Cross VLAN bit for RESERV_B2 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP09_EN	2Ah.[08]	PSE0 RW	Identify Enable for RESERV_B2 DMAC=0180C2-000022 ~ 0180C2-00002F 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP08_ACT	2Ah.[06:05]	PSE0 RW	Forwarding Action for GXRP 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP08_TAG	2Ah.[04:03]	PSE0 RW	TX Tag Handle for GXRP 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP08_OVERRIDE	2Ah.[02]	PSE0 RW	Override bit for GXRP 0: Not a overriding packet 1: A Overriding packet
1	SP08_CVLAN	2Ah.[01]	PSE0 RW	Cross VLAN bit for GXRP 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP08_EN	2Ah.[00]	PSE0 RW	Identify Enable for GXRP(GARP/GVRP) DMAC=0180C2-000020, 0180C2-000021 0: Disable 1: Enable

5.4.25 Special Packet Control 5 Register (239h)

Bit	Name	ROM	Default	Description
15:7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP0A_ACT	2Bh.[06:05]	PSE0 RW	Forwarding Action for RESERV_B3 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP0A_TAG	2Bh.[04:03]	PSE0 RW	TX Tag Handle for RESERV_B3 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP0A_OVERRIDE	2Bh.[02]	PSE0 RW	Override bit for RESERV_B3 0: Not a overriding packet 1: A Overriding packet
1	SP0A_CVLAN	2Bh.[01]	PSE0 RW	Cross VLAN bit for RESERV_B3 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP0A_EN	2Bh.[00]	PSE0 RW	Identify Enable for RESERV_B3 DMAC=0180C2-000030 ~ 0180C2-0000FF 0: Disable 1: Enable

5.4.26 Special Packet Control 6 Register (23Ah)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP0D_ACT	2Ch.[14:13]	PSE0 RW	Forwarding Action for ARP 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP0D_TAG	2Ch.[12:11]	PSE0 RW	TX Tag Handle for ARP 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP0D_OVERRIDE	2Ch.[10]	PSE0 RW	Override bit for ARP 0: Not a overriding packet 1: A Overriding packet
9	SP0D_CVLAN	2Ch.[09]	PSE0 RW	Cross VLAN bit for ARP 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP0D_EN	2Ch.[08]	PSE0 RW	Identify Enable for ARP DMAC=FFFFFF-FFFFFF, EthType=8036 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP0C_ACT	2Ch.[06:05]	PSE0 RW	Forwarding Action for RARP 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP0C_TAG	2Ch.[04:03]	PSE0 RW	TX Tag Handle for RARP 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP0C_OVERRIDE	2Ch.[02]	PSE0 RW	Override bit for RARP 0: Not a overriding packet 1: A Overriding packet
1	SP0C_CVLAN	2Ch.[01]	PSE0 RW	Cross VLAN bit for RARP 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP0C_EN	2Ch.[00]	PSE0 RW	Identify Enable for RARP DMAC=FFFFFF-FFFFFF, EthType=0x8035 0: Disable 1: Enable

5.4.27 Special Packet Control 7 Register (23Bh)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP0F_ACT	2Dh.[14:13]	PSE0 RW	Forwarding Action for IPV6_MLD 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP0F_TAG	2Dh.[12:11]	PSE0 RW	TX Tag Handle for IPV6_MLD 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP0F_OVERRIDE	2Dh.[10]	PSE0 RW	Override bit for IPV6_MLD 0: Not a overriding packet 1: A Overriding packet
9	SP0F_CVLAN	2Dh.[09]	PSE0 RW	Cross VLAN bit for IPV6_MLD 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP0F_EN	2Dh.[08]	PSE0 RW	Identify Enable for IPV6_MLD DMAC==3333XX-XXXXXX, EthType=0x86DD, IP.Version=6, Next field? 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP0E_ACT	2Dh.[06:05]	PSE0 RW	Forwarding Action for IP_IGMP 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP0E_TAG	2Dh.[04:03]	PSE0 RW	TX Tag Handle for IP_IGMP 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP0E_OVERRIDE	2Dh.[02]	PSE0 RW	Override bit for IP_IGMP 0: Not a overriding packet 1: A Overriding packet
1	SP0E_CVLAN	2Dh.[01]	PSE0 RW	Cross VLAN bit for IP_IGMP 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP0E_EN	2Dh.[00]	PSE0 RW	Identify Enable for IP_IGMP DMAC=01005E-XXXXXX, EthType=0x0800, IP.Version=4, IP.Protocol=02 0: Disable 1: Enable

5.4.28 Special Packet Control 8 Register (23Ch)

Bit	Name	ROM	Default	Description
15	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
14:13	SP11_ACT	2Eh.[14:13]	PSE0 RW	Forwarding Action for PPPoE 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
12:11	SP11_TAG	2Eh.[12:11]	PSE0 RW	TX Tag Handle for PPPoE 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
10	SP11_OVERRIDE	2Eh.[10]	PSE0 RW	Override bit for PPPoE 0: Not a overriding packet 1: A Overriding packet
9	SP11_CVLAN	2Eh.[09]	PSE0 RW	Cross VLAN bit for PPPoE 0: Obey VLAN constraint 1: Can cross VLAN constraint
8	SP11_EN	2Eh.[08]	PSE0 RW	Identify Enable for PPPoE EthType=0x8863/0x8864 0: Disable 1: Enable
7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6:5	SP10_ACT	2Eh.[06:05]	PSE0 RW	Forwarding Action for IP_ICMP 00: Unmodified 01: Drop 10: Trap to CPU 11: Flood excluding CPU
4:3	SP10_TAG	2Eh.[04:03]	PSE0 RW	TX Tag Handle for IP_ICMP 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2	SP10_OVERRIDE	2Eh.[02]	PSE0 RW	Override bit for IP_ICMP 0: Not a overriding packet 1: A Overriding packet
1	SP10_CVLAN	2Eh.[01]	PSE0 RW	Cross VLAN bit for IP_ICMP 0: Obey VLAN constraint 1: Can cross VLAN constraint
0	SP10_EN	2Eh.[00]	PSE0 RW	Identify Enable for IP_ICMP EthType=0x0800, IP.Version=4, IP.Protocol=01 0: Disable 1: Enable

5.4.29 QinQ TPID Register (23Dh)

Bit	Name	ROM	Default	Description
15:0	QinQ_TPID	30h.[15:0]	PSE 88A8h RW	QinQ Tag Protocol Identifier For VLAN stacking function

5.4.30 VLAN Mode and Rule Control Register (23Eh)

Bit	Name	ROM	Default	Description
15	FIR_VIDFFF	31h.[15]	PSE0 RW	Enable to drop Pakcet with VID==0xFFF 0: Disable 1: Enable
14	FIR_CFI	31h.[14]	PSE0 RW	Enable to drop Pakcet with Nonzero CFI Drop incoming packet, if the CFI field is not equal to zero. 0: Disable 1: Enable
13:12	VLAN_UVID	31h.[13:12]	PSE0 RW	Unknown VID Handle 00: Drop 01: Trap to CPU 10: Trap to Sniffer Port 11: Reserved
11:9	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
8	QINQ_EN	31h.[8]	PSE0 RW	VLAN Stacking Enable (QinQ) 0: Disable 1: Enable
7	TOS6	31h.[7]	PE0 RW	Full IP ToS Field for Priority Queue 0: Check most significant 3-bit only of TOS 1: Check most significant 6-bit of TOS
6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5	UCLEAKY_EN	31h.[5]	PE0 RW	Unicast packet can across VLAN boundary. The function allows switch without external router when inter-VLAN communicate in switch. 0: Disable 1: Enable
4	VLAN_RVIDFFF	31h.[4]	PSE0 RW	Replace VIDFFF with PVID Enable Replace VID field of VLAN tag with PVID, if VID==0xFFF 0: Disable 1: Enable
3	VLAN_RVID1	31h.[3]	PSE0 RW	Replace VID1 with PVID Enable Replace VID field of VLAN tag with PVID, if VID==0x001 0: Disable 1: Enable
2	VLAN_RVIDO	31h.[2]	PSE0 RW	Replace VID0 with PVID Enable Replace VID field of VLAN tag with PVID, if VID==0x000 0: Disable 1: Enable
1	VLAN_RPRI	31h.[1]	PSE0 RW	Replace Priority Enable Replace priority field of VLAN tag with PPRI 0: Disable 1: Enable

0	VLAN_MODE	31h.[0]	PSE0 RW	VLAN_MODE 0: Port-based VLAN 1: Tag-based VLAN

5.4.31 VLAN Table - Valid Control Register (23Fh)

Bit	Name	ROM	Default	Description
15:0	VTAB_VALD	32h.[15:0]	PSE 01H RW	Entry Vailid Bits in VLAN Table There are 16 entries in the VLAN table. This field indicates which entries are valid. 0: Invalid 1: Valid

5.4.32 VLAN Table - ID_0H Register (250h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID0	33h.[15:12]	PSE0 RW	FID of VLAN Entry 0
11:00	VTAB_VID0	33h.[11:00]	PSE1 RW	VID of VLAN Entry 0

5.4.33 VLAN Table - ID_1H Register (251h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID1	34h.[15:12]	PSE0 RW	FID of VLAN Entry 1
11:00	VTAB_VID1	34h.[11:00]	PSE0 RW	VID of VLAN Entry 1

5.4.34 VLAN Table - ID_2H Register (252h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID2	35h.[15:12]	PSE0 RW	FID of VLAN Entry 2
11:00	VTAB_VID2	35h.[11:00]	PSE0 RW	VID of VLAN Entry 2

5.4.35 VLAN Table - ID_3H Register (253h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID3	36h.[15:12]	PSE0 RW	FID of VLAN Entry 3
11:00	VTAB_VID3	36h.[11:00]	PSE0 RW	VID of VLAN Entry 3

5.4.36 VLAN Table - ID_4H Register (254h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID4	37h.[15:12]	PSE0 RW	FID of VLAN Entry 4
11:00	VTAB_VID4	37h.[11:00]	PSE0 RW	VID of VLAN Entry 4

5.4.37 VLAN Table - ID_5H Register (255h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID5	38h.[15:12]	PSE0 RW	FID of VLAN Entry 5
11:00	VTAB_VID5	38h.[11:00]	PSE0 RW	VID of VLAN Entry 5

5.4.38 VLAN Table - ID_6H Register (256h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID6	39h.[15:12]	PSE0 RW	FID of VLAN Entry 6
11:00	VTAB_VID6	39h.[11:00]	PSE0 RW	VID of VLAN Entry 6

5.4.39 VLAN Table - ID_7H Register (257h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID7	3Ah.[15:12]	PSE0 RW	FID of VLAN Entry 7
11:00	VTAB_VID7	3Ah.[11:00]	PSE0 RW	VID of VLAN Entry 7

5.4.40 VLAN Table - ID_8H Register (258h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID8	3Bh.[15:12]	PSE0 RW	FID of VLAN Entry 8
11:00	VTAB_VID8	3Bh.[11:00]	PSE0 RW	VID of VLAN Entry 8

5.4.41 VLAN Table - ID_9H Register (259h)

Bit	Name	ROM	Default	Description
15:12	VTAB_FID9	3Ch.[15:12]	PSE0 RW	FID of VLAN Entry 9
11:00	VTAB_VID9	3Ch.[11:00]	PSE0 RW	VID of VLAN Entry 9

5.4.42 VLAN Table - ID_AH Register (25Ah)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDA	3Dh.[15:12]	PSE0 RW	FID of VLAN Entry 10
11:00	VTAB_VIDA	3Dh.[11:00]	PSE0 RW	VID of VLAN Entry 10

5.4.43 VLAN Table - ID_BH Register (25Bh)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDB	3Eh.[15:12]	PSE0 RW	FID of VLAN Entry 11
11:00	VTAB_VIDB	3Eh.[11:00]	PSE0 RW	VID of VLAN Entry 11

5.4.44 VLAN Table - ID_CH Register (25Ch)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDC	3Fh.[15:12]	PSE0 RW	FID of VLAN Entry 12
11:00	VTAB_VIDC	3Fh.[11:00]	PSE0 RW	VID of VLAN Entry 12

5.4.45 VLAN Table - ID_DH Register (25Dh)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDD	40h.[15:12]	PSE0 RW	FID of VLAN Entry 13
11:00	VTAB_VIDD	40h.[11:00]	PSE0 RW	VID of VLAN Entry 13

5.4.46 VLAN Table - ID_EH Register (25Eh)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDF	41h.[15:12]	PSE0 RW	FID of VLAN Entry 14
11:00	VTAB_VIDF	41h.[11:00]	PSE0 RW	VID of VLAN Entry 14

5.4.47 VLAN Table - ID_FH Register (25Fh)

Bit	Name	ROM	Default	Description
15:12	VTAB_FIDF	42h.[15:12]	PSE0 RW	FID of VLAN Entry 15
11:00	VTAB_VIDF	42h.[11:00]	PSE0 RW	VID of VLAN Entry 15

5.4.48 VLAN Table - MEMBER_0H Register (270h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM0	43h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 0 Port map indicates which ports are forced output tagging. [13]: Port 5 | [12]: Port 4 | [11]: Port 3 [10]: Port 2 | [09]: Port 1 | [08]: Port 0 0: Disable 1: Enable
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM0	43h.[5:0]	PSE 3Fh RW	VLAN Member of VLAN Entry 0 Port map indicates which ports belong to this VLAN entry. [05]: Port 5 | [04]: Port 4 | [03]: Port 3 [02]: Port 2 | [01]: Port 1 | [00]: Port 0 0: Disable 1: Enable

5.4.49 VLAN Table - MEMBER_1H Register (271h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM1	44h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 1
7:6	RESERVED	–	RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM1	44h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 1

5.4.50 VLAN Table - MEMBER_2H Register (272h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM2	45h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 2
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM2	45h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 2

5.4.51 VLAN Table - MEMBER_3H Register (273h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM3	46h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 3
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM3	46h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 3

5.4.52 VLAN Table - MEMBER_4H Register (274h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM4	47h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 4
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM4	47h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 4

5.4.53 VLAN Table - MEMBER_5H Register (275h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM5	48h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 5
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM5	48h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 5

5.4.54 VLAN Table - MEMBER_6H Register (276h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM6	49h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 6
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM6	49h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 6

5.4.55 VLAN Table - MEMBER_7H Register (277h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM7	4Ah.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 7
7:6	RESERVED	–	RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM7	4Ah.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 7

5.4.56 VLAN Table - MEMBER_8H Register (278h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM8	4Bh.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 8
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM8	4Bh.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 8

5.4.57 VLAN Table - MEMBER_9H Register (279h)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TM9	4Ch.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 9
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VM9	4Ch.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 9

5.4.58 VLAN Table - MEMBER_AH Register (27Ah)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TMA	4Dh.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 10
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VMA	4Dh.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 10

5.4.59 VLAN Table - MEMBER_BH Register (27Bh)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TMB	4Eh.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 11
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VMB	4Eh.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 11

5.4.60 VLAN Table - MEMBER_CH Register (27Ch)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TMC	4Fh.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 12
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VMC	4Fh.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 12

5.4.61 VLAN Table - MEMBER_DH Register (27Dh)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TMD	50h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 13
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VMD	50h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 13

5.4.62 VLAN Table - MEMBER_EH Register (27Eh)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TME	51h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 14
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VME	51h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 14

5.4.63 VLAN Table - MEMBER_FH Register (27Fh)

Bit	Name	ROM	Default	Description
15:14	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
13:8	VTAB_TMF	52h.[13:8]	PSE0 RW	Tagged Member of VLAN Entry 15
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	VTAB_VMF	52h.[5:0]	PSE0 RW	VLAN Member of VLAN Entry 15

5.4.64 VLAN Table - Priority Enable Register (290h)

Bit	Name	ROM	Default	Description
15:0	VTAB_PEN	53h.[15:0]	PSE0 RW	VLAN-based Priority Enable This field is used to enable VLAN-based priority of each entry. The priority queue number is decided in VTAB_QUE field of register 293H to 299H. 0: Disable 1: Enable

5.4.65 VLAN Table - STP Index Enable Register (292h)

Bit	Name	ROM	Default	Description
15:0	VTAB_STPE	55h.[15:0]	PSE0 RW	VLAN-based STP Enable DM8806 supports four Spanning Tree Instance in MSTP application. This field is used to enable the function of each entry. The index of Spanning Tree Instance of each VLAN is listed in VTAB_STPIDX field of register 293H to 299H. 0: Disable 1: Enable

5.4.66 VLAN Table - Misc_0 Register (293h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPID X_1	56h.[14:13]	PSE0 RW	STP Index of VLAN Entry 1
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_1	56h.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 1
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPID X_0	56h.[6:5]	PSE0 RW	STP Index of VLAN Entry 0
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_0	56h.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 0

5.4.67 VLAN Table - Misc_1 Register (294h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPID X_3	57h.[14:13]	PSE0 RW	STP Index of VLAN Entry 3
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_3	57h.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 3
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPID X_2	57h.[6:5]	PSE0 RW	STP Index of VLAN Entry 2
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_2	57h.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 2

5.4.68 VLAN Table - Misc_2 Register (295h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPID X_5	58h.[14:13]	PSE0 RW	STP Index of VLAN Entry 5
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_5	58h.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 5
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPID X_4	58h.[6:5]	PSE0 RW	STP Index of VLAN Entry 4
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_4	58h.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 4

5.4.69 VLAN Table - Misc_3 Register (296h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPID X_7	59h.[14:13]	PSE0 RW	STP Index of VLAN Entry 7
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_7	59h.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 7
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPID X_6	59h.[6:5]	PSE0 RW	STP Index of VLAN Entry 6
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_6	59h.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 6

5.4.70 VLAN Table - Misc_4 Register (297h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPIDX_9	5Ah.[14:13]	PSE0 RW	STP Index of VLAN Entry 9
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_9	5Ah.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 9
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPIDX_8	5Ah.[6:5]	PSE0 RW	STP Index of VLAN Entry 8
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_8	5Ah.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 8

5.4.71 VLAN Table - Misc_5 Register (298h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPIDX_B	5Bh.[14:13]	PSE0 RW	STP Index of VLAN Entry 11
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_B	5Bh.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 11
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPIDX_A	5Bh.[6:5]	PSE0 RW	STP Index of VLAN Entry 10
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_A	5Bh.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 10

5.4.72 VLAN Table - Misc_6 Register (299h)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPIDX_D	5Ch.[14:13]	PSE0 RW	STP Index of VLAN Entry 13
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_D	5Ch.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 13
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPIDX_C	5Ch.[6:5]	PSE0 RW	STP Index of VLAN Entry 12
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_C	5Ch.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 12

5.4.73 VLAN Table - Misc_7 Register (29Ah)

Bit	Name	ROM	Default	Description
15	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
14:13	VTAB_STPIDX_F	5Dh.[14:13]	PSE0 RW	STP Index of VLAN Entry 15
12:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9:8	VTAB_QUE_F	5Dh.[9:8]	PSE0 RW	Priority Queue Number of VLAN Entry 15
7	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
6:5	VTAB_STPIDX_E	5Dh.[6:5]	PSE0 RW	STP Index of VLAN Entry 14
4:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1:0	VTAB_QUE_E	5Dh.[1:0]	PSE0 RW	Priority Queue Number of VLAN Entry 14

5.4.74 Snooping Control 0 Register (29Bh)

Bit	Name	ROM	Default	Description
15:14	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
13:8	RPP	17h.[13:8]	PSE0 RW	Router Port Portmap [13] : Port 5 [12] : Port 4 [11] : Port 3 [10] : Port 2 [09] : Port 1 [08] : Port 0 0: Disable 1: Enable
7	UD_RP	17h.[7]	PSE0 RW	User-defined Router Port Enable 0: Disable 1: Enable
6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:4	MC_CTRL	17h.[5:4]	PSE0 RW	Multicast Control Packet Handle 00: Forward Membership Reports to router port. General Query to all port. 01: Mirror to CPU (Forward to CPU also) 10: Trap to CPU (Forward to CPU only) 11: Flood
3:2	UMD_CTRL	17h.[3:2]	PSE0 RW	Unregistered Multicast Data Packet Handle 00: As normal multicast packets 01: Dropped. 10: Trap to CPU 11: Flood except CPU
1	MLDS_EN	17h.[1]	PSE0 RW	MLD Snooping Enable 0: Disable 1: Enable
0	HIGS_EN	17h.[0]	PSE0 RW	Hardware IGMP Snooping Enable 0: Disable 1: Enable

5.4.75 Snooping Control 1 Register (29Ch)

Bit	Name	ROM	Default	Description
15:13	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
12	IGS_TODIS	18h.[12]	PSE0 RW	IGMP Snooping Timeout Scheme Disable 0: Timeout is enabled 1: Timeout is disabled
11:10	RP_TV	18h.[11:10]	PSE0 RW	Router Port Timeout Value Selection 00: 1 times of Query Interval 01: 2 times of Query Interval 10: 3 times of Query Interval (default) 11: 4 times of Query Interval
9:8	IGS_RV	18h.[9:8]	PSE0 RW	Robustness Variable 00: 1 times 01: 2 times (default) 10: 3 times 11: 4 times
7:0	IGS_QI	18h.[7:0]	PSE 7DH RW	Query Interval Default = 125 (sec)

5.4.76 Address Table Control & Status Register (2B0h)

Bit	Name	ROM	Default	Description
15	ATB_S	—	PS0 RO	Address Table Access is Busy 0: Available (Access process is completed) 1: Busy (Access process is operating)
14:13	ATB_CR	—	PS0 RO	Address Table Command Result 00: Command OK, entry doesn't exist a. Create an new entry (Write Command) b. Do noting (Delete Command) c. Entry is not found (Search Command) d. Entry is invalid (Read Command) e. Process is successful (Clear Command) 01: Command OK, entry is exist a. Overwrite entry (Write Command) b. Delete entry (Delete Command) c. Entry is found (Search Command) d. Entry is valid (Read Command) e. Process is successful (Clear Command) 1X: Command Error
12:7	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
6	ATB_CLSE_FID	—	PS0 RW	Enable to Clear Entries with Specified FID 0: Disable 1: Enable
5	ATB_CLSE_PORT	—	PS0 RW	Enable to Clear Entries with Specified Port Number or Port Map (Port number for accessing unicast address table, port map for multicast) 0: Disable 1: Enable
4:2	ATB_CMD	—	PS0 RW	Command 000: Read a entry with sequence number of address table 001: Write a entry with MAC address 010: Delete a entry with MAC address 011: Search a entry with MAC address 100: Clear one or more than one entries with Port or FID 101,110,111: Reserved
1:0	ATB_IDX	—	PS0,RW	Address Table Index 00: Unicast Address Table 01: Multicast Address Table 10: IGMP Table 11: Reserved

5.4.77 Address Table Data 0 Register (2B1h)

Bit	Name	ROM	Default	Description
15:12	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
11:8	ATB_FID	_	PS0 RW	FID Value
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	ATB_PORT	_	PS0 RW	Port Number or Port Map

5.4.78 Address Table Data 1 Register (2B2h)

Bit	Name	ROM	Default	Description
15:0	ATB_DW1	—	PSE0 RW	Address Table Data Word 1

5.4.79 Address Table Data 2 Register (2B3h)

Bit	Name	ROM	Default	Description
15:0	ATB_DW2	—	PSE0 RW	Address Table Data Word 2

5.4.80 Address Table Data 3 Register (2B4h)

Bit	Name	ROM	Default	Description
15:0	ATB_DW3	—	PSE0 RW	Address Table Data Word 3

5.4.81 Address Table Data 4 Register (2B5h)

Bit	Name	ROM	Default	Description
15:0	ATB_DW4	—	PSE0 RW	Address Table Data Word 4

5.4.82 Ethernet Address Register 0 for Magic Packet (2B8h)

Bit	Name	ROM	Default	Description
15:8	ETH_ADR1	19h.[15:8]	PE0 RW	Ethernet Address 1
7:0	ETH_ADR0	19h.[7:0]	PE0 RW	Ethernet Address 0

5.4.83 Ethernet Address Register 1 for Magic Packet (2B9h)

Bit	Name	ROM	Default	Description
15:8	ETH_ADR3	1Ah.[15:8]	PE0 RW	Ethernet Address 3
7:0	ETH_ADR2	1Ah.[7:0]	PE0 RW	Ethernet Address 2

5.4.84 Ethernet Address Register 2 for Magic Packet (2BAh)

Bit	Name	ROM	Default	Description
15:8	ETH_ADR5	1Bh.[15:8]	PE0 RW	Ethernet Address 5
7:0	ETH_ADR4	1Bh.[7:0]	PE0 RW	Ethernet Address 4

5.4.85 WoL Control Register (2BBh)

Bit	Name	ROM	Default	Description
15	STANDBY	10h.[15]	PS0 RW	WOL Standby Mode Enable 0: Disable 1: Enable
14	SLOW_CLK	10h.[14]	PS0 RW	Slow Down System Clock in WOL Standby Mode When WoL Standby Mode is enabled and this bit is set, The system clock is down to to 3.125MHz. 0: Disable 1: Enable
13	MAGIC_EN5	10h.[13]	PS0 RW	Port 5 Magic Packet Interrupt Enable 0: Disable 1: Enable
12	MAGIC_EN4	10h.[12]	PS0 RW	Port 4 Magic Packet Interrupt Enable 0: Disable 1: Enable
11	MAGIC_EN3	10h.[11]	PS0 RW	Port 3 Magic Packet Interrupt Enable 0: Disable 1: Enable
10	MAGIC_EN2	10h.[10]	PS0 RW	Port 2 Magic Packet Interrupt Enable 0: Disable 1: Enable
9	MAGIC_EN1	10h.[9]	PS0 RW	Port 1 Magic Packet Interrupt Enable 0: Disable 1: Enable
8	MAGIC_EN0	10h.[8]	PS0 RW	Port 0 Magic Packet Interrupt Enable 0: Disable 1: Enable
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5	LNK_EN5	—	PS0 RW	Port 5 Link Status Change Interrupt Enable 0: Disable 1: Enable
4	LNK_EN4	—	PS0 RW	Port 4 Link Status Change Interrupt Enable 0: Disable 1: Enable
3	LNK_EN3	—	PS0 RW	Port 3 Link Status Change Interrupt Enable 0: Disable 1: Enable
2	LNK_EN2	—	PS0 RW	Port 2 Link Status Change Interrupt Enable 0: Disable 1: Enable
1	LNK_EN1	—	PS0 RW	Port 1 Link Status Change Interrupt Enable 0: Disable 1: Enable
0	LNK_EN0	—	PS0 RW	Port 0 Link Status Change Interrupt Enable 0: Disable 1: Enable

5.4.86 General Purpose I/O Control Register (2D0h)

Bit	Name	ROM	Default	Description
15:10	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
9	GP1_TYPE	_	PS0 RW	GPIO 1 Buffer Type 0: Open-Collect output 1: Forced output
8	GP0_TYPE	_	PS0 RW	GPIO 0 Buffer Type 0: Open-Collect output 1: Forced output
7:6	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
5	GP1_DIR	_	PS0 RW	GPIO 1 Direction 0: GPIO 1 pin is an input 1: GPIO 1 pin is an output
4	GP0_DIR	_	PS0 RW	GPIO 0 Direction 0: GPIO 0 pin is an input 1: GPIO 0 pin is an output
3:2	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
1	GP1_IN	_	PS0 RW	GPIO 1 Data If GPIO 1 pin is an input, 0: GPIO 1 pin is driven low 1: GPIO 1 pin is driven high If GPIO 1 pin is an output, 0: Set GPIO 1 pin to 0 1: Set GPIO 1 pin to 1
0	GP0_IN	_	PS0 RW	GPIO 0 Data If GPIO 0 pin is an input, 0: GPIO 0 pin is driven low 1: GPIO 0 pin is driven high If GPIO 1 pin is an output, 0: Set GPIO 0 pin to 0 1: Set GPIO 0 pin to 1

5.5 Chip Control and Status Registers

5.5.1 Vendor ID Register (310h)

Bit	Name	ROM	Default	Description
15:0	VID	04h.[15:0]	PE 0A46h RO	Vendor ID

5.5.2 Product ID Register (311h)

Bit	Name	ROM	Default	Description
15:0	PID	05h.[15:0]	PE 8606h RO	Product ID

5.5.3 Port 4 MAC Control Register (314h)

Bit	Name	ROM	Default	Description
15:12	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
11,10	P4_TB_SEL	0Ch.[11:10]	PET00 RW	Port4 Turbo Speed in RevMII 00: Default TXCLK 25MHz(100M)/2.5MHz(10M) 01: P4 RevMII TXCLK generate 50MHz clock 10: P4 RevMII TXCLK generate 100MHz clock 11: P4 RevMII TXCLK generate 125MHz clock
9:8	P4_DRIVE	0Ch.[9:8]	PET01 RW	Port 4 Output Pin Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
7	P4_SLEW	0Ch.[7]	PET0 RW	Port 4 Output Pin Slew Rate 0: Normal slew rate 1: Low slew rate
6	P4_50M_IN	0Ch.[6]	PE0 RW	50MHz Clock Source Selection Only available when Port 4 be configured as RMII or TP RMII 0: 50MHz clock source from external 1: 50MHz clock source from Internal
5	P4_50MOUT	0Ch.[5]	PET0 RW	50MHz Clock Output Enable Only available when Port 4 be configured as RMII or TP RMII 0: Disable, high impedance 1: Enable, output 50MHz clock
4	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
3	P4_MODE	0Ch.[3]	PET0 RW	Port 4 Force Mode Enable Only available for MII/RevMII/RMII 0: Disable, auto-negotiation mode 1: Enable, force mode
2	P4_LINK	0Ch.[2]	PET0 RW	Port 4 Force Link Only available in force mode 0: Link ON 1: Link OFF
1	P4_DPX	0Ch.[1]	PET0 RW	Port 4 Force Duplex Only available in force mode 0: Full-duplex mode 1: Half-duplex mode
0	P4_SPEED	0Ch.[0]	PET0 RW	Port 4 Force Speed Only availabe in force mode 0: 100M mode 1: 10M mode

5.5.4 Port 5 MAC Control Register (315h)

Bit	Name	ROM	Default	Description
15:10	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
9:8	P5_DRIVE	0Dh.[9:8]	PET01 RW	Port 5 Output Pin Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
7	P5_SLEW	0Dh.[7]	PET0 RW	Port 5 Output Pin Slew Rate 0: Normal slew rate 1: Low slew rate
6	P5_50M_IN	0Dh.[6]	PE0 RW	Port 5 Clock Source Selection Only available when Port 5 be configured as RMII, 0: 50Mhz clock source from external 1: 50Mhz clock source from internal
5	P5_50M_OUT	0Dh.[5]	PET0 RW	Port 5 50MHz Clock Output Enable Only available when Port 5 be configured as RMII, 0: Disable, high impedance 1: Enable, output 50MHz clock
4	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
3	P5_MODE	0Dh.[3]	PET0 RW	Port 5 Force Mode Enable Only available for MII/RevMII/RMII 0: Disable, auto-negotiation mode 1: Enable, force mode
2	P5_LINK	0Dh.[2]	PET0 RW	Port 5 Force Link Only available in force mode 0: Link ON 1: Link OFF
1	P5_DPX	0Dh.[1]	PET0 RW	Port 5 Force Duplex Only available in force mode 0: Full-duplex mode 1: Half-duplex mode
0	P5_SPEED	0Dh.[0]	PET0 RW	Port 5 Force Speed Only availabe in force mode 0: 100M mode 1: 10M mode

5.5.5 Fiber Control Register (316h)

Bit	Name	ROM	Default	Description
15	P01_LFP	08h.[15]	PE0 RW	Port 0 and Port 1 Repeater Enable Enable fiber repeater function with Link Fault Pass through (LFP) ability between Port 0 and Port1. 0: Disable 1: Enable
14:13	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
12	P4_SD	08h.[12]	PE0 RW	Port 4 Fiber Signal Detect Selection Select the source of Fiber SD, only available in fiber mode. The Port 4 operation mode must be configured as internal PHY, i.e. pull-down P4_SET1 and P4_SET0 pins. 0: Fiber SD decode internally 1: Fiber SD input P4_SPD_LED (pin 101)
11	P3_SD	08h.[11]	PE0 RW	Port 3 Fiber Signal Detect Selection Select the source of Fiber SD, only available in fiber mode. 0: Fiber SD decode internally 1: Fiber SD input P3_SPD_LED (pin 102)
10	P2_SD	08h.[10]	PE0 RW	Port 2 Fiber Signal Detect Selection Select the source of Fiber SD, only available in fiber mode. 0: Fiber SD decode internally 1: Fiber SD input P2_SPD_LED (pin 103)
9	P1_SD	08h.[9]	PE0 RW	Port 1 Fiber Signal Detect Selection Select the source of Fiber SD, only available in fiber mode. 0: Fiber SD decode internally 1: Fiber SD input P1_SPD_LED (pin 104)
8	P0_SD	08h.[8]	PE0 RW	Port 0 Fiber Signal Detect Selection Select the source of Fiber SD, only available in fiber mode. 0: Fiber SD decode internally 1: Fiber SD input P0_SPD_LED (pin 105)
7:5	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
4	P4_FIBER	08h.[4]	PET0 RW	Port 4 Firber Mode Enable 0: Disable (Copper) 1: Enable
3	P3_FIBER	08h.[3]	PE0 RW	Port 3 Firber Mode Enable 0: Disable (Copper) 1: Enable
2	P2_FIBER	08h.[2]	PE0 RW	Port 2 Firber Mode Enable 0: Disable (Copper) 1: Enable
1	P1_FIBER	08h.[1]	PE0 RW	Port 1 Firber Mode Enable 0: Disable (Copper) 1: Enable
0	P0_FIBER	08h.[0]	PE0 RW	Port 0 Firber Mode Enable 0: Disable (Copper) 1: Enable

5.5.6 IRQ and LED Control Register (317h)

Bit	Name	ROM	Default	Description
15	IRQ_PIN	06h.[15]	PSE0 RW	IRQ Output Pin Type 0: Force output 1: Open-collected
14	IRQ_POL	06h.[14]	PSE0 RW	IRQ Active Low Enable 0: Active high 1: Active low
13	IRQ_PULSE	06h.[13]	P0 RO	IRQ Output Pulse 0: Assert until source event cleared 1: Assert a 1000ns pulse
12:11	CTL_DRIVE	06h.[12:11]	PET01 RW	Switch Control Output Pin Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
10	CTL_SLEW	06h.[10]	PET0 RW	Switch Control Output Pin Slew Rate 0: Normal slew rate 1: Low slew rate
9:8	LED_DRIVE	06h.[9:8]	PET10 RW	LED Pin Current Driving/Sinking Capability 00: 2mA 01: 4mA 10: 6mA (default) 11: 8mA
7	LED_SLEW	06h.[7]	PET1 RW	LED Pin Slew Rate 0: Normal slew rate 1: Low slew rate (default)
6:2	RESERVED	–	RO	Reserved Write as 0h, ignore when read
1:0	LED_MODE	06h.[1:0]	PET11 RW	LED_MODE 00 : LED mode 0 01 : LED mode 1, dual color mode 10 : LED mode 2 11 : LED mode 3 (default)

5.5.7 Interrupt Status Register (318h)

Bit	Name	ROM	Default	Description
15:3	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
2	MAGIC	–	PS0 RW/C1	Magic Packet Detected Status 0 = No interrupt request present 1 = Interrupt request present
1	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
0	LNKCHG	–	PS0 RW/C1	Link Status Change Status 0 = No interrupt request present 1 = Interrupt request present

5.5.8 Interrupt Mask & Control Register (319h)

Bit	Name	ROM	Default	Description
15:3	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
2	MAGIC_IEN	10h.[2]	PS0 RW	Magic Packet Interrupt Enable 0: Disable 1: Enable
1	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
0	LNKCHG	–	PS0 RW	Link Status Change Interrupt Enable 0: Disable 1: Enable

5.5.9 EEPROM Control & Address Register (31Ah)

Bit	Name	ROM	Default	Description
15:8	EROA	_	PS0 RW	EEPROM Address 8-bit EEPROM word address
7	RESERVED	_	P0 RO	Reserved Write as 0h, ignore when read
6	EETYPE	_	P0 RW	EEPROM Type Selection & Status 0: 93C46 1: 93C66
5	REEP	_	PS0 RW	Reload EEPROM Write 1 and then write 0 to generate a pulse to active EEPROM reload circuit
4	WEP	_	PS0 RW	EEPROM Write Enable 0: Disable 1: Enable
3	EPOS	_	PS0 RW	Access External PHY Enable 0: Disable 1: Enable
2	ERPRR	_	PS0 RW	EEPROM Read Command Launch EEPROM read process by set this bit to one.It is non self-clearing bit, driver need to clear after operation ending.
1	ERPRW	_	PS0 RW	EEPROM Write Command Launch EEPROM write process by set this bit to one.It is non self-clearing bit, driver need to clear after operation ending.
0	ERRE	_	PS0 RO	EEPROM Access Status 0: Busy, accessing EEPROM or external PHY is in progress 1: Idle, accessing EEPROM or external PHY is completed.

5.5.10 EEPROM Data Register (31Bh)

Bit	Name	ROM	Default	Description
15:0	EE_DATA	_	PS0 RW	EEPROM Data 16-bit EEPROM data field

5.5.11 Monitor Register 1 (31Ch)

Bit	Name	ROM	Default	Description
15	STRP_DIS	_	RO	Display the input value of pin 93, STRAP_DIS.
14	RESERVED	–	RO	Reserved Write as 0h, ignore when read
13	TEST3	_	RO	Display the input value of pin 41, TEST3.
12	TEST2	_	RO	Display the input value of pin 69, TEST2.
11	TEST1	_	RO	Display the input value of pin 108, TEST1.
10	RESERVED	–	RO	Reserved Write as 0h, ignore when read
9	RESERVED	–	RO	Reserved Write as 0h, ignore when read
8	P2_SPD	_	RO	Display the latched value of pin 103, P2_SPD_LED.
7	P1_SPD	_	RO	Display the latched value of pin 104, P1_SPD_LED.
6	P0_SPD	_	RO	Display the latched value of pin 105, P0_SPD_LED.
5:3	RESERVED	–	RO	Reserved Write as 0h, ignore when read
2	EECS	_	RO	Display the latched value of pin 80, EECS.
1	EECK	_	RO	Display the latched value of pin 81, EECK.
0	RESERVED	–	RO	Reserved Write as 0h, ignore when read

5.5.12 Monitor Register 2 (31Dh)

Bit	Name	ROM	Default	Description
15	SPDLED3	–	RO	Display the latched value of pin 102, P3_SPD_LED.
14	SPDLED4	–	RO	Display the latched value of pin 101, P4_SPD_LED.
13	RESERVED	–	RO	Reserved Write as 0h, ignore when read
12	FDXLED4	–	RO	Display the latched value of pin 107, P4_FDX_LED.
11	FDXLED3	–	RO	Display the latched value of pin 110, P3_FDX_LED.
10	FDXLED2	–	RO	Display the latched value of pin 111, P2_FDX_LED.
9	FDXLED1	–	RO	Display the latched value of pin 112, P1_FDX_LED.
8	FDXLED0	–	RO	Display the latched value of pin 113, P0_FDX_LED.
7:6	RESERVED	–	RO	Reserved Write as 0h, ignore when read
5	LNKLED4	–	RO	Display the latched value of pin 51, P4_LNK_LED.
4:0	RESERVED	–	RO	Reserved Write as 0h, ignore when read

5.5.13 Monitor Register 3 (31Eh)

Bit	Name	ROM	Default	Description
15	LNKLED3	–	RO	Display the latched value of pin 48, P3_LNK_LED.
14	LNKLED2	–	RO	Display the latched value of pin 47, P2_LNK_LED.
13	LNKLED1	–	RO	Display the latched value of pin 43, P1_LNK_LED.
12	LNKLED0	–	RO	Display the latched value of pin 42, P0_LNK_LED.
11	P4S0	–	RO	Display the input value of pin 98, P4_SET0.
10	CFG4	–	RO	Display the input value of pin 98, P4_CFG.
9	P4S1	–	RO	Display the latched value of pin 100, P4_SET1.
8:1	RESERVED	–	RO	Reserved Write as 0h, ignore when read
0	MDC_EXT	–	RO	Display the latched value of pin 68, PHY_MDC.

5.5.14 Debug Monitor Pin Register (31Fh)

Bit	Name	ROM	Default	Description
15:14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
7	MONI_EN	–	PS0 RW	Debug Monitor Enable 0: Disable 1: Enable
3:0	MONI_IDX	–	PS0 RW	Debug Monitor Table Index

5.5.15 Memory Access Enable Register (330h)

Bit	Name	ROM	Default	Description
15	SEL_RAM	–	PS0 RW	Memory Access Selection 0: Select 48K SRAM 1: Select 25K SRAM
14	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
13	WRMEM	–	PS0 RW	Memory Write Enable 0: Disable 1: Enable
12:0	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read

5.5.16 Memory Address Register (331h)

Bit	Name	ROM	Default	Description
15:0	MDA	–	PS0 RW	Memory Data Address

5.5.17 Memory Dummy Data Register (332h)

Bit	Name	ROM	Default	Description
15:0	MDRD	–	RO	Memory Dummy Read Data

5.5.18 Memory Read Data Register (333h)

Bit	Name	ROM	Default	Description
15:0	MRD	–	RO	Memory Data Read

5.5.19 Memory Write Data Register (334h)

Bit	Name	ROM	Default	Description
15:0	MWD	–	PS0 WO	Memory Write Data

5.5.20 Memory Write Data Low Byte Register (335h)

Bit	Name	ROM	Default	Description
15:8	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
7:0	MWDL	—	PS0 WO	Memory Write Data Low Bits 7~0

5.5.21 Memory Write Data High Byte Register (336h)

Bit	Name	ROM	Default	Description
15:8	MWDH	—	PS0 WO	Memory Write Data High Bits 15~8
7:0	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read

5.5.22 System Clock Select Register (338h)

Bit	Name	ROM	Default	Description
15:3	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
2:0	CLK_TYPE	–	PS0 RW	Internal System Clock Rate Selection 000: 50MHz 001: 66Mhz 010: 83MHz 011: 100MHz 10X: 25MHz 11X: 3.125MHz

5.5.23 Serial Bus Error Check Register (339h)

Bit	Name	ROM	Default	Description
15:9	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
8	SMI_ERR	–	PS0 RO	SMI Bus Error Status 0: Checksum is correct 1: Checksum is wrong
7:0	SMI_CSUM	–	PS0 RW	Checksum field for SMI Bus Error Check

5.5.24 Serial Bus Control Register (33Ah)

Bit	Name	ROM	Default	Description
15:1	RESERVED	–	P0 RO	Reserved Write as 0h, ignore when read
0	SMI_ECE	–	PS0 RW	SMI Bus Error Check Enable 0: Disable 1: Enable

5.5.25 Virtual PHY Control Register (33Dh)

Bit	Name	ROM	Default	Description
15:10	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
9	VPHY_LNK_AND	—	PS0 RW	Virtual PHY Link with AND Mode 0: Disable 1: Enable
8	VPHY_LNK_OR	—	PS1 RW	Virtual PHY Link with OR Mode 0: Disable 1: Enable
7:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	VPHY_PMAP	—	PS 1Fh RW	Virtual PHY Link Port Map [05]: Port 5 | [04]: Port 4 | [03]: Port 3 [02]: Port 2 | [01]: Port 1 | [00]: Port 0 Note: Valid if Reg33DH.[9] or Reg33DH.[8] is enabled

5.5.26 PHY Control Test Register (33Eh)

Bit	Name	ROM	Default	Description
15	AT_MDIX0	07h.[15]	P0 RW	Port 0 Auto-MDIX Control Disable 0: Disable 1: Enable
14	AT_MDIX1	07h.[14]	P0 RW	Port 1 Auto-MDIX Control Disable 0: Disable 1: Enable
13	AT_MDIX2	07h.[13]	P0 RW	Port 2 Auto-MDIX Control Disable 0: Disable 1: Enable
12	AT_MDIX3	07h.[12]	P0 RW	Port 3 Auto-MDIX Control Disable 0: Disable 1: Enable
11	AT_MDIX4	07h.[11]	P0 RW	Port 4 Auto-MDIX Control Disable 0: Disable 1: Enable
10:4	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
3:0	RESERVED	—	P3 RW	Reserved Write as 3h, ignore when read

5.5.27 Disable Port Control Register (399h)

Bit	Name	ROM	Default	Description
15:6	RESERVED	—	P0 RO	Reserved Write as 0h, ignore when read
5:0	PORT_DIS	—	P0 RW	Disable Buffer Usage of Port It is used to release the reserved buffers on useless port for memory utilization improvment. Notice that Switch must be software reset after this function is applied. [05]: Port 5 | [04]: Port 4 | [03]: Port 3 [02]: Port 2 | [01]: Port 1 | [00]: Port 0 0: Enable, reserve buffers on selected port. 1: Disable, release buffers on selected port.

6. EEPROM Format

<table>
<tr><th>Name</th><th>Word</th><th>Description</th></tr>
<tr><td>Signature</td><td>00h</td><td>When this word is 1049h, the EEPROM data is valid and can be loaded to DM8806.</td></tr>
<tr><td>RESERVED</td><td>01h~02h</td><td>Reserved</td></tr>
<tr><td>Load Control 0</td><td>03h</td><td>EEPROM Load Control 0
<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>[01:00]</td><td>Load enable of word 04h & 05h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[03:02]</td><td>Load enable of word 06h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[05:04]</td><td>Load enable of word 08h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[07:06]</td><td>Load enable of word 09h & 0Ah
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[09:08]</td><td>Load enable of word 0Bh,0Ch,0Dh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[11:10]</td><td>Load enable of word 10h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[13:12]</td><td>Reserved
Set to “00b” or “11b” in application</td></tr>
<tr><td>[15:14]</td><td>Load enable of word 07h
01b: Enable, 00b/10b/11b: Disable</td></tr>
</table></td></tr>
<tr><td>Vendor ID</td><td>04h</td><td>Vendor ID (Default: 0A46h)
If bit [01:00] of word 03h is “01b”, this field will be loaded to REG 310h</td></tr>
<tr><td>Product ID</td><td>05h</td><td>Product ID
If bit [01:00] of word 03h is “01b”, this field will be loaded to REG 311h</td></tr>
<tr><td>IRQ &
LED Control</td><td>06h</td><td>IRQ & LED Control
If bit [03:02] of word 03h is “01b”, this field will be loaded to REG 317h</td></tr>
<tr><td>PHY control</td><td>07h</td><td>PHY Auto-MDIX Control
If bit [15:14] of word 03h is “01b”, this field will be loaded to REG 33Eh
<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>[10:00]</td><td>Reserved</td></tr>
<tr><td>[11]</td><td>Port 4 AUTO-MDIX control
1: ON, 0: OFF</td></tr>
<tr><td>[12]</td><td>Port 3 AUTO-MDIX control
1: ON, 0: OFF</td></tr>
<tr><td>[13]</td><td>Port 2 AUTO-MDIX control
1: ON, 0: OFF</td></tr>
<tr><td>[14]</td><td>Port 1 AUTO-MDIX control
1: ON, 0: OFF</td></tr>
<tr><td>[15]</td><td>Port 0 AUTO-MDIX control
1: ON 0: OFF</td></tr>
</table></td></tr>
<tr><td>Fiber control</td><td>08h</td><td>PHY Fiber Control
If bit [05:04] of word 03h is "01b", this field will be loaded to REG 316h</td></tr>
<tr><td>Phy Vendor ID</td><td>09h</td><td>Internal PHY ID1
If bit [07:06] of word 03h is “01b”, this field will be loaded to Identifier 1 Register of all internal PHYs.</td></tr>
<tr><td>Phy Device ID</td><td>0Ah</td><td>Internal PHY ID2
If bit [07:06] of word 03h is “01b”, this field will be loaded to Identifier 2 Register of all internal PHYs.</td></tr>
</table>

<table>
<tr><td>Port 4 MAC Control</td><td>0Ch</td><td>Port 4 MAC Control
If bit [09:08] of word 03h is “01b”, this field will be loaded to REG 314h</td></tr>
<tr><td>Port 5 MAC Control</td><td>0Dh</td><td>Port 5 MAC Control
If bit [09:08] of word 03h is “01b”, this field will be loaded to REG 315h</td></tr>
<tr><td>Load Control 1</td><td>0Eh</td><td>EEPROM Load Control 1
<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>[01:00]</td><td>Load enable of word 12h ~ 16h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[03:02]</td><td>Load enable of word 17h &18h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[05:04]</td><td>Load enable of word 1Ch ~ 24h
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[07:06]</td><td>Load enable of word 26h ~ 2Eh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[09:08]</td><td>Load enable of word 30h ~ 5Dh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[11:10]</td><td>Reserved
Set to “00b” or “11b” in application</td></tr>
<tr><td>[13:12]</td><td>Reserved
Set to “00b” or “11b” in application</td></tr>
<tr><td>[15:14]</td><td>Reserved
Set to “00b” or “11b” in application</td></tr>
</table></td></tr>
<tr><td>Load Control 2</td><td>0Fh</td><td>EEPROM Load Control 2
<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>[01:00]</td><td>Load enable of word 80h ~ 8Bh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[03:02]</td><td>Load enable of word 90h ~ 9Bh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[05:04]</td><td>Load enable of word A0h ~ ABh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[07:06]</td><td>Load enable of word B0h ~ BBh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[09:08]</td><td>Load enable of word C0h ~ CBh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[11:10]</td><td>Load enable of word D0h ~ DBh
01b: Enable, 00b/10b/11b: Disable</td></tr>
<tr><td>[13:12]</td><td>Reserved
Set to “00b” or “11b in application</td></tr>
<tr><td>[15:14]</td><td>Reserved
Set to “00b” or “11b” in application</td></tr>
</table></td></tr>
<tr><td>Magic Packet Control</td><td>10h</td><td>If bit [11:10] of word 03h is “01b”, this field will be loaded to registers that is shown in the following table.
<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>[00]</td><td>Reserved</td></tr>
<tr><td>[01]</td><td>10M TX power saving in bit 10 of all PHY register PSCR
(Bit 10 of REG 054h/074h/094h/0B4h/0D4h)
1: Enable, 0: Disable</td></tr>
<tr><td>[02]</td><td>Magic packet interrupt enable
(REG 319h.[2])
1: Enable, 0: Disable</td></tr>
<tr><td>[07:03]</td><td>Reserved</td></tr>
</table></td></tr>
</table>

		[13:08] Per port magic packet interrupt enable (REG 2BBh.[13:08]) 1: Enable, 0: Disable [14] Slow down system clock in WOL standby mode (REG 2BBh.[14]) 1: Enable, 0: Disable [15] WOL standby mode enable (REG 2BBh.[15]) 1: Enable, 0: Disable
RESERVED	11h	Reserved
Switch Control	12h	If bit [01:00] of word 0Eh is “01b”, this field will be loaded to REG 212h
CPU Port & Mirror Control	13h	If bit [01:00] of word 0Eh is “01b”, this field will be loaded to REG 213h
Special Tag Ether-Type	14h	If bit [01:00] of word 0Eh is “01b”, this field will be loaded to REG 214h
Global Learning & Aging Control	15h	If bit [01:00] of word 0Eh is “01b”, this field will be loaded to REG 215h
MIB Counter Disable	16h	If bit [01:00] of word 0Eh is “01b”, this field will be loaded to REG 230h
Snoop Control 0	17h	If bit [03:02] of word 0Eh is “01b”, this field will be loaded to REG 29Bh
Snoop Control 1	18h	If bit [03:02] of word 0Eh is “01b”, this field will be loaded to REG 29Ch
ETH_ADR	19h~1Bh	Ethernet Address for Magic Packet. Word 19h will be loaded to REG 2B8h Word 1Ah will be loaded to REG 2B9h Word 1Bh will be loaded to REG 2Bah
VLAN Priority Map Register	1Ch	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 217h
TOS Priority Map 0	1Dh	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 218h
TOS Priority Map 1	1Eh	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 219h
TOS Priority Map 2	1Fh	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 21Ah
TOS Priority Map 3	20h	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 21Bh
TOS Priority Map 4	21h	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 21Ch
TOS Priority Map 5	22h	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 21Dh
TOS Priority Map 6	23h	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 21Eh
TOS Priority Map 7	24h	If bit [05:04] of word 0Eh is “01b”, this field will be loaded to REG 21Fh
RESERVED	25h	Reserved
Special Packet Control 0	26h	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 234h.
Special Packet Control 1	27h	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 235h.
Special Packet Control 2	28h	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 236h.
Special Packet Control 3	29h	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 237h.
Special Packet Control 4	2Ah	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 238h.
Special Packet Control 5	2Bh	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 239h.
Special Packet Control 6	2Ch	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 23Ah.
Special Packet Control 7	2Dh	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 23Bh.
Special Packet Control 8	2Eh	If bit [07:06] of word 0Eh is “01b”, this field will be loaded to REG 23Ch.

RESERVED	2Fh	Reserved
QinQ TPID Register	30h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 23Dh.
VLAN Mode & Rule Control	31h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 23Eh.
VLAN Table - Valid Control	32h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 23Fh.
VLAN Table - ID_0H	33h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 250h.
VLAN Table - ID_1H	34h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 251h.
VLAN Table - ID_2H	35h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 252h.
VLAN Table - ID_3H	36h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 253h.
VLAN Table - ID_4H	37h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 254h.
VLAN Table - ID_5H	38h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 255h.
VLAN Table - ID_6H	39h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 256h.
VLAN Table - ID_7H	3Ah	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 257h.
VLAN Table - ID_8H	3Bh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 258h.
VLAN Table - ID_9H	3Ch	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 259h.
VLAN Table - ID_AH	3Dh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 25Ah.
VLAN Table - ID_BH	3Eh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 25Bh.
VLAN Table - ID_CH	3Fh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 25Ch.
VLAN Table - ID_DH	40h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 25Dh.
VLAN Table - ID_EH	41h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 25Eh.
VLAN Table - ID_FH	42h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 25Fh.
VLAN Table - MEMBER_0H	43h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 270h.
VLAN Table - MEMBER_1H	44h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 271h.
VLAN Table - MEMBER_2H	45h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 272h.
VLAN Table - MEMBER_3H	46h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 273h.
VLAN Table - MEMBER_4H	47h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 274h.
VLAN Table - MEMBER_5H	48h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 275h.
VLAN Table - MEMBER_6H	49h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 276h.
VLAN Table - MEMBER_7H	4Ah	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 277h.
VLAN Table - MEMBER_8H	4Bh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 278h.
VLAN Table - MEMBER_9H	4Ch	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 279h.
VLAN Table - MEMBER_AH	4Dh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 27Ah.
VLAN Table - MEMBER_BH	4Eh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 27Bh.
VLAN Table - MEMBER_CH	4Fh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 27Ch.
VLAN Table - MEMBER_DH	50h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 27Dh.
VLAN Table - MEMBER_EH	51h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 27Eh.

VLAN Table - MEMBER_FH	52h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 27Fh.
VLAN Table - Priority Enable	53h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 290h.
VLAN Table - Priority Replace Enable	54h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 291h.
VLAN Table - STP Index Enable	55h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 292h.
VLAN Table - Misc_0	56h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 293h.
VLAN Table - Misc_1	57h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 294h.
VLAN Table - Misc_2	58h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 295h.
VLAN Table - Misc_3	59h	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 296h.
VLAN Table - Misc_4	5Ah	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 297h.
VLAN Table - Misc_5	5Bh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 298h.
VLAN Table - Misc_6	5Ch	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 299h.
VLAN Table - Misc_7	5Dh	If bit [09:08] of word 0Eh is “01b”, this field will be loaded to REG 29Ah.
RESERVED	5Eh~7Fh	Reserved
P0 Basic Control 0	80h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 111h.
P0 Basic Control 1	81h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 112h.
P0 Block Control 0	82h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 113h.
P0 Block Control 1	83h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 114h.
P0 Bandwidth Control	84h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 115h.
P0 VLAN Tag Information	85h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 116h.
P0 Priority & VLAN Control	86h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 117h.
P0 Security Control	87h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 118h.
P0 Advanced Control	88h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 119h.
P0 Memory Configuration	89h	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 11Ah.
P0 Discard packet limitation	8Ah	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 11Bh.
P0 EEE Control	8Bh	If bit [01:00] of word 0Fh is “01b”, this field will be loaded to REG 11Eh.
RESERVED	8Ch~8Fh	Reserved
P1 Basic Control 0	90h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 131h.
P1 Basic Control 1	91h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 132h.
P1 Block Control 0	92h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 133h.
P1 Block Control 1	93h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 134h.
P1 Bandwidth Control	94h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 135h.
P1 VLAN Tag Information	95h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 136h.
P1 Priority & VLAN Control	96h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 137h.
P1 Security Control	97h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 138h.
P1 Advanced Control	98h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 139h.
P1 Memory Configuration	99h	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 13Ah.
P1 Discard packet limitation	9Ah	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 13Bh.
P1 EEE Control	9Bh	If bit [03:02] of word 0Fh is “01b”, this field will be loaded to REG 13Eh.

RESERVED	9Ch~9Fh	Reserved
P2 Basic Control 0	A0h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 151h.
P2 Basic Control 1	A1h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 152h.
P2 Block Control 0	A2h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 153h.
P2 Block Control 1	A3h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 154h.
P2 Bandwidth Control	A4h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 155h.
P2 VLAN Tag Information	A5h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 156h.
P2 Priority & VLAN Control	A6h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 157h.
P2 Security Control	A7h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 158h.
P2 Advanced Control	A8h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 159h.
P2 Memory Configuration	A9h	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 15Ah.
P2 Discard packet limitation	AAh	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 15Bh.
P2 EEE Control	ABh	If bit [05:04] of word 0Fh is “01b”, this field will be loaded to REG 15Eh.
RESERVED	ACh~AFh	Reserved
P3 Basic Control 0	B0h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 171h.
P3 Basic Control 1	B1h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 172h.
P3 Block Control 0	B2h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 173h.
P3 Block Control 1	B3h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 174h.
P3 Bandwidth Control	B4h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 175h.
P3 VLAN Tag Information	B5h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 176h.
P3 Priority & VLAN Control	B6h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 177h.
P3 Security Control	B7h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 178h.
P3 Advanced Control	B8h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 179h.
P3 Memory Configuration	B9h	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 17Ah.
P3 Discard packet limitation	BAh	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 17Bh.
P3 EEE Control	BBh	If bit [07:06] of word 0Fh is “01b”, this field will be loaded to REG 17Eh.
RESERVED	BCh~BFh	Reserved
P4 Basic Control 0	C0h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 191h.
P4 Basic Control 1	C1h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 192h.
P4 Block Control 0	C2h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 193h.
P4 Block Control 1	C3h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 194h.
P4 Bandwidth Control	C4h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 195h.
P4 VLAN Tag Information	C5h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 196h.
P4 Priority & VLAN Control	C6h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 197h.
P4 Security Control	C7h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 198h.
P4 Advanced Control	C8h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 199h.
P4 Memory Configuration	C9h	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 19Ah.

P4 Discard packet limitation	CAh	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 19Bh.
P4 EEE Control	CBh	If bit [09:08] of word 0Fh is “01b”, this field will be loaded to REG 19Eh.
RESERVED	CCh~CFh	Reserved
P5 Basic Control 0	D0h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B1h.
P5 Basic Control 1	D1h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B2h.
P5 Block Control 0	D2h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B3h.
P5 Block Control 1	D3h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B4h.
P5 Bandwidth Control	D4h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B5h.
P5 VLAN Tag Information	D5h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B6h.
P5 Priority & VLAN Control	D6h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B7h.
P5 Security Control	D7h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B8h.
P5 Advanced Control	D8h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1B9h.
P5 Memory Configuration	D9h	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1BAh.
P5 Discard packet limitation	DAh	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1BBh.
P5 EEE Control	DBh	If bit [11:10] of word 0Fh is “01b”, this field will be loaded to REG 1BEh.
RESERVED	DCh~FFh	Reserved

7. Function Description

7.1 Switch Functions

7.1.1 Address Learning

The DM8806 stores MAC addresses, port number and time stamp information in the Hash-based Address Table. The table can learn up to 2K unicast address entries. The DM8806 provides two methods to learn address in the table, self-learning and manual learning.

◆ **Self-learning**

The self-learning mechanism means the DM8806 learn the MAC addresses of incoming packets in real time without CPU's assistance. The switch engine creates a new entry if incoming packet's Source Address (SA) does not exist and the packet is valid (error-free). If SA was found and incoming port mismatch with port number in table, update the entry with SA and incoming port number. Those entries will be created, updated or aged dynamically. Besides, the DM8806 has an option to disable address learning for individual port. This feature can be set by bit 12 of per port register 11h (i.e. 111h, 131h, 151h, 171h, 191h, and 1B1h).

◆ **Manual Learning**

The DM8806 also provides manual learning mechanism with CPU's assistance. The CPU can create, update or delete entry for flexible management. In addition to above, the entry can be set as static one that will not be aged-out.

7.1.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time. The period can be programmed or disabled through bit 0 & 1 of register 215h.

7.1.3 Packet Forwarding

The DM8806 forwards the incoming packet according to following decision:

(1). If Destination Address (DA) is multicast/broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.
(2). Switch engine would look up address table based on DA when incoming packets is uni-cast. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.
(3). Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM8806 will filter incoming packets under following conditions:

(1). Error packets, including CRC errors, alignment errors, illegal size errors.
(2). IEEE 802.3X PAUSE packets.
(3). If incoming packet is uni-cast and its destination port number is equal to source port number

7.1.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

7.1.5 Back-off Algorithm

The DM8806 implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

7.1.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

7.1.7 Half Duplex Flow Control

The DM8806 supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM8806 sends jam pattern and results in a collision.

7.1.8 Full Duplex Flow Control

The DM8806 supports IEEE standard 802.3x flow control frames on both transmit and receive sides. On the receive side, The DM8806 will defer transmitting next normal frames, if it receives a pause frame from link partner. On the transmit side, The DM8806 issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM8806 sends out a pause frame with zero pause time allows traffic to resume immediately.

7.1.9 Partition Mode

The DM8806 provides a partition mode for each port. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

◆ **Entering Partition State**

A port will enter the Partition State when either of the following conditions occurs:

(1). The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
(2). The port detects a single collision which occurs for more than 512 bit times.
(3). Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

◆ **While in Partition State**

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

◆ **Exiting from Partition State**

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

7.1.10 Broadcast Storm Filtering

The DM8806 has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability. There are two types of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through bit 12 of per port register 12h. The broadcast storm threshold can be programmed by EEPROM or per port register 5h, the default setting is no broadcast storm protecting.

7.1.11 Bandwidth Control

The DM8806 supports two types of bandwidth control for each port. One is the ingress and egress bandwidth rate can be controlled separately, the other is combined together, this function can be set through bit 14 of per port register 12h. The bandwidth control is disabled by default. To separate bandwidth control mode, the threshold rate is defined in per port register 5h. For combined mode, it is defined in bit 3~0 of per port register 15h.

The behavior of bandwidth control as below:

(1). For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.
(2). For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.
(3). In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

7.1.12 Port Monitoring Support

The DM8806 supports “Port Monitoring” function on per port base, detail as below:

◆ **Sniffer Port and Monitor Port**

There is only one port can be selected as “sniffer port” by bit 5~3 of register 213h, multiple ports can be set as “receive monitor port” or “transmit monitor port” in per-port register 11h.

◆ **Receive monitor**

All packets received on the “receive monitor port” are send a copy to “sniffer port”. For example, port 0 is set as “receive monitor port” and port 2 is selected as a “sniffer port”. If a packet is received form port 0 and predestined to port 1 after forwarding decision, the DM8806 will forward it to port 1 and port 2 in the end.

◆ **Transmit monitor**

All packets transmitted on the “transmit monitor port” are send a copy to “sniffer port”. For example, port 1 is set as “transmit monitor port” and port 2 is selected as “sniffer port”. If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM8806 will forward it to port 1 and port 2 in the end.

◆ **Exception**

The DM8806 has an optional setting that broadcast/multicast packets are not monitored (see bit 11 of per port register 12h). It’s useful to avoid unnecessary bandwidth.

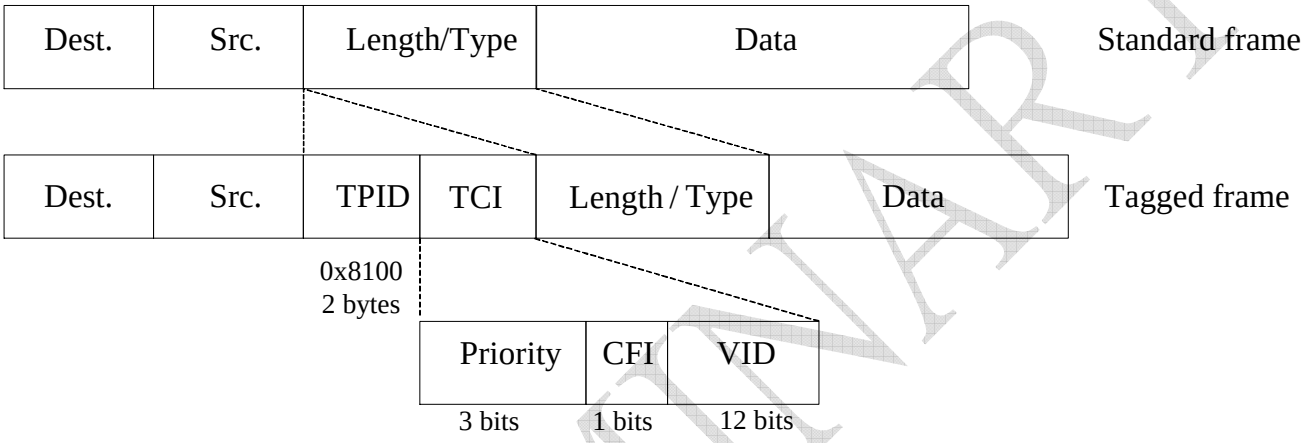
7.1.13 VLAN Support

◆ **Port-Based VLAN**

The DM8806 supports port-based VLAN as default, up to 16 groups. Each port has a default VID called PVID (Port VID, in bit 11~0 of per port register 16H). The DM8806 used 12 bits PVID as index and mapped with registers 250H~25FH to define the VLAN groups.

◆ **802.1q-Based VLAN**

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).



The DM8806 also supports 16 802.1Q-based VLAN groups, as specified in bit 0 of register 23Eh. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM8806 used full 12 bits VID of received packet with VLAN tag and VLAN table ID registers (250h~25Fh) and then define members by VLAN Group Mapping Register (270h~27Fh) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.

◆ **Tag/Untag**

User can define each port as Tag port or Un-tag port by bit 14 of per port register 17h in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

(1). Receive untagged packet and forward to Un-tag port.
Received packet will forward to destination port without modification.

(2). Receive tagged packet and forward to Un-tag port.
The DM8806 will remove the tag from the packet and recalculate CRC before sending it out.

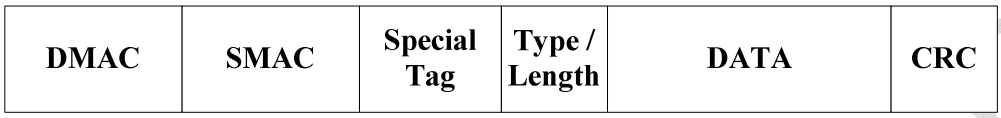
(3). Receive untagged packet and forward to Tag port.
The DM8806 will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

(4). Receive tagged packet and forward to Tag port.
Received packet will forward to destination port without modification.

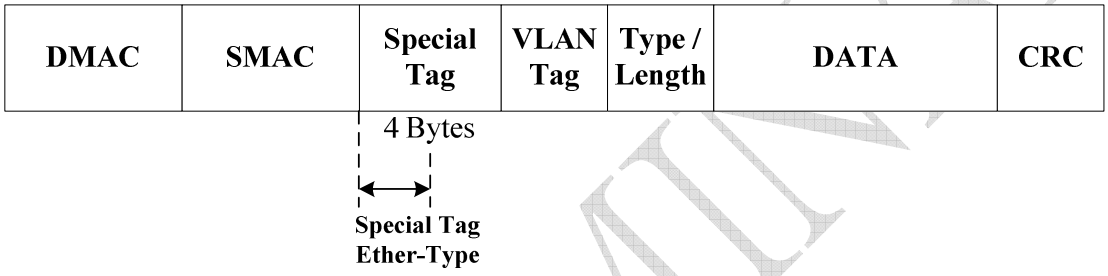
7.1.14 Special Tag

The Special Tag function provided by the DM8806 is used to exchange control and status information between Switch and CPU within frame. An extra 4-bytes tag is added into frame to carry different content according to direction of special tag frame. Received special tag (CPU → Switch) specifies the desired port mapping of packet sent by CPU and some configurations about frame handle rules. Transmitted special tag (Switch → CPU) indicates the source port number of incoming frame.
The following figure shows special tag frame format. In left 2 bytes of special tag field, there is an identifier called Special Tag Ether-Type that can use to recognize special tag frame. The value of this field can be set by REG 23DH.

Frame without VLAN Tag



Frame with VLAN Tag



The detail information carried by received special tag is described as below. Through received special tag, CPU can tell switch the handle rule per frame over the internal setting. This feature can be enabled through REG 213H bit 6.

Received Special Tag(CPU → Switch) 4-byte Format:

Byte 0/1	[15:0]	Special Tag Ether-Type (Default: 0x8086)
Byte 2	[7]	Reserved
Byte 2	[6]	ST_PMAP_en, ST_PMAP Enable
Byte 2	[5:0]	ST_PMAP, Force to assign forwarding port map
Byte 3	[7]	Reserved
Byte 3	[6]	ST_CVLAN, Cross VLAN 0: This frame obeys VLAN boundary. 1: This frame can cross VLAN boundary.
Byte 3	[5]	ST_LRN_DIS, Disable learning 0: This frame will be learned 1: This frame will not be learned
Byte 3	[4]	ST_PRI_EN, ST_PRI Enable
Byte 3	[3:2]	ST_PRI, Priority Queue Number (0~3) 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3
Byte 3	[1:0]	ST_TAG 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved

Beside, transmitted special tag is used to indicate source port number. CPU can use this message to judge the incoming port number of the frame. REG 213H bit 7 can enable this feature by setting to 1.

Transmitted Special Tag (Switch → CPU) 4-byte Format:

Byte 0/1	[15:0]	Special Tag Ether-Type (Default: 0x8086)
Byte 2	[7:3]	Reserved
Byte 2	[2:0]	ST_SPORT, Source Port Number (0~5)
Byte 3	[7:0]	Reserved

7.1.15 Priority Support

The DM8806 supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing. The DM8806 provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM8806 offers four level queues for transmit on per-port based.
The DM8806 provides two packet scheduling algorithms: Weighted Fair Queuing and Strict Priority Queuing. Weighted Fair Queuing (WFQ) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The Packet on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in bit 5 of per port register 17H.

◆ **Port-Based Priority**

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in bit 1~0 of per port register 17H.

◆ **802.1p-Based Priority**

The DM8806 extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers 217H to determine which transmit queue is designated. The VLAN Priority Map is programmable.

◆ **DiffServ-Based Priority**

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (218H~21FH) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see bit 7 of register 23EH.

7.1.16 Address Table Accessing

◆ **Type of Address Table**

There are three types of address table in the DM8806. The description is represented below:

(1). Unicast Address Table

This table is used for destination MAC address lookup and source MAC address learning. The table can have up to 2048 entries. If the table is full, the latest one will kick out the eldest one. The programming method can refer to next section.

(2). Multicast Address Table

The table that stores multicast addresses shares with unicast address table and can be maintained by host CPU for custom filtering and forwarding multicast packets. If the table is full, the latest one will kick out the eldest one. All of entries in multicast address table are static one. In addition to host CPU, multicast address table can be manipulated by internal switch engine, if hardware-based IGMP Snooping function is enabled.

(3). IGMP Membership Table

This table is used to establish IPv4 multicast forwarding rule under IGMP protocol if hardware-based IGMP Snooping function is enabled. It is automatic maintained by internal engine according to snooping IGMP control packets, and can only support to read out by the host CPU. The maximum of entries of table is 32. If the table is full, never join anymore.

◆ Access Rules of Address Table

In DM8806, unicast and multicast address table support “Write”, “Delete”, ”Search”, “Read” and “Clear” commands. However, for IGMP membership table, there are only three different type commands such as “Write”, “Delete” and “Read”. The DM8806 procedure and flow chart of Entry Access is described as following:

- Entry Write

(1). Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the MAC address to the Address Table Data 1~3 Registers (Reg2B2H~2B4H).

(3). Write the Port Number or Port Map to Address Table Data 0 Register (Reg2B1.[2:0]).

(4). If need, write the entry’s attribute such as static to Address Table Data 4 Register (Reg2B5H.0).

(5). Write the “WRITE” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.

(6). Check the busy bit again, wait for available.

(7). Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13])

- Entry Delete

(1). Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the MAC address to the Address Table Data 1~3 Registers (Reg2B2H~2B4H).

(3). Write the “DELETE” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation

(4). Check the busy bit again, wait for available.

(5). Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13]).

- Entry Search

(1). Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the MAC address to the Address Table Data 1~3 Registers (Reg2B2H~2B4H).

(3). Write the “SEARCH” command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.

(4). Check the busy bit again, wait for available.

(5). Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13]).

(6). Read the Port Number or Port Map to Address Table Data 0 Register (Reg2B1.[2:0]).

(7). If need, read the entry sequence (the sequence number of entry in address table) from Address Table Data 1 Register (Reg2B2H).

(8). If need, read the entry’s attributes that include static (unicast address table only) and IGMP Entry (multicast address table only) from Address Table Data 4 Register (Reg2B5H.0 for static and Reg2B5h.12 for IGMP Entry).

- Entry Read

(1). Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the entry sequence to the Address Table Data 1 Register (Reg2B2H).

(3). Write the "READ" command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.

(4). Check the busy bit again, wait for available.

(5). Read the command status from Address Table Control & Status Register (Reg2B0H.[14:13]).

(6). Read the Port Number or Port Map to Address Table Data 0 Register (Reg2B1.[2:0]).

(7). If target is unicast or multicast address table, read the entry's MAC address from Address Table Data 1~3 Register (Reg2B2H~2B4H). If target is IGMP membership table, read the real memory address from Address Table Data 1 Register (Reg2B2H.[10:0]).

(8). If target is unicast address table, read the entry's attributes such as static from Address Table Data 4 Register (Reg2B5H.0). For multicast address table, IGMP Entry can be read from Address Table Data 4 Register (Reg2B5H.[12]). For IGMP membership table, IGMP valid signal and per-port aged timer can be read from Address Table Data 2~3 Register (Reg2B3H.[2:0], Reg2B4H.[5:0]).

- Entry Clear

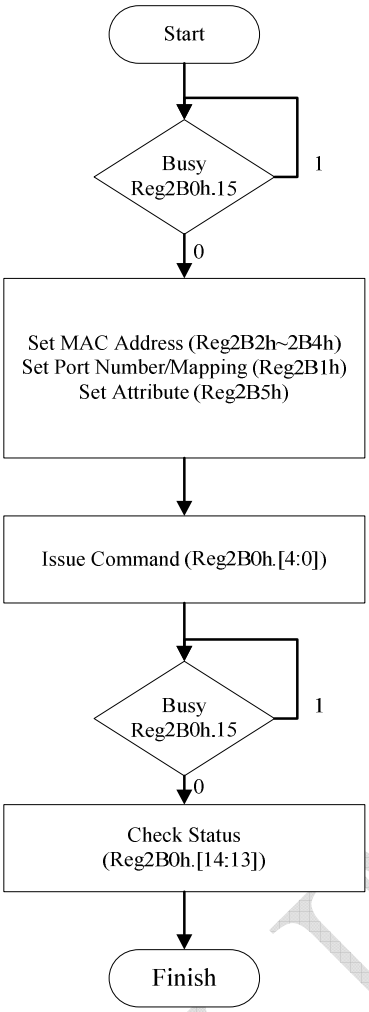
(1). Check the busy bit of Address Table Control & Status Register (Reg2B0H.15) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the "Clear" command and assign the target table to Address Table Control & Status Register (Reg2B0H.[4:0]) to start the operation.

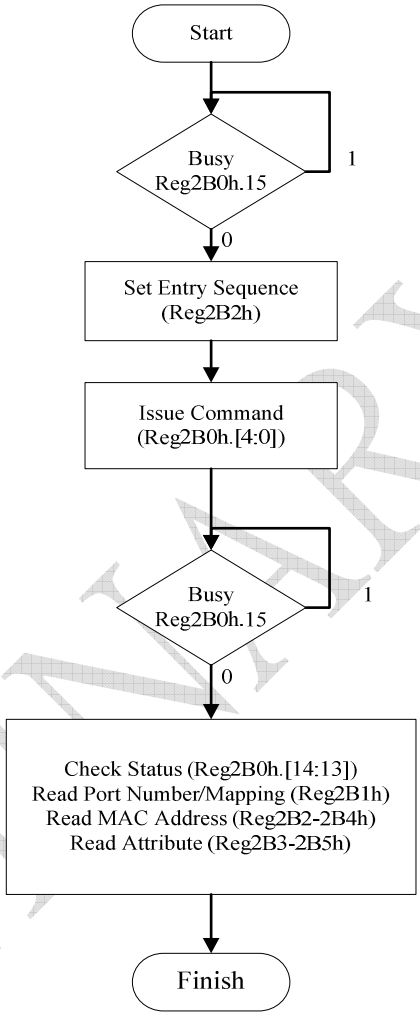
(3). Wait at least 4.5ms for clear procedure is done.

(4). Check the busy bit again, wait for available.

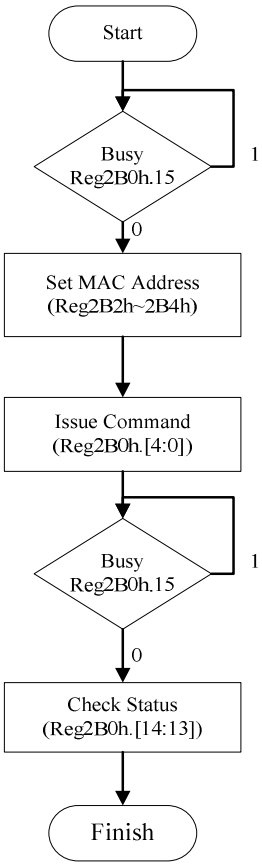
Entry Write



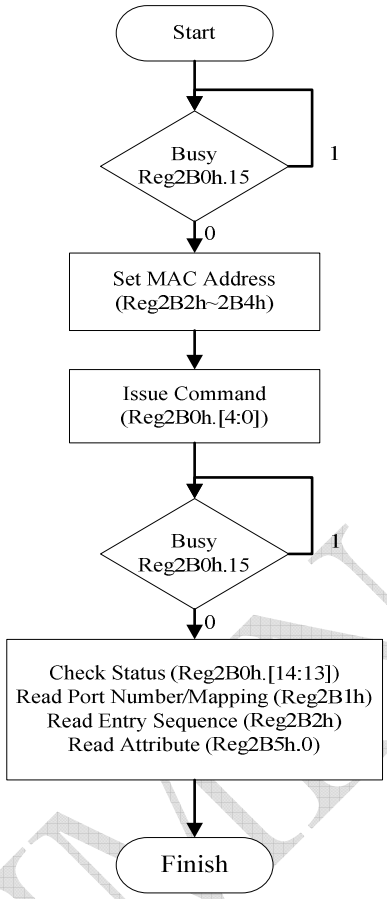
Entry Read



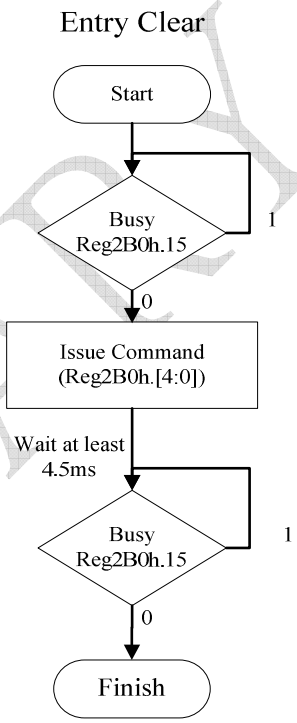
Entry Delete



Entry Search



Entry Clear



7.1.17 IGMP Snooping

The Internet Group Management Protocol (IGMP) is a communications protocol used to manage the membership of Internet Protocol multicast groups. IGMP is used by IP hosts and adjacent multicast routers to establish multicast group memberships. There are three versions of IGMP, as defined by "Request for Comments" (RFC) documents of the Internet Engineering Task Force (IETF). IGMP v1 is defined by RFC 1112, IGMP v2 is defined by RFC 2236 and IGMP v3 is defined by RFC 3376.
IGMP snooping is a feature that allows the switch to "listen in" on the IGMP protocol conversation between hosts and routers. The IGMP snooping switch hears an IGMP report from a host with a given multicast group address. It adds the host's port number to the multicast list for that group, and when the switch hears an IGMP Leave, it removes the host's port from the table entry. Finally, switch will only forward multicast traffic to the hosts interested in that traffic. Therefore, this function can effectively reduce multicast traffic.

◆ **Hardware-Based IGMP Snooping**

The DM8806 supports IGMP v1/v2 snooping and the maximal group is 32 without any software effort in this mode. The DM8806 automatically manipulates and updates IGMP membership table and Multicast table according to IGMP control packets, such as membership report and leave.
If IGMP membership table is full, the later incoming IGMP Membership Report (Join) packet will be ignored and the group address won't be registered into multicast address table. After that, the unregistered IP multicast packets (the destination MAC address can not be found in the multicast address table) will be treated as normal multicast packets by default. The additional forwarding control method can see the register Reg29BH.[3:2].
The DM8806 supports router ports auto-detect and auto-aging mechanism. The port which receives IGMP Query packets will be treated as router port by default. The router port also can be define as static one by user (see Reg29BH.7) and the port map of the router port can be programmed at Reg29BH.[10:8]. Keep in mind that the CPU port is never treated as router port. The DM8806 leaves the router port if the time (Router Present Timeout, 400sec by default) is expired that the port never receives IGMP Query during this period.
If receiving V1REPORT or V2REPORT (group join), DM8806 creates new or updates the entry. If receiving LEAVE, DM8806 deletes the entry directly when Fast Leave is enabled, or waiting until timeout.
DM8806 removes the entry that was never updated after the timer of host timeout (Group Membership Interval) is expired. This timer is programmable in DM8806 and defined by RFC 2236 as ((the Robustness Variable) times (the Query Interval)) plus (one Query Response Interval). The setting of the Robustness Variable and the Query Interval can see Reg29CH.

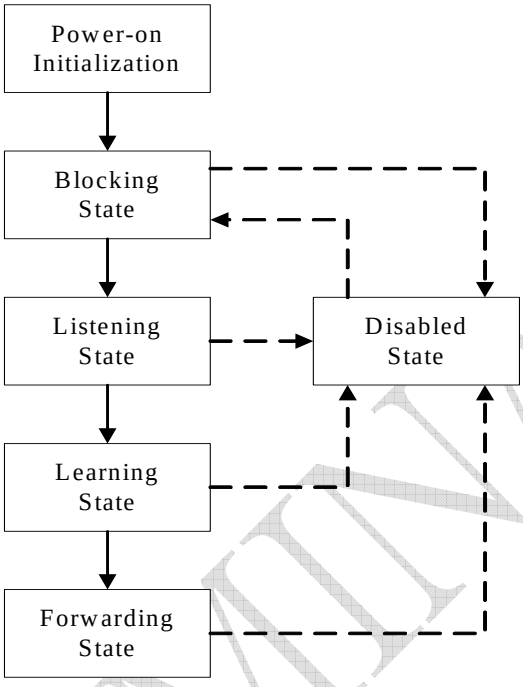
7.1.18 IPv6 MLD Snooping

The DM8806 forwards the IPv6 Multicast Listener Discovery (MLD) packets to the processor port when MLD Snooping is enabled and the MLD packets meet following scenario:

(1). IPv6 Multicast packets.
(2). The Hop Limit in IPv6 header is 1.
(3). The Next Header in IPv6 header is 0x3A (ICMPv6) or 0x00 (and next header of hop-by-hop option header is 0x3A).
(4). The Type in ICMP header is 0x82 (Multicast Listener Query), 0x83 (Multicast Listener Report) or 0x84 (Multicast Listener Done).

7.1.19 STP / RSTP Support

DM8806 supports both Spanning Tree Protocol(STP) and Rapid Spanning Tree Protocol(RSTP). There are five types of STP Port State (Disabled, Blocking, Listening, Learning and Forwarding state) and three types of RSTP Port State (Discarding, Learning and Forwarding) for these two protocols. The following figure is the port state diagram of STP.



But in RSTP, there are only three port states. The port states comparison between STP and RSTP are listed as below.

STP Port State	RSTP Port State
Disabled	Discarding
Blocking	Discarding
Listening	Discarding
Learning	Learning
Forwarding	Forwarding

For compatibility and design consideration, this function needs the cooperation with external CPU. Moreover, the behavior of Disabled/Blocking/Listening states in STP must be equal to the behavior of Discarding state in RSTP in DM8806. The difference between STP and RSTP should be implemented by CPU. The following statement describes the STP/RSTP port state behavior and software action in DM8806.

◆ **Disable State:**
(1). Drop all packets including BPDUs
→ Implemented by transmitting BPDUs to CPU and CPU drops BPDUs.
(2). Learning is disabled.
(3). Does not transmit BPDUs received from CPU
→ Implemented by CPU does not send BPDUs to this port

◆ **Blocking State:**
(1). Drop all packets except BPDUs and transmit received BPDUs to CPU.
(2). Learning is disabled.
(3). Does not transmit BPDUs received from CPU

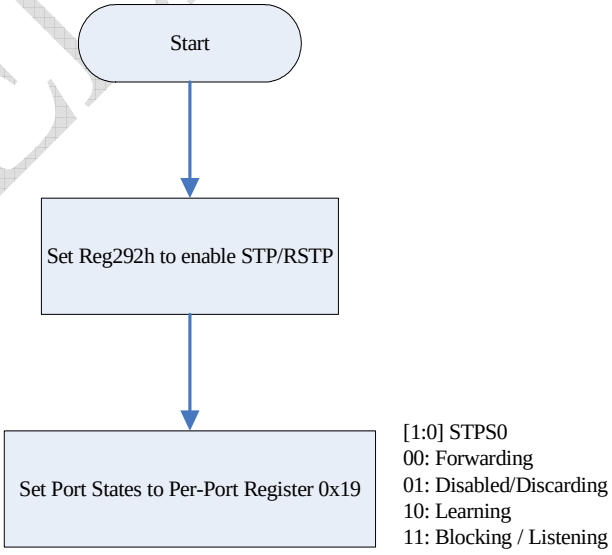
◆ **Listening State:**
(1). Drop all packets except BPDUs and tranmit received BPDUs to CPU
(2). Learning is disabled.
(3). Forward BPDUs received from CPU
→ Implemented by CPU uses special tag function to send BPDUs to decided port

◆ **Learning State:**
(1). Drop all packets except BPDUs and transmit received BPDUs to CPU
(2). Learning is enabled
(3). Forward BPDUs received from CPU

◆ **Forwarding State:**
(1). Forward all packets
(2). Learning is enabled
(3). Forward BPDUs received from CPU

Base on the behavior of different states described above, DM8806 has a port states setting for both STP and RSTP in per-port register 19h, . The register setting is：
00： Forwarding
01： Disabled / Discarding
10： Learning
11： Blocking / Listening

The following flow diagram shows how to configure STP/RSTP function.



STP/RSTP Setting

7.1.20 Port Trunking Description

The DM8806/DM8806I supports one group trunk port which includes four 10/100Mbp ports. User can configure two or more ports as trunking group between Port0 and Port3. For setting details, please refer to bit 11~8 of REG 212h. The DM8806/DM8806I trunk function support load balancing and fault auto recovery, the next paragraph is detail description.

First, when balancing traffic, network administrators often wish to avoid reordering Ethernet frames. The load balancing behavior is achieved by DA and SA L2 hash algorithm to ensure that the same flow is always sent via the same physical link. Second, port failure recovery function on trunking can change the path from the unlinked port to other in trunk group automatically and recover the path if the port is re-linked.

7.2 Internal PHY Functions

7.2.1 100Base-TX Operation

The transmitter section contains the following functional blocks:
- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

◆ **4B5B Encoder**

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

◆ **Scrambler**

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

◆ **Parallel to Serial Converter**

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

◆ **NRZ to NRZI Encoder**

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

◆ **MLT-3 Converter**

The MLT-3 conversion is accomplished by converting the data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic one event.

◆ **MLT-3 Driver**

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

◆ **4B5B Code Group**

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

7.2.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.
The receive section contains the following functional blocks:
- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

◆ **Signal Detect**

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

◆ **Adaptive Equalization**

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

◆ **MLT-3 to NRZI Decoder**

The DM8806 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

◆ **Clock Recovery Module**

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

◆ **NRZI to NRZ**

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

◆ **Serial to Parallel**

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

◆ **Descrambler**

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

◆ **Code Group Alignment**

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

◆ **4B5B Decoder**

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).
The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

7.2.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM8806 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

7.2.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

7.2.5 Carrier Sense

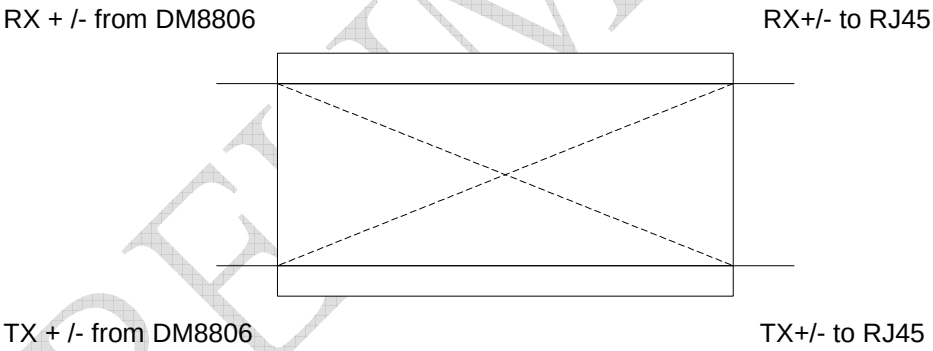
Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only when receiving operations.

7.2.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

7.2.7 Auto-MDIX Functional Description

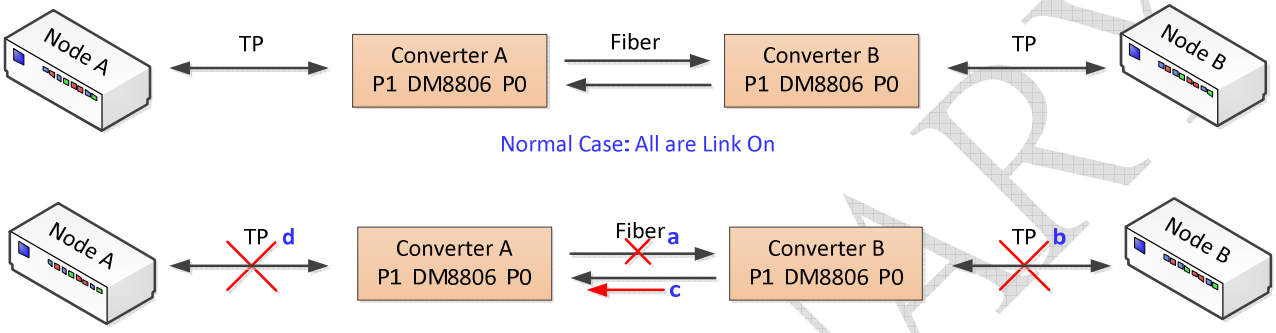
The DM8806 supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over) for internal port 0 ~ 4 PHY. A manual configuration by register bit for MDI or MDIX is still accepted. When set to automatic, the polarity of MDI/MDIX controlled timing is generated by a 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX, this feature is able to detect the required cable connection type.(straight through or crossed over) and make correction automatically.



* MDI : _____
* MDIX : - - - - - - - - -

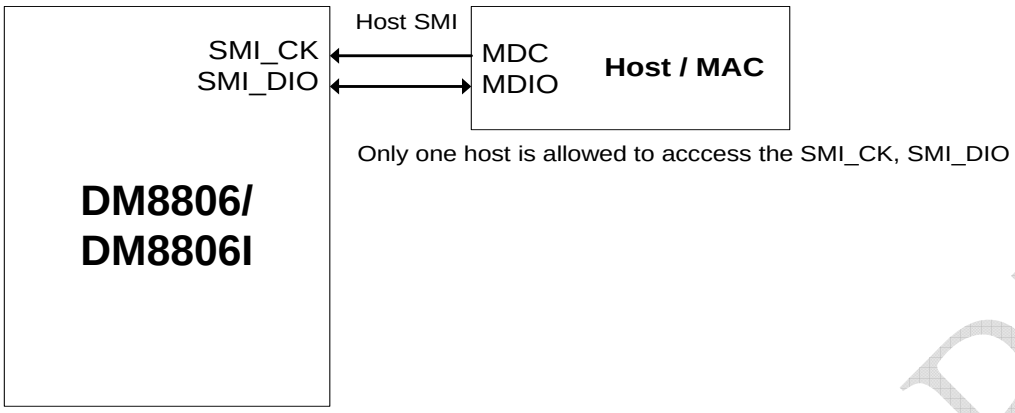
7.2.8 Link Fault Pass-through and Far End Fault Functional Description

The DM8806/DM8806I pairs Port 0 and Port 1 for media converter application and supports Link Fault Pass-through (LFP) and Far End Fault (FEF) troubleshooting features. The LFP allows the DM8806/DM8806I to monitor both the fiber and TP ports for loss of signal. In case of a loss of RX signal on one media port, the DM8806/DM8806I will automatically disable the TX signal to the other media port, thus passing through the link fault. FEF enables the DM8806/DM8806I to stop sending link pulse to the link partner once a loss of the fiber RX signal is encountered. Then the link partner will synchronously stop sending data. FEF prevents loss of valuable data transmitted over invalid link. Combining those two functions of DM8806/DM8806I, both end devices can be notified of a loss of fiber link



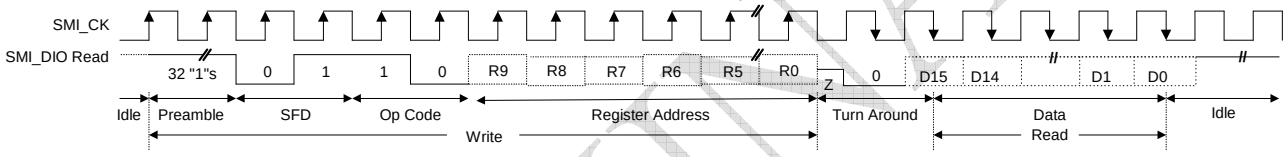
a. Converter B loss Fiber RX Link
b. Converter B disables TX TP via LFP to alert FEF Node B link loss
c. Converter B sends FEF signal back pin TX fiber to alert converter A of link loss
d. Converter A disables TX TP via LFP to alert near end Node A link loss

7.3 Host SMI Interface

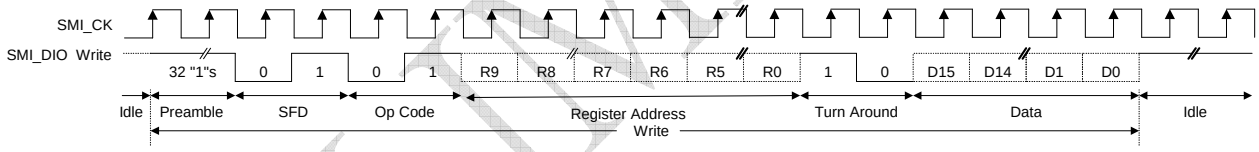


Only one host is allowed to acccess the SMI_CK, SMI_DIO

Host SMI - Read Frame Structure



Host SMI - Write Frame Structure



The internal registers of DM8806 can be accessed by Host Serial Management Interface (SMI). The application of SMI illustrated as below.
The Host SMI consists of two pins, one is SMI_CK and another is SMI_DIO. User can access DM8806's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI. The format is following. 32 bit "1" preamble field, "01" <SFD> field, <OpCode> field ("10" for read, ""01" for write), the <Register Address> field of the frame is mapped to address of control and status register set of DM8806, and the 16-bit <Data> field for read/writ data.

7.3.1 Host SMI Bus Error Check Function

To prevent the host SMI bus to be interfered by noise on board-level. This function is used to check the command validity to suppress the mistaken command. In write procedure, the written value in register will be applied until the correct checksum is written (error proofing) and user can read status for validation (error detecting). In read procedure, user can compare hardware calculated checksum with software calculated one to validate the result.

For example:

- Write Procedure
  (1). Set register 33AH.[0] = 1 to enable SMI Bus Error Check function
  (2). Write data to DM8806's register (general write command)
  (3). CPU calculate checksum (CSUM[7:0]) and write it to register 339H.[7:0]
  (4). Check function status in register 339H.[8]

- Read Procedure
  (1). Set register 33AH.[0] = 1 to enable SMI Bus Error Check function
  (2). Read data from DM8806's register (general read command)
  (3). Read hardware calculated checksum from register 339H.[7:0] and compare it with CPU calculated one (CSUM[7:0])

Checksum calculate formula:

CSUM[0] = D[0] ^ D[8] ^ R[0] ^ R[8]
CSUM[1] = D[1] ^ D[9] ^ R[1] ^ R[9]
CSUM[2] = D[2] ^ D[10] ^ R[2] ^ OP[0]
CSUM[3] = D[3] ^ D[11] ^ R[3] ^ OP[1]
CSUM[4] = D[4] ^ D[12] ^ R[4]
CSUM[5] = D[5] ^ D[13] ^ R[5]
CSUM[6] = D[6] ^ D[14] ^ R[6]
CSUM[7] = D[7] ^ D[15] ^ R[7]

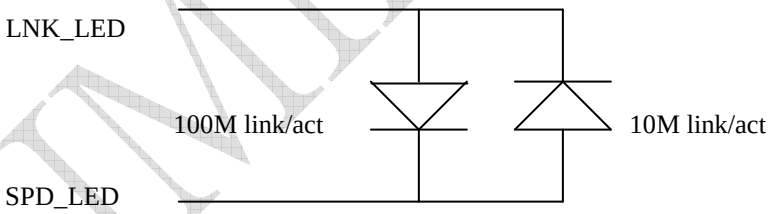
Note:

D[15:0] = <Data> field of SMI frame
R[9:0] = <Register Address> field of SMI frame
OP[1:0] = <Op Code> field of SMI frame

7.4 LED Mode Control

LED mode	
Bit [1:0] of register 317H	"00" : LED mode 0 "01" : LED mode 1, dual color mode "10" : LED mode 2 "11" : LED mode 3 (default)

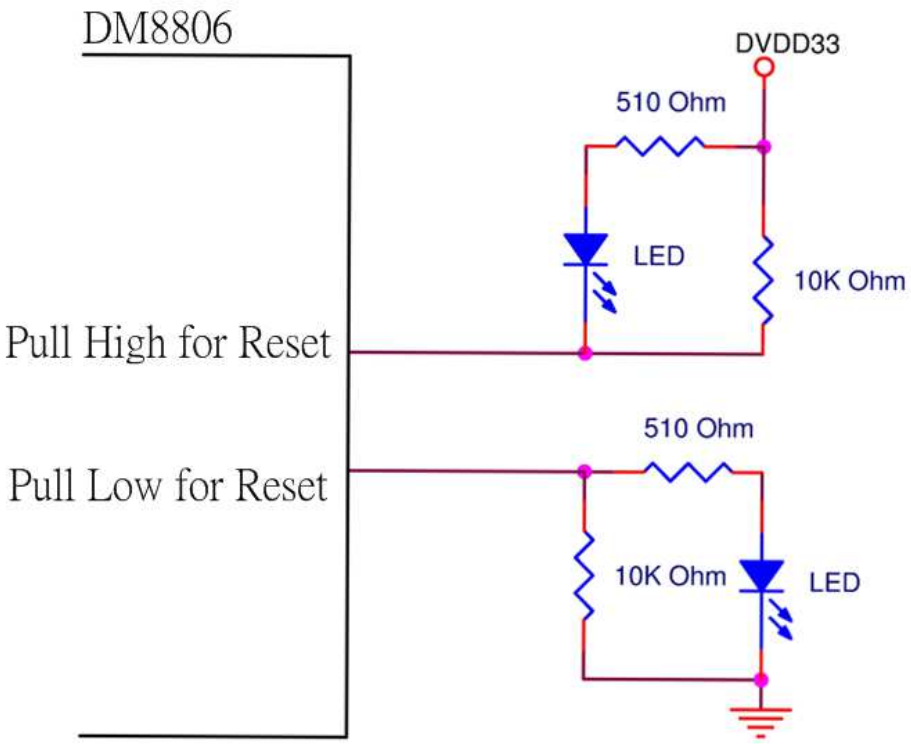
LED mode 0	
P0~4_LNK_LED	100M link + Activity OFF: 100M link fail ON : 100M link ok and no TX/RX activity BLINK: 100M link ok and TX/RX activity
P0~4_SPD_LED	Collision OFF: no collision BLINK: collision
P0~4_FDX_LED	10M link + Activity OFF: 10M link fail ON: 10M link ok and no TX/RX activity BLINK: 10M link ok and TX/RX activity

LED mode 1 (Dual color mode)			
P0~4_LNK_LED P0~4_SPD_LED	Application circuit :  		
		LNK_LED	SPD_LED
	link off	HI	HI
	100M link	HI	LO
	100M link / activity	BLINK	LO
	10M link	LO	HI
	10M link / activity	LO	BLINK
P0~4_FDX_LED	Full / half duplex mode OFF: half-duplex ON: full-duplex BLINK: half-duplex and collision		

LED mode 2	
P0~4_LNK_LED	100M link + Activity OFF: 100M link fail ON: 100M link ok and no TX/RX activity BLINK: 100M link ok and TX/RX activity
P0~4_SPD_LED	Full / half duplex mode OFF: half-duplex ON: full-duplex BLINK: half-duplex and collision
P0~4_FDX_LED	10M link + Activity OFF: 10M link fail ON: 10M link ok and no TX/RX activity BLINK: 10M link ok and TX/RX activity

LED mode 3 (Default)	
P0~4_LNK_LED	link + Activity OFF: link fail ON,: link ok and no TX/RX activity BLINK: link ok and TX/RX activity
P0~4_SPD_LED	Speed OFF: 10M mode or link OFF ON: 100M mode link
P0~4_FDX_LED	Full / half duplex mode OFF: half-duplex ON: full-duplex BLINK: half-duplex and collision

Where OFF means in floating state
ON means in ground state if LED is low active, or in high voltage state if LED is high active
BLINK means in toggle state with ON 20ms and OFF 80ms
HI means in high voltage state
LO means in ground state


DM8806
DVDD33
510 Ohm
LED
10K Ohm
Pull High for Reset
510 Ohm
Pull Low for Reset
10K Ohm
LED

8. DC and AC Electrical Characteristics

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD33	3.3V Supply Voltage	3.135	3.6	V	
DVDD18	1.8V core power supply	1.71	1.95	V	
AVDD33	Analog power supply 3.3V	3.135	3.6	V	
AVDD18	Analog power supply 1.8V	1.71	1.95	V	
V_{IN}	DC Input Voltage (VIN)	3.135	3.6	V	
T_{STG}	Storage Temperature range	-65	+150	°C	
T_A	Ambient Temperature	0	+70	°C	DM8806
T_A	Ambient Temperature	-40	+85	°C	DM8806I
L_T	Lead Temperature (TL, soldering, 10 sec.).	-	+245	°C	Lead-free Device

8.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD33	3.3V Supply Voltage	3.135	3.30	3.465	V	
DVDD18	1.8V core power supply	1.71	1.80	1.89	V	
AVDD33	Analog power supply 3.3V	3.135	3.30	3.465	V	
AVDD18	Analog power supply 1.8V	1.71	1.80	1.89	V	
P_D (Power Dissipation)	5 ports 100BASE-TX	-	471	-	mA	1.8V only
		-	243	-	mA	3.3V only
	5 ports10BASE-TX		549		mA	1.8V only
			66		mA	3.3V only

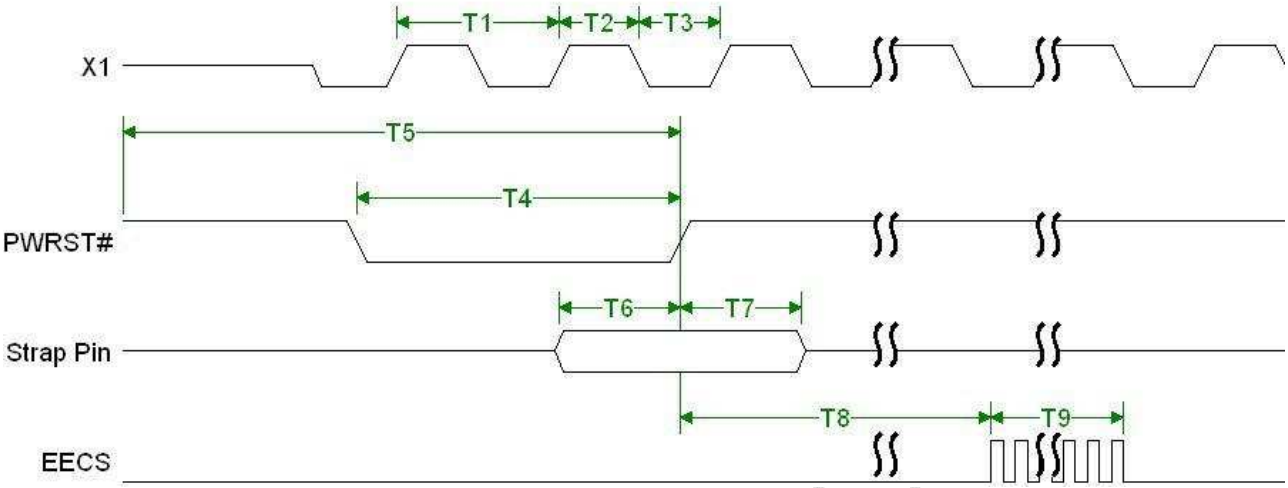
8.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

Note: Vcond1 = DVDD33 = 3.3V, DVDD18 = 1.8V, AVDD33 = 3.3V, AVDD18 = 1.8V.

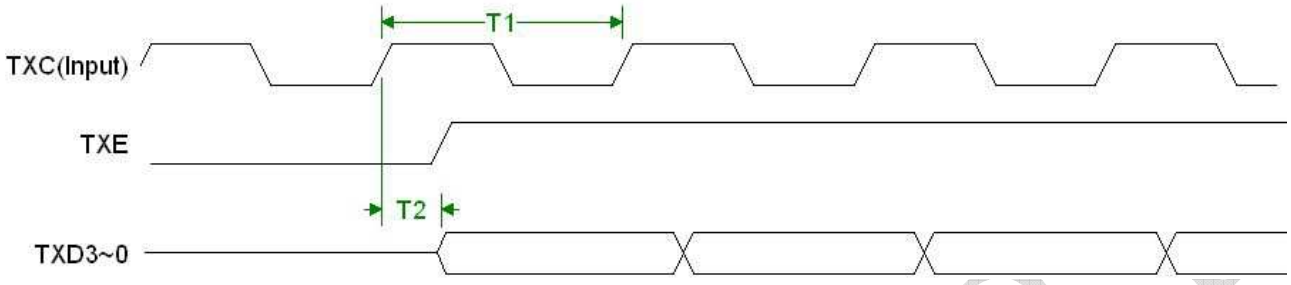
8.4 AC Characteristics

8.4.1 Power On Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	X1 Period	39.995	40	40.005	ns	-
T2	X1 High Time	18	-	22	ns	-
T3	X1 Low Time	18	-	22	ns	
T4	Reset Low Duration	1	-	-	ms	
T5	Power On Reset Duration	10	-	-	ms	
T6	Strap Valid Setup to PWRST# Rising	100	-	-	ns	
T7	Strap Valid Hold from PWRST# Rising	200	-	-	ns	
T8	PWRST# high to EECS high	-	5	-	us	
T9	EEPROM Load Duration	-	-	21	ms	

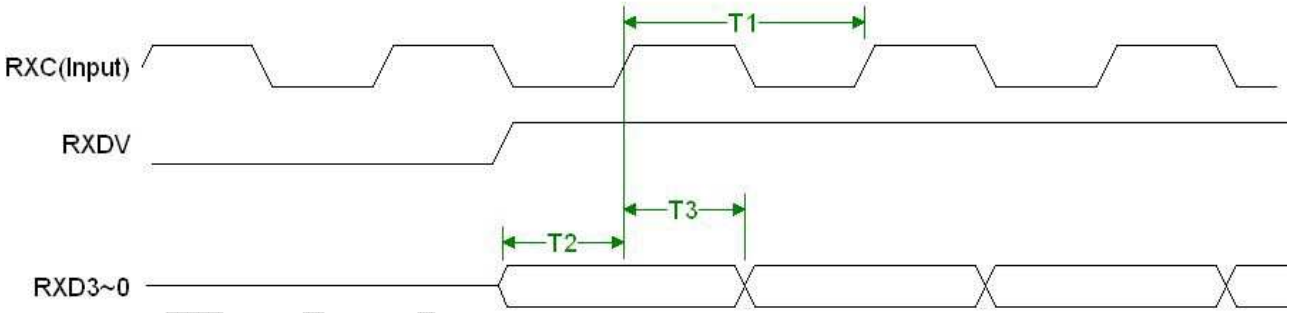
8.4.2 MAC MII/RevMII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Transmit Clock Period	-	40	-	ns
	10M MII Transmit Clock Period	-	400	-	ns
T2	TXE, TXD3~0 Output Delay to TXC Rising	4	8	12	ns

Note: TXC stand for pin P4M_TXC in port 4 and pin P5_TXC in port 5
TXE stand for pin P4M_TXE in port 4 and pin P5_TXE in port 5
TXD_3~0 stand for pin P4M_TXD3~0 in port 4 and pin P5_TXD3~0 in port 5

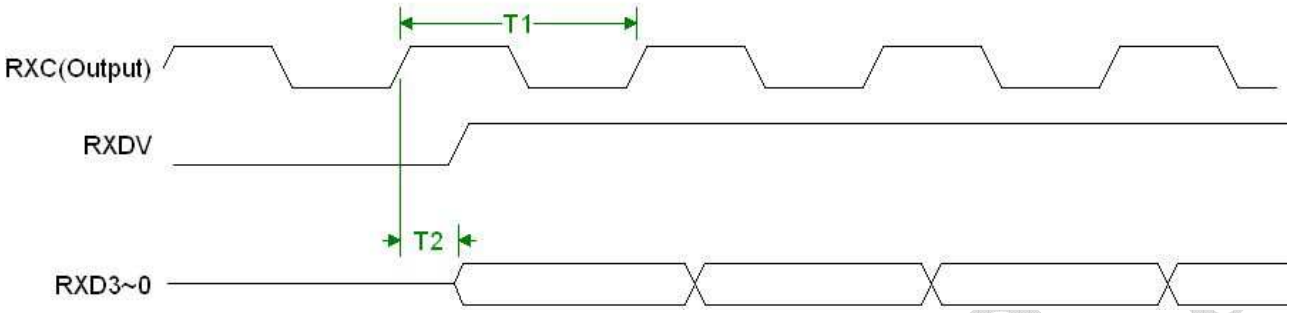
8.4.3 MAC MII/RevMII Interface Receive Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Receive Clock Period	-	40	-	ns
	10M MII Receive Clock Period	-	400	-	ns
T2	RXDV, RXD3~0 Setup Time to RXC	5	-	-	ns
T3	RXDV, RXD3~0 Hold Time to RXC	5	-	-	ns

Note: RXC stand for pin P4M_RXC in port 4 and pin P5_RXC in port 5
RXDV stand for pin P4M_RXDV in port 4 and pin P5_RXDV in port 5
RXD_3~0 stand for pin P4M_RXD3~0 in port 4 and pin P5_RXD3~0 in port 5

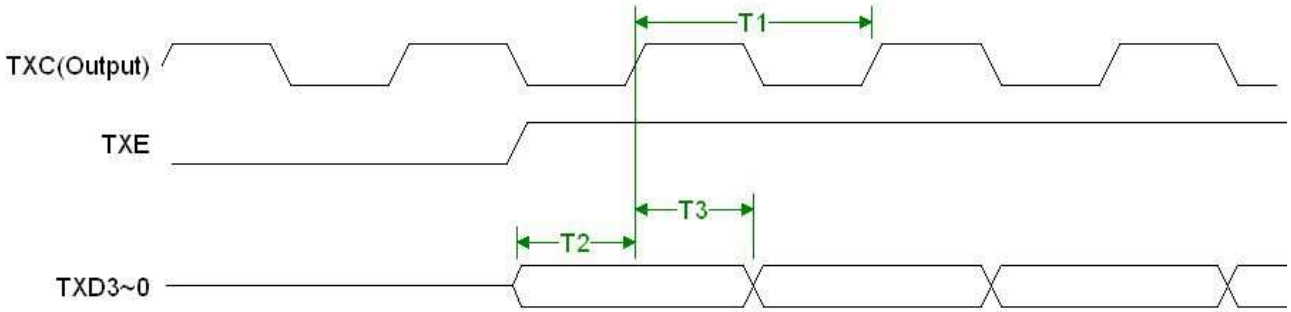
8.4.4 PHY MII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Receive Clock Period	-	40	-	ns
	10M MII Receive Clock Period	-	400	-	ns
T2	RXDV, RXD3~0 Output Delay to RXC Rising	4	8	12	ns

Note: RXC stand for pin P4P_RXC in port 4
RXDV stand for pin P4P_RXDV in port 4
RXD_3~0 stand for pin P4P_RXD3~0 in port 4

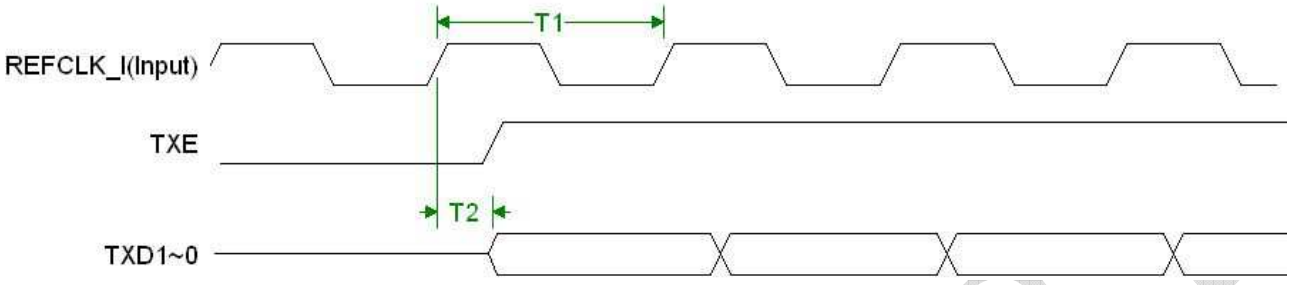
8.4.5 PHY MII Interface Receive Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Transmit Clock Period	-	40	-	ns
	10M MII Transmit Clock Period	-	400	-	ns
T2	TXE, TXD3~0 to TXC Setup Time	5	-	-	ns
T3	TXE, TXD3~0 to TXC Hold Time	5	-	-	ns

Note: TXC stand for pin P4P_TXC in port 4
TXE stand for pin P4P_TXE in port 4
TXD_3~0 stand for pin P4P_TXD3~0 in port 4

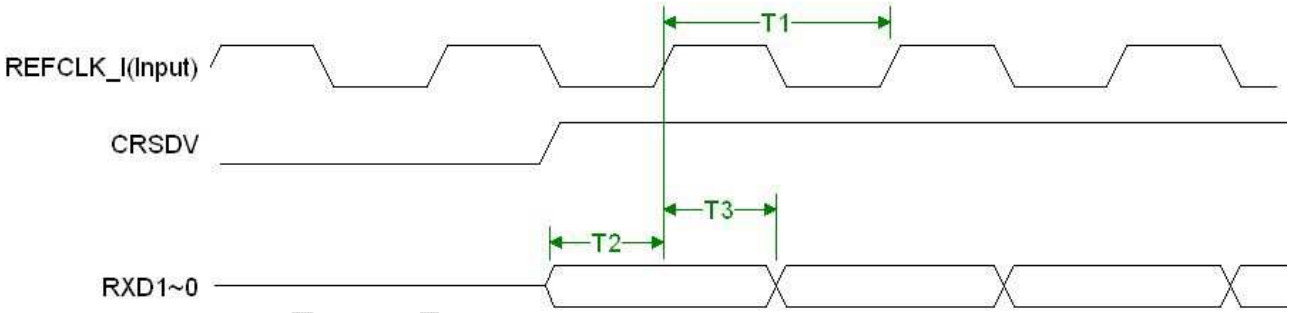
8.4.6 MAC RMII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMII REFCLK_I Period	-	20	-	ns
T2	TXE, TXD1~0 Output Delay to REFCLK_I Rising	4	8	12	ns

Note: REFCLK_I stand for pin P4M_ REFCLK_I in port 4 and pin P5_ REFCLK_I in port 5
TXE stand for pin P4M_TXE in port 4 and pin P5_TXE in port 5
TXD_1~0 stand for pin P4M_TXD1~0 in port 4 and pin P5_TXD1~0 in port 5

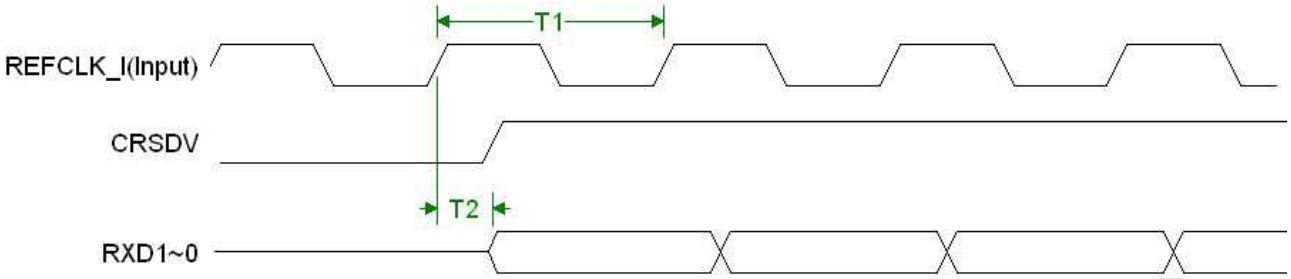
8.4.7 MAC RMII Interface Receive Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMII REFCLK_I Period	-	20	-	ns
T2	CRSDV, RXD1~0 Setup Time to REFCLK_I	4	-	-	ns
T3	CRSDV, RXD1~0 Hold Time to REFCLK_I	2	-	-	ns

Note: REFCLK_I stand for pin P4M_ REFCLK_I in port 4 and pin P5_ REFCLK_I in port 5
CRSDV stand for pin P4M_CRSDV in port 4 and pin P5_CRSDV in port 5
RXD_1~0 stand for pin P4M_RXD1~0 in port 4 and pin P5_RXD1~0 in port 5

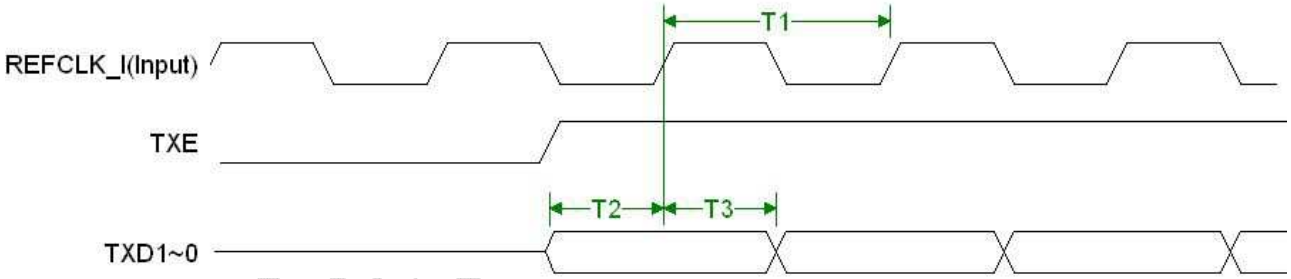
8.4.8 PHY RMII Interface Transmit Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMII REFCLK_I Period	-	20	-	ns
T2	CRSDV, RXD1~0 Output Delay to REFCLK_I Rising	4	8	12	ns

Note: REFCLK_I stand for pin P4P_ REFCLK_I in port 4
CRSDV stand for pin P4P_CRSDV in port 4
RXD_1~0 stand for pin P4P_RXD1~0 in port 4

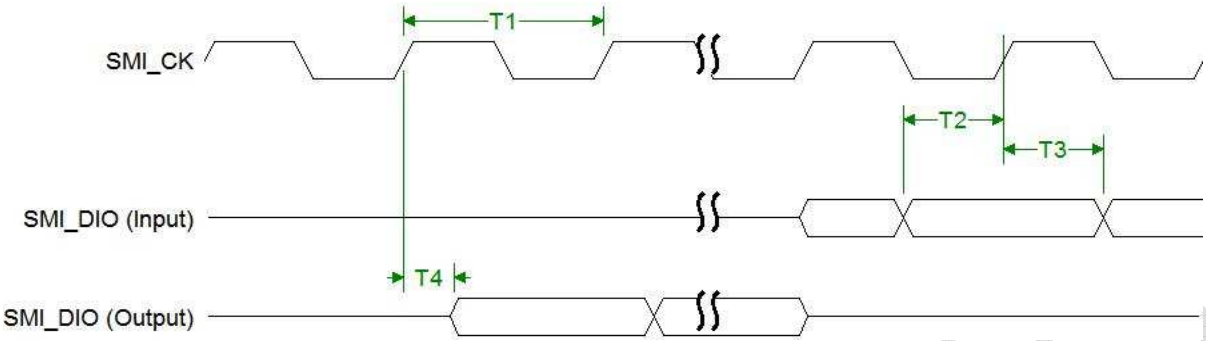
8.4.9 PHY RMII Interface Receive Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMII REFCLK_I Period	-	20	-	ns
T2	TXE, TXD1~0 Setup Time to REFCLK_I	4	-	-	ns
T3	TXE, TXD1~0 Hold Time to REFCLK_I	2	-	-	ns

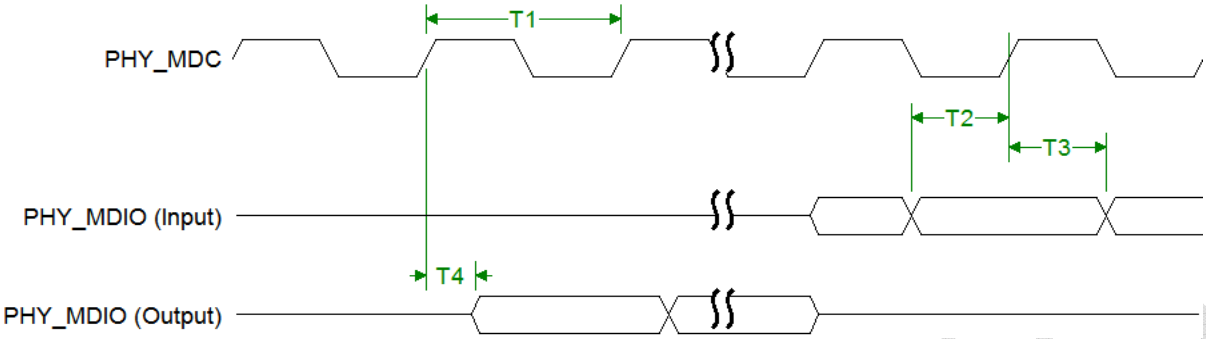
Note: REFCLK_I stand for pin P4P_ REFCLK_I in port 4
TXE stand for pin P4P_TXE in port 4
TXD_1~0 stand for pin P4P_TXD1~0 in port 4

8.4.10 Host SMI Interface Timing



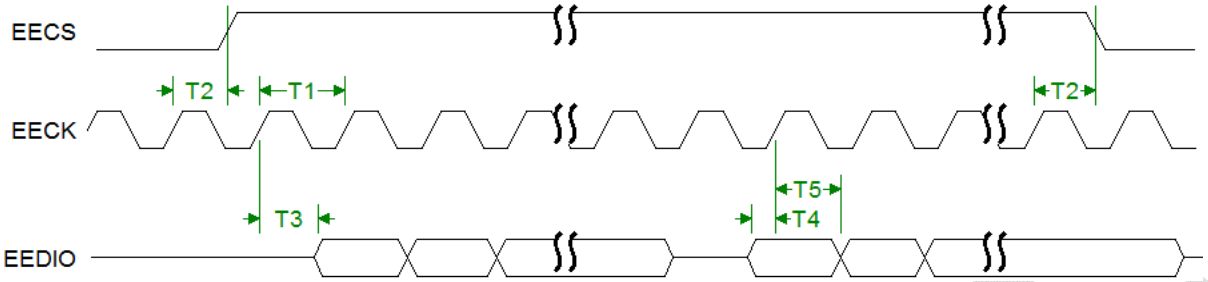
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SMI_CK Period	80	-	-	ns
T2	SMI_DIO to SMI_CK Setup Time on Input State	10	-	-	ns
T3	SMI_DIO to SMI_CK Hold Time on Input State	10	-	-	ns
T4	SMI_DIO to SMI_CK Rising Output Delay on Output State	-	5	-	ns

8.4.11 PHY SMI Interface Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	PHY_MDC Period	-	1920	-	ns
T2	PHY_MDIO to PHY_MDC Setup Time on Input State	40	-	-	ns
T3	PHY_MDIO to PHY_MDC Hold Time on Input State	40	-	-	ns
T4	PHY_MDIO to PHY_MDC Rising Output Delay on Output State	-	960	-	ns

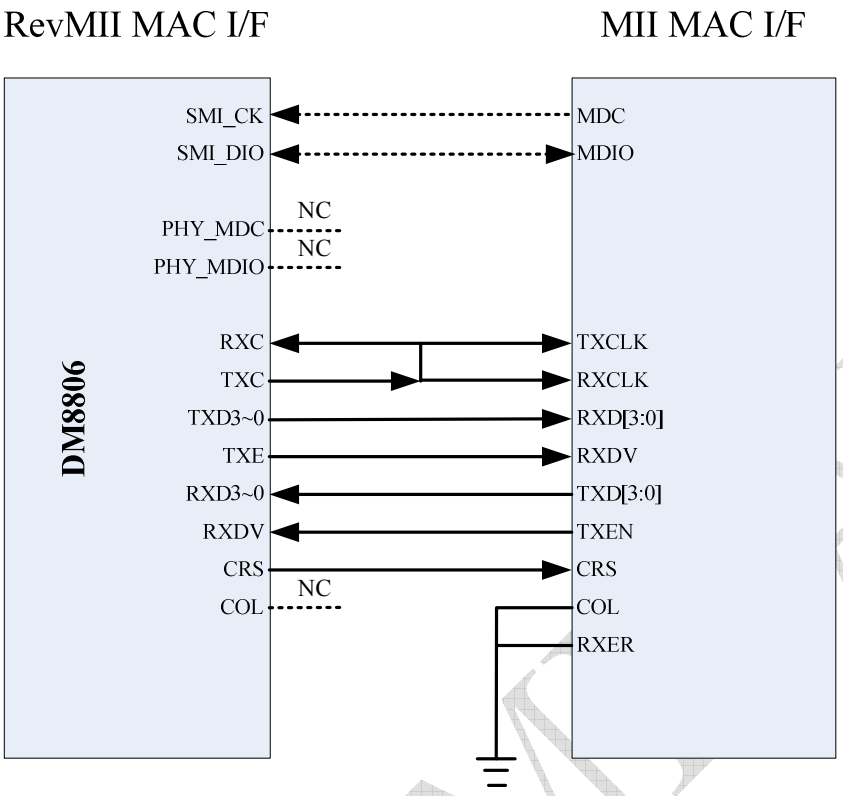
8.4.12 EEPROM Timing



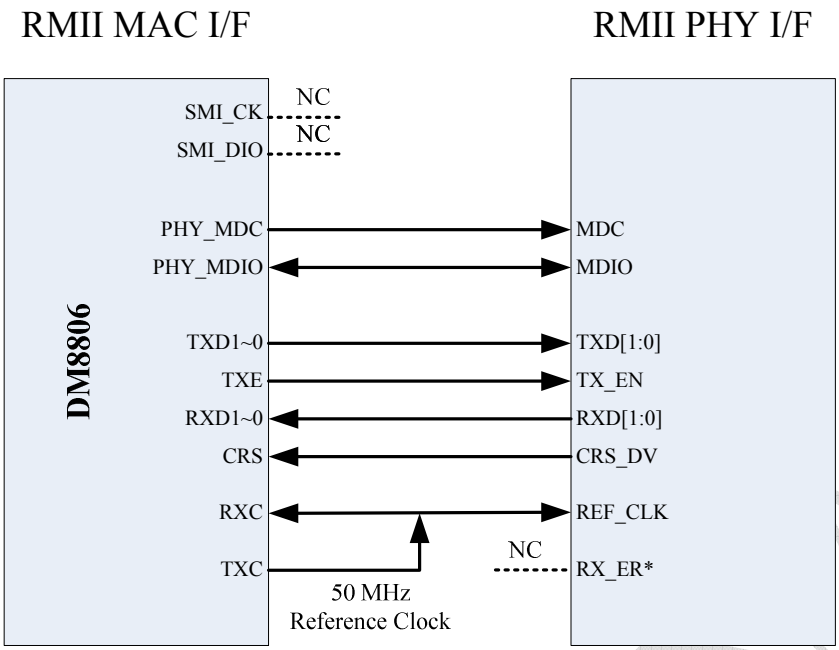
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECK Period	-	2560	-	ns
T2	EECS to EECK Rising Output Delay	-	2080	-	ns
T3	EEDIO to EECK Rising Output Delay on Output State	-	2100	-	ns
T4	EEDIO to EECK Rising Setup Time on Input State	200	-	-	ns
T5	EEDIO to EECK Rising Hold Time on Input State	200	-	-	ns

9. Application Information

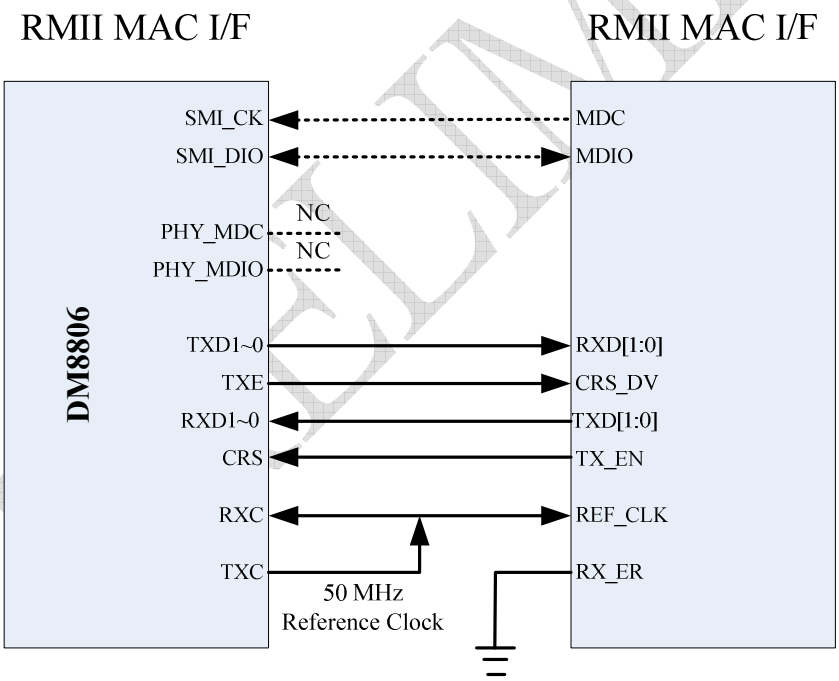
9.1 Application of Reverse MII



9.2 Application of Reduce MII to PHY

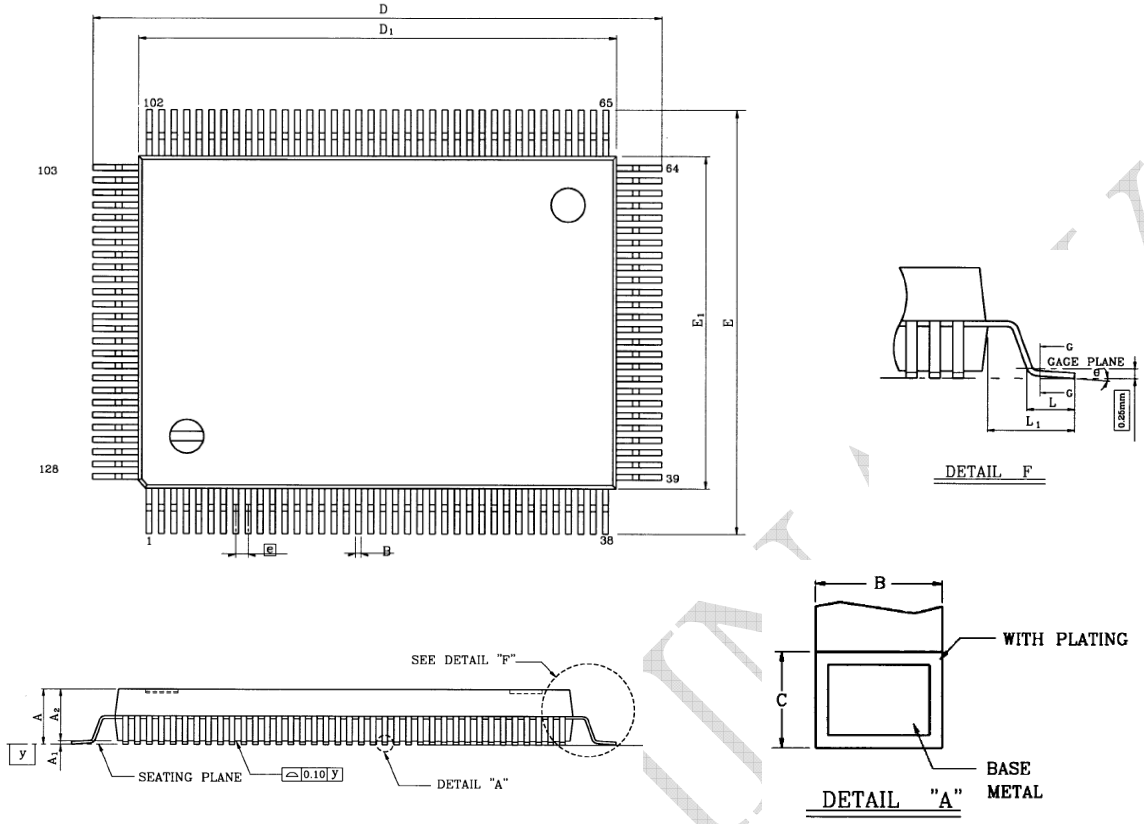


9.3 Application of Reduce MII to MAC



10. Package Information

128 Pins QFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	—	—	3.40		—	—	0.134
A_1	0.25	—	—		0.010	—	—
A_2	2.73	2.85	2.97		0.107	0.112	0.117
B	0.17	0.22	0.27		0.007	0.009	0.011
C	0.09	—	0.20		0.004	—	0.008
D	23.00	23.20	23.40		0.906	0.913	0.921
D_1	19.90	20.00	20.10		0.783	0.787	0.791
E	17.00	17.20	17.40		0.669	0.677	0.685
E_1	13.90	14.00	14.10		0.547	0.551	0.555
e	0.50 BSC				0.020 BSC		
L	0.73	0.88	1.03		0.029	0.035	0.041
L_1	1.60 BSC				0.063 BSC		
y	—	—	0.10		—	—	0.004
θ	0^o	—	7^o		0^o	—	7^o

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

11. Ordering Information

Part Number	Temperature Range	Package
DM8806FP	0℃ to 70℃	128-Pin QFP (Pb-Free)
DM8806IFP	−40℃ to +85℃	128-Pin QFP (Pb-Free)

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6 Li-Hsin Rd. VI,
Science-based Industrial Park,
Hsin-chu City, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.