Line Drivers /Receivers

DM7838/DM8838 quad unified bus transceiver

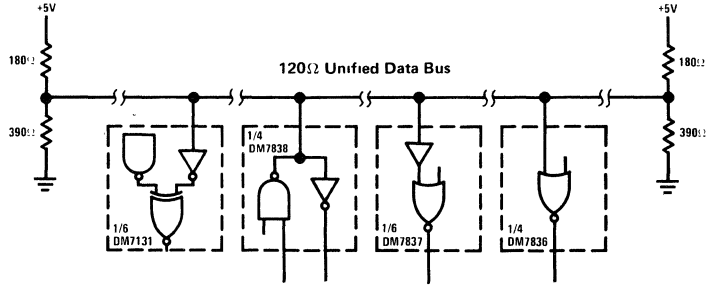
general description

The DM7838/DM8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times $\leq 10\mu s$.

features

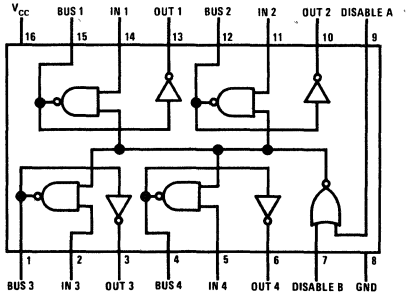
- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

typical application



connection diagram

Dual In-Line and Flat Package



TOP VIEW

Order Number DM7838J or DM8838J
See Package 17

Order Number DM7838W or DM8838W
See Package 28

Order Number DM8838N
See Package 23

absolute maximum ratings

Supply Voltage	7V	Operating Temperature Range	
Input and Output Voltage	5 5V	DM7838	−55 C to +125 C
Power Dissipation	600 mW	DM8838	0 C to +70 C
		Storage Temperature Range	−65 C to +150 C
		Lead Temperature (Soldering, 10 sec)	300 C

electrical characteristics

DM7838/DM8838 The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$ unless otherwise specified (Note 2)

PARAMETER	DISABLE INPUT	DRIVER INPUT	BUS PIN	RECEIVER OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
Logic "1" Input Voltage Disable	V_{IN}	2V	4V		Bus < 100 μA	2 0			V
Logic "0" Input Voltage Disable	V_{IN}	2V	50 mA		Bus < 0 7V			0 8	V
Logic "1" Input Voltage Driver	0 8V	V_{IN}	50 mA		Bus < 0 7V	2 0			V
Logic "0" Input Voltage Driver	0 8V	V_{IN}	4V		Bus < 100 μA			0 8	V
High Level Receiver Threshold DM7838		0 8V	V_{TH}	16 mA	Receiver output < 0 4V	1 65	2 25	2 65	V
High Level Receiver Threshold DM8838		0 8V	V_{TH}	16 mA	Receiver output < 0 4V	1 80	2 25	2 50	V
Low Level Receiver Threshold DM7838		0 8V	V_{TH}	−400 μA	Receiver output > 2 4V	0 97	1 30	1 63	V
Low Level Receiver Threshold DM8838		0 8V	V_{TH}	−400 μA	Receiver output > 2 4V	1 05	1 30	1 55	V
Logic "1" Input Current Disable and Driver	5 5V	5 5V						1	mA
Logic "1" Input Current Disable and Driver	2 4V	2 4V						40	μA
Logic "0" Input Current Disable and Driver	0 4V	0 4V						−1 6	mA
Maximum Bus Current	0 8V	0 8V	4V		$V_{CC} = V_H$		20	100	μA
Maximum Bus Current	0 8V	0 8V	4V		$V_{CC} = 0V$		2	100	μA
Low Level Bus Voltage	0 8V	2V	50 mA				0 4	0 7	V
Logic "1" Output Voltage Receiver	0 8V	0 8V	0 5V	−400 μA		2 4			V
Logic "0" Output Voltage Receiver	0 8V	0 8V	4V	16 mA			0 25	0 4	V
Output Short Circuit Current Receiver	0 8V	0 8V	0 5V	0V	$V_{CC} = V_H$	−18		−55	mA
Supply Current	0V	2V			Per Package		50	70	mA
Input Diode Clamp Voltage	−12 mA	−12 mA	−12 mA		$T_A = 25°C$		−1	−1 5	V
The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified									
Propagation Delays									
Disable to Bus "1"					Note 3		19	30	ns
Disable to Bus "0"					Note 3		15	23	ns
Driver Input to Bus "1"					Note 3		17	25	ns
Driver Input to Bus "0"					Note 3		9	15	ns
Bus to Logic "1" Receiver Output					Note 4		20	30	ns
Bus to Logic "0" Receiver Output					Note 5		18	30	ns

Note 1: Voltage values are with respect to network ground terminal Positive current is defined as current into the referenced pin.

Note 2: For DM7838. $V_L = 4.5V$, $V_H = 5.5V$, $T_L = -55°C$, $T_H = +125°C$
For DM8838. $V_L = 4.75V$, $V_H = 5.25V$, $T_L = 0°C$, $T_H = +70°C$

Note 3: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 4: Fan-out of 10 load, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1\ 5V$, $V_{IN} = 0V$ to 3.0V pulse

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1\ 5V$, $V_{IN} = 0V$ to 3 0V pulse.