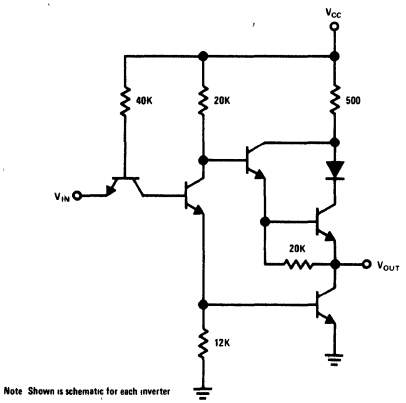
Level Translators/Buffers

DM88L12 TTL-MOS hex inverter/ interface gate

general description

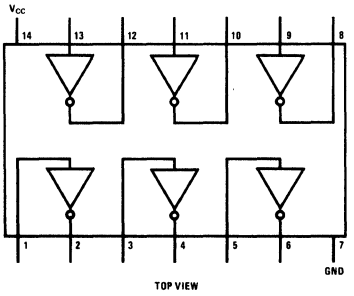
The DM88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} – 2.2V with an output current of –200 μA.

schematic and connection diagrams



Note Shown is schematic for each inverter

Dual-In-Line and Flat Package

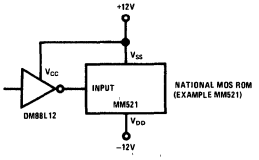


TOP VIEW

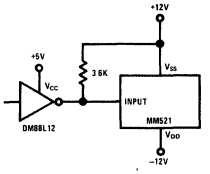
Order Number DM88L12F
See Package 4
Order Number DM88L12J
See Package 16
Order Number DM88L12N
See Package 22

typical applications

TTL Interface to MOS ROM Without Resistive Pull-Up



TTL Interface to MOS ROM With Resistive Pull-Up



ac test circuits

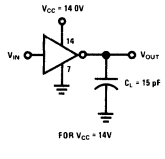


Figure 1

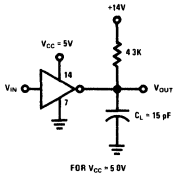
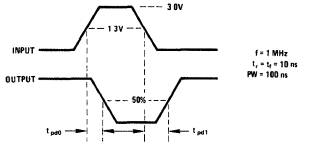


Figure 2

switching time waveforms



absolute maximum ratings (Note 1)

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage.	15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM78L12	4.5	5.5	V
DM88L12	4.75	5.25	V
Temperature			
DM78L12	−55	125	°C
DM88L12	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 14.0V			2.0	1.3		V
	V_{CC} = Min			2.0	1.3		V
Logical "0" Input Voltage	V_{CC} = 14.0V				1 3	0 7	V
	V_{CC} = Min				1.3	0.7	V
Logical "1" Output Voltage	V_{CC} = 14 0V	V_{IN} = 0.7V	I_{OUT} = −200 μA	11 8	12.0		V
	V_{CC} = Min	V_{IN} = 0.7V	I_{OUT} = +200 μA	14 5	15.0		V
	V_{CC} = Min	V_{IN} = 0V	I_{OUT} = −5.0μA	V_{CC} = 1.1V			V
Logical "0" Output Voltage	V_{CC} = 14.0V	V_{IN} = 2.0V	I_{OUT} = 12 mA		0.5	1.0	V
	V_{CC} = Min	V_{IN} = 2.0V	I_{OUT} = 3.6 mA		0.2	0.4	V
Logical "1" Input Current	V_{CC} = 14 0V	V_{IN} = 2.4V			<1	20	μA
	V_{CC} = Max	V_{IN} = 2.4V			<1	10	μA
	V_{CC} = 14.0V	V_{IN} = 5.5V			<1	100	μA
	V_{CC} = Max	V_{IN} = 5.5V			<1	100	μA
Logical "0" Input Current	V_{CC} = 14.0V	V_{IN} = 0.4V			−320	−500	μA
	V_{CC} = Max	V_{IN} = 0.4V			−100	−180	μA
Output Short Circuit Current (Note 3)	V_{CC} = 14.0V	V_{OUT} = 0V		−10	−25	−50	mA
	V_{CC} = Max	V_{OUT} = 0V		−3	−8	−15	mA
Supply Current — Logical "1" (Each Inverter)	V_{CC} = 14.0V	V_{IN} = 0V			0.32	0 50	mA
	V_{CC} = Max	V_{IN} = 0V			0.11	0.16	mA
Logical "0"	V_{CC} = 14.0V	V_{IN} = 5.25V			1 0	1 5	mA
	V_{CC} = Max	V_{IN} = 5.25V			0.3	0.5	mA
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	See Figure 2			27	45	ns
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 14.0V, T_A = 25°C	See Figure 1			11	20	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1} (Note 4)	V_{CC} = 5.0V, T_A = 25°C	See Figure 2			79	100	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1}	V_{CC} = 14.0V, T_A = 25°C	See Figure 1			34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78L12 and across the 0°C to +70°C range for the DM88L12. All typicals are given for V_{CC} = 5.0V and T_A = 25°C, or for V_{CC} = 14.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Note 4: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.