



DM9000A

Ethernet Controller with General Processor Interface

DAVICOM Semiconductor, Inc.

DM9000A

Ethernet Controller
with General Processor Interface

DATA SHEET

Preliminary

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Content

| | |
|---|----|
| 1. General Description | 6 |
| 2. Block Diagram | 6 |
| 3. Feature | 7 |
| 4. Pin Configuration | 8 |
| 4.1 Pin Configuration I: 16-bit mode..... | 8 |
| 4.2 Pin Configuration II: 8-bit mode..... | 9 |
| 5. Pin Description | 10 |
| 5.1 Processor Interface..... | 10 |
| 5.1.1 8-bit mode | 10 |
| 5.2 EEPROM Interface..... | 11 |
| 5.3 Clock Interface..... | 11 |
| 5.4 LED Interface..... | 11 |
| 5.5 10/100 PHY/Fiber..... | 11 |
| 5.6 Miscellaneous..... | 12 |
| 5.7 Power Pins..... | 12 |
| 5.8 strap pins table | 12 |
| 6. Vendor Control and Status Register Set | 13 |
| 6.1 Network Control Register (00H)..... | 14 |
| 6.2 Network Status Register (01H)..... | 15 |
| 6.3 TX Control Register (02H)..... | 15 |
| 6.4 TX Status Register I (03H) for packet index I..... | 15 |
| 6.5 TX Status Register II (04H) for packet index I I..... | 16 |
| 6.6 RX Control Register (05H)..... | 16 |
| 6.7 RX Status Register (06H)..... | 16 |



| | |
|--|----|
| 6.8 Receive Overflow Counter Register (07H)..... | 17 |
| 6.9 Back Pressure Threshold Register (08H)..... | 17 |
| 6.10 Flow Control Threshold Register (09H)..... | 17 |
| 6.11 RX/TX Flow Control Register (0AH)..... | 18 |
| 6.12 EEPROM & PHY Control Register (0BH)..... | 18 |
| 6.13 EEPROM & PHY Address Register (0CH)..... | 18 |
| 6.14 EEPROM & PHY Data Register (0DH~0EH) | 18 |
| 6.15 Wake Up Control Register (0FH)..... | 19 |
| 6.16 Physical Address Register (10H~15H)..... | 19 |
| 6.17 Multicast Address Register (16H~1DH) | 19 |
| 6.18 General purpose control Register (1EH)..... | 19 |
| 6.19 General purpose Register (1FH)..... | 20 |
| 6.20 TX SRAM Read Pointer Address Register (22H~23H)..... | 20 |
| 6.21 RX SRAM Write Pointer Address Register (24H~25H)..... | 20 |
| 6.22 Vendor ID Register (28H~29H)..... | 20 |
| 6.23 Product ID Register (2AH~2BH)..... | 20 |
| 6.24 Chip Revision Register (2CH)..... | 20 |
| 6.25 Transmit Control Register 2 (2DH) | 20 |
| 6.26 Operation Test Control Register (2EH)..... | 21 |
| 6.27 Special Mode Control Register (2FH)..... | 21 |
| 6.28 Early Transmit Control/Status Register (30H)..... | 22 |
| 6.29 Check Sum Control Register (31H)..... | 22 |
| 6.30 Receive Check Sum Control Status Register (32H)..... | 22 |
| 6.31 Memory Data Pre-Fetch Read Command without Address Increment (F0H)..... | 23 |
| 6.32 Memory Data Read Command without Address Increment Register (F1H)..... | 23 |
| 6.33 Memory Data Read Command with Address Increment Register (F2H) | 23 |
| 6.34 Memory Data Read_address Register (F4H~F5H)..... | 23 |
| 6.35 Memory Data Write Command without Address Increment Register (F6H)..... | 23 |
| 6.36 Memory data write command with address increment Register (F8H)..... | 23 |
| 6.37 Memory data write_address Register (FAH~FBH)..... | 23 |
| 6.38 TX Packet Length Register (FCH~FDH)..... | 23 |
| 6.39 Interrupt Status Register (FEH)..... | 24 |
| 6.40 Interrupt Mask Register (FFH)..... | 24 |



7. EEPROM Format.....25

8. PHY Register Description.....26

8.1 Basic Mode Control Register (BMCR) - 00.....27

8.2 Basic Mode Status Register (BMSR) - 01.....28

8.3 PHY ID Identifier Register #1 (PHYIDR1) - 02.....29

8.4 PHY ID Identifier Register #2 (PHYIDR2) - 03.....30

8.5 Auto-negotiation Advertisement Register (ANAR) - 04.....31

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) - 05.....32

8.7 Auto-negotiation Expansion Register (ANER)- 06.....33

8.8 DAVICOM Specified Configuration Register (DSCR) -16.....33

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) -1735

8.10 10Base-T Configuration / Status (10BTCSR) - 18.....36

8.11 Power Down Control Register (PWDOR) - 19.....37

8.12(Specified config) Register – 20.....37

9. Functional Description39

9.1 Host Interface.....39

9.2 Direct Memory Access Control39

9.3 Packet Transmission.....39

9.4 Packet Reception.....39

9.5 100Base-TX Operation.....40

9.6 100Base-TX Receiver.....42

9.7 10Base-T Operation.....43

9.8 Collision Detection.....43

9.9 Carrier Sense.....43

9.10 Auto-Negotiation.....43

9.11 Power Reduced Mode.....44

10. DC and AC Electrical Characteristics.....45

10.1 Absolute Maximum Ratings(25).....45



| | |
|---|-----------|
| 10.1.1 Operating Conditions..... | 45 |
| 10.2 DC Electrical Characteristics (VDD = 3.3V)..... | 45 |
| 10.3 AC Electrical Characteristics & Timing Waveform..... | 46 |
| 10.3.1 TP Interface..... | 46 |
| 10.3.2 Oscillator/Crystal Timing..... | 46 |
| 10.3.3 Processor Register Read Timing..... | 46 |
| 10.3.4 Processor Register Write Timing..... | 47 |
| 10.3.5 EEPROM Interface Timing..... | 48 |
| 11. Application Notes..... | 49 |
| 11.1 Network Interface Signal Routing..... | 49 |
| 11.2 10Base-T/100Base-TX (Auto MDIX Application)..... | 49 |
| 11.3 10Base-T/100Base-TX (Non Auto MDIX Application)..... | 50 |
| 11.4 Power Decoupling Capacitors..... | 51 |
| 11.5 Ground Plane Layout..... | 52 |
| 11.6 Power Plane Partitioning..... | 53 |
| 11.7 Magnetics Selection Guide..... | 54 |
| 11.8 Crystal Selection Guide..... | 54 |
| 12. Package Information..... | 55 |
| 13. Ordering Information..... | 56 |

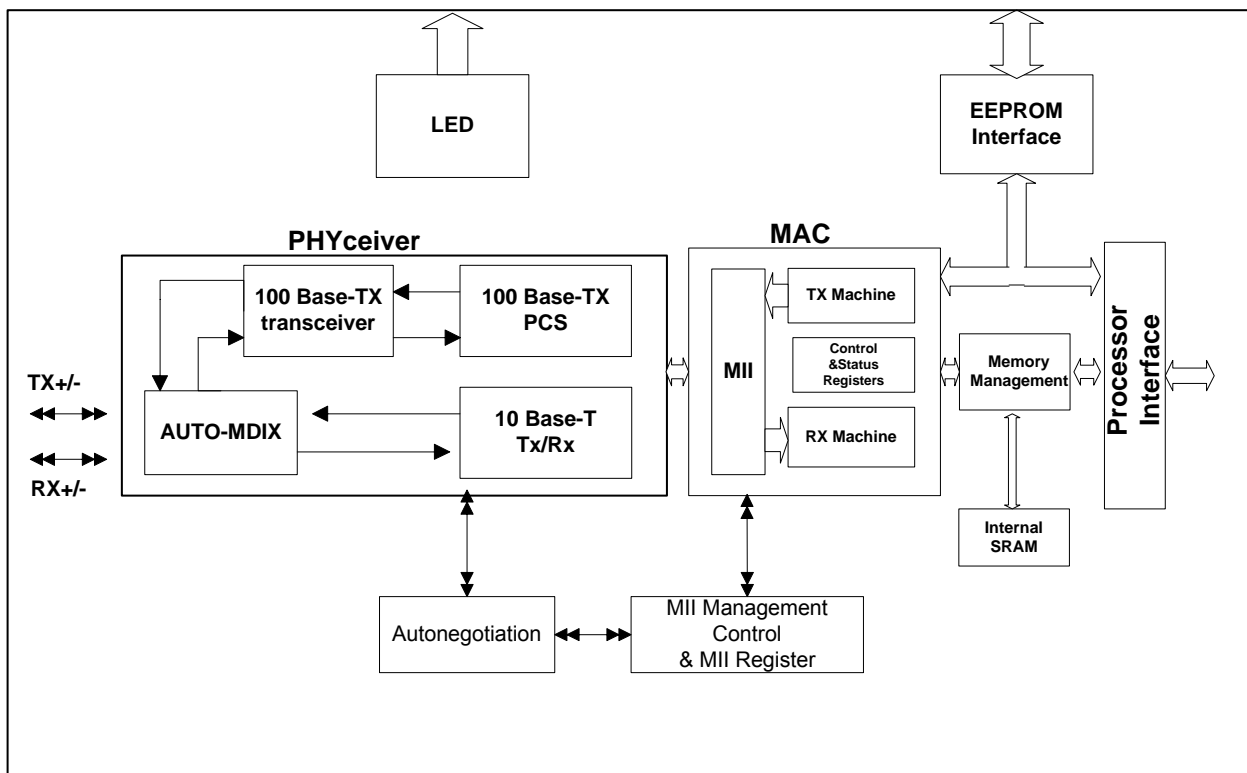
1. General Description

The DM9000A is a fully integrated and cost-effective low pin count single chip Fast Ethernet controller with a general processor interface, a 10/100M PHY and 4K Dword SRAM. It is designed with low power and high performance process that support 3.3V with 5V IO tolerance.

The DM9000A supports 8-bit and 16-bit data interfaces to internal memory accesses for various

processors. The PHY of the DM9000A can interface to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX with AUTO-MDIX. It is fully compliant with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9000A to take the maximum advantage of its abilities. The DM9000A also supports IEEE 802.3x full-duplex flow control..

2. Block Diagram



3. Features

48-pin LQFP

Supports processor interface: byte/word of I/O

command to internal memory data operation

Integrated 10/100M transceiver with AUTO-MDIX

Supports back pressure mode for half-duplex mode flow control

IEEE802.3x flow control for full-duplex mode

Supports wakeup frame, link status change and

magic packet events for remote wake up

Integrated 16K Byte SRAM

Build in 3.3V to 2.5V regulator

Supports early Transmit

Supports IP/TCP/UDP checksum generation and checking

Supports automatically load vendor ID and product ID from EEPROM

Optional EEPROM configuration

Very low power consumption mode:

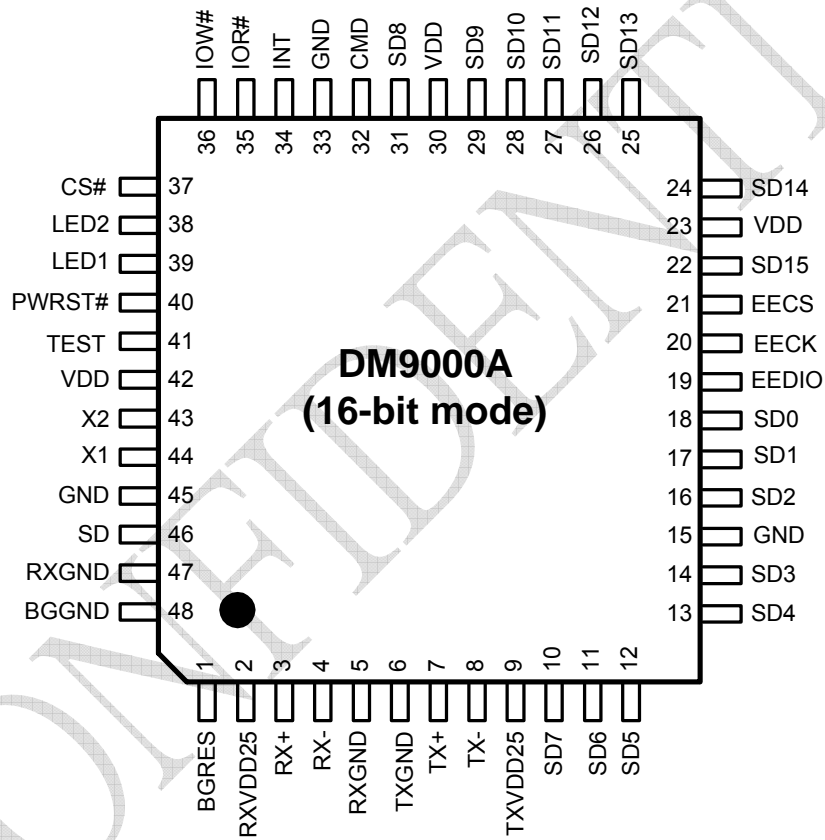
- Power reduced mode (cable detection)
- Power down mode
- Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.

Compatible with 3.3V and 5.0V tolerant I/O

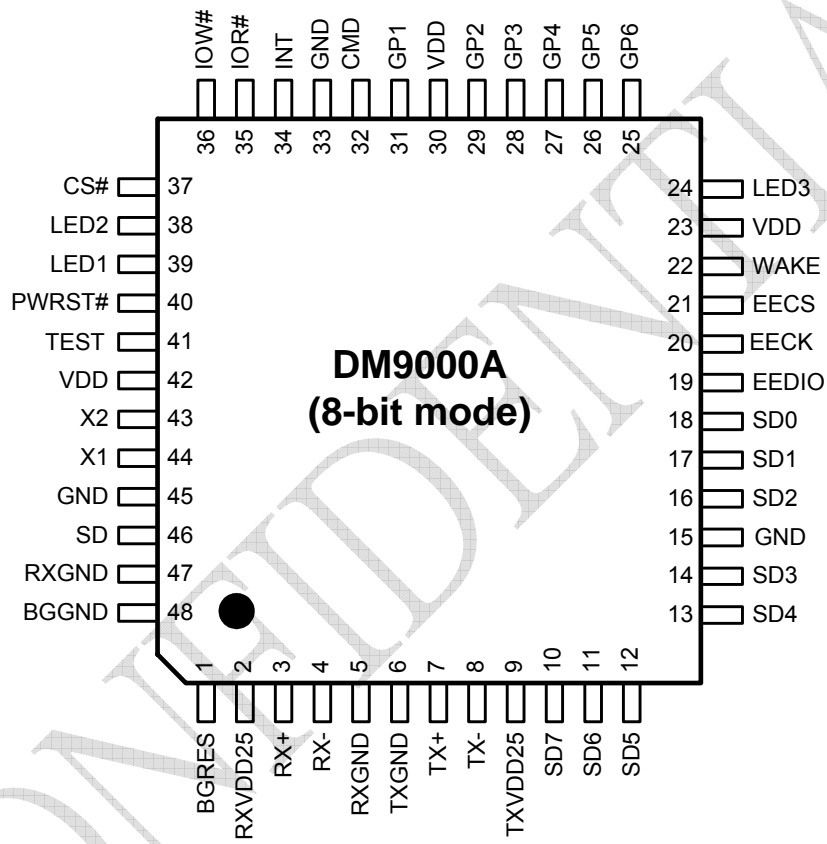
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4. Pin Configuration

4.1 (16-bit mode)



4.2 (8-bit mode)



5. Pin Description

I = Input O = Output I/O = Input/Output O/D = Open Drain P = Power
 # = asserted low PD = internal pull-low about 60K

5.1 Processor Interface

| Pin No. | Pin Name | Type | Description |
|-------------------------|----------|--------|---|
| 35 | IOR# | I,PD | Processor Read Command This pin is low active at default, its polarity can be modified by EEPROM setting. See the EEPROM content description for detail |
| 36 | IOW# | I,PD | Processor Write Command This pin is low active at default, its polarity can be modified by EEPROM setting. See the EEPROM content description for detail |
| 37 | CS# | I,PD | Chip Select A default low active signal used to select the DM9000A. Its polarity can be modified by EEPROM setting. See the EEPROM content description for detail. |
| 32 | CMD | I,PD | Command Type When high, the access of this command cycle is DATA port When low, the access of this command cycle is INDEX port |
| 34 | INT | O,PD | Interrupt Request This pin is high active at default, its polarity can be modified by EEPROM setting or by strap pin EECK. See the EEPROM content description for detail |
| 18,17,16,14,13,12,11,10 | SD0~7 | I/O,PD | Processor Data Bus bit 0~7 |
| 31,29,28,27,26,25,24,22 | SD8~15 | I/O,PD | Processor Data Bus bit 8~15 In 16-bit mode, these pins act as the processor data bus bit 8~15; When EECS pin is pulled high, they have other definitions. See 8-bit mode pin description for details. |

5.1.1 8-bit mode pins

| Pin No. | Pin Name | Type | Description |
|----------|----------|------|--|
| 22 | WAKE | O,PD | Issue a wake up signal when wake up event happens |
| 24 | LED3 | O,PD | Full-duplex LED In LED mode 1, Its low output indicates that the internal PHY is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY In LED mode 0, Its low output indicates that the internal PHY is operated in 10M mode, or it is floating for the 100M mode of the internal PHY Note: LED mode is defined in EEPROM setting. |
| 25,26,27 | GP6~4 | O,PD | General Purpose output pins: These pins are output only for general purpose that are configured by register 1Fh. GP6 pin also act as trap pin for the INT output type. When GP6 is pulled high, the INT is Open-Drain output type; Otherwise it is force output type. |



| | | | |
|----------|-------------|-----|--|
| 28,29,31 | GP3,GP2,GP1 | I/O | General I/O Ports Registers GPCR and GPR can program these pins These pins are input ports at default. |
|----------|-------------|-----|--|

5.2 EEPROM Interface

| Pin No. | Pin Name | Type | Description |
|---------|----------|--------|---|
| 19 | EEDIO | I/O,PD | IO Data to EEPROM |
| 20 | EECK | O,PD | Clock to EEPROM This pin is also used as the strap pin of the polarity of the INT pin When this pin is pulled high, the INT pin is low active; otherwise the INT pin is high active |
| 21 | EECS | O,PD | Chip Select to EEPROM This pin is also used as a strap pin to define the internal memory data bus width. When it is pulled high, the memory access bus is 8-bit; Otherwise it is 16-bit. |

5.3 Clock Interface

| Pin No. | Pin Name | Type | Description |
|---------|----------|------|-------------------|
| 43 | X2 | O | Crystal 25MHz Out |
| 44 | X1 | I | Crystal 25MHz In |

5.4 LED Interface

| Pin No. | Pin Name | Type | Description |
|---------|----------|------|--|
| 39 | LED1 | O | Speed LED Its low output indicates that the internal PHY is operated in 100M/S, or it is floating for the 10M mode of the internal PHY. This pin also acts as ISA bus IO16 defined in EEPROM setting in 16-bit mode. |
| 38 | LED2 | O | Link / Active LED In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only This pin also acts as ISA bus IOWAIT or WAKE defined in EEPROM setting in 16-bit mode. |

5.5 10/100 PHY/Fiber

| Pin No. | Pin Name | Type | Description |
|---------|----------|------|---|
| 46 | SD | I | Fiber-optic Signal Detect PECL signal, which indicates whether or not the fiber-optic receive pair is receiving valid levels |
| 48 | BGGND | P | Bandgap Ground |
| 1 | BGRES | I/O | Bandgap Pin |



DM9000A

Ethernet Controller with General Processor Interface

| | | | |
|------|---------|-----|-----------------------------|
| 2 | RXVDD25 | P | 2.5V power output for TP RX |
| 9 | TXVDD25 | P | 2.5V power output for TP TX |
| 3 | RX+ | I/O | TP RX Input |
| 4 | RX- | I/O | TP RX Input |
| 5,47 | RXGND | P | RX Ground |
| 6 | TXGND | P | TX Ground |
| 7 | TX+ | I/O | TP TX Output |
| 8 | TX- | I/O | TP TX Output |

5.6 Miscellaneous

| Pin No. | Pin Name | Type | Description |
|---------|----------|------|--|
| 41 | TEST | I | Operation Mode Force to ground in normal application |
| 40 | PWRST# | I | Power on Reset Active low signal to initiate the DM9000A The DM9000A is ready after 5us when this pin deasserted |

5.7 Power Pins

| Pin No. | Pin Name | Type | Description |
|----------|----------|------|---------------------------------|
| 23,30,42 | VDD | P | Digital VDD 3.3V power input |
| 15,33,45 | GND | P | Digital GND |

5.8 strap pins table

1: pull-high 1K~10K, 0: floating (default)

| Pin No. | Pin Name | Description |
|---------|----------|---|
| 20 | EECK | Polarity of INT 1: INT pin low active; 0: INT pin high active |
| 21 | EECS | DATA Bus Width 1: 8-bit 0: 16-bit |
| 25 | GP6 | INT output type in 8-bit mode 1: Open-Drain 0: force mode |

6. Vendor Control and Status Register Set

The DM9000A implements several control and status registers, which can be accessed by the host. These CSRs

are byte aligned. All CSRs are set to their default values by hardware or software reset unless they are specified

| Register | Description | Offset | Default value after reset |
|----------|---|---------|---------------------------|
| NCR | Network Control Register | 00H | 00H |
| NSR | Network Status Register | 01H | 00H |
| TCR | TX Control Register | 02H | 00H |
| TSR I | TX Status Register I | 03H | 00H |
| TSR II | TX Status Register II | 04H | 00H |
| RCR | RX Control Register | 05H | 00H |
| RSR | RX Status Register | 06H | 00H |
| ROCR | Receive Overflow Counter Register | 07H | 00H |
| BPTR | Back Pressure Threshold Register | 08H | 37H |
| FCTR | Flow Control Threshold Register | 09H | 38H |
| FCR | RX Flow Control Register | 0AH | 00H |
| EPCR | EEPROM & PHY Control Register | 0BH | 00H |
| EPAR | EEPROM & PHY Address Register | 0CH | 40H |
| EPDRL | EEPROM & PHY Low Byte Data Register | 0DH | XXH |
| EPDRH | EEPROM & PHY High Byte Data Register | 0EH | XXH |
| WCR | Wake Up Control Register (in 8-bit mode) | 0FH | 00H |
| PAR | Physical Address Register | 10H-15H | Determined by EEPROM |
| MAR | Multicast Address Register | 16H-1DH | XXH |
| GPCR | General Purpose Control Register (in 8-bit mode) | 1EH | 01H |
| GPR | General Purpose Register | 1FH | XXH |
| TRPAL | TX SRAM Read Pointer Address Low Byte | 22H | 00H |
| TRPAH | TX SRAM Read Pointer Address High Byte | 23H | 00H |
| RWPAL | RX SRAM Write Pointer Address Low Byte | 24H | 00H |
| RWPAH | RX SRAM Write Pointer Address High Byte | 25H | 0CH |
| VID | Vendor ID | 28H-29H | 0A46H |
| PID | Product ID | 2AH-2BH | 9000H |
| CHIPR | CHIP Revision | 2CH | 18H |
| TCR2 | TX Control Register 2 | 2DH | 00H |
| OCR | Operation Control Register | 2EH | 00H |
| SMCR | Special Mode Control Register | 2FH | 00H |
| ETXCSR | Early Transmit Control/Status Register | 30H | 00H |
| TCSCR | Transmit Check Sum Control Register | 31H | 00H |
| RCSCSR | Receive Check Sum Control Status Register | 32H | 00H |
| MRCMDX | Memory Data Pre-Fetch Read Command Without Address Increment Register | F0H | XXH |
| MRCMDX1 | Memory Data Read Command With Address Increment Register | F1H | XXH |
| MRCMD | Memory Data Read Command With Address Increment Register | F2H | XXH |



DM9000A

Ethernet Controller with General Processor Interface

| | | | |
|--------|--|-----|-----|
| MRRL | Memory Data Read_ address Register Low Byte | F4H | 00H |
| MRRH | Memory Data Read_ address Register High Byte | F5H | 00H |
| MWCMDX | Memory Data Write Command Without Address Increment Register | F6H | XXH |
| MWCMD | Memory Data Write Command With Address Increment Register | F8H | XXH |
| MWRL | Memory Data Write_ address Register Low Byte | FAH | 00H |
| MWRH | Memory Data Write_ address Register High Byte | FBH | 00H |
| TXPLL | TX Packet Length Low Byte Register | FCH | XXH |
| TXPLH | TX Packet Length High Byte Register | FDH | XXH |
| ISR | Interrupt Status Register | FEH | 00H |
| IMR | Interrupt Mask Register | FFH | 00H |

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type>

Where :

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

P = power on reset default value

H = hardware reset default value

S = software reset default value

E = default value from EEPROM

T = default value from strap pin

<Access Type>:

RO = Read only

RW = Read/Write

R/C = Read and Clear

RW/C1=Read/Write and Cleared by write 1

WO = Write only

Reserved bits are shaded and should be written with 0.

Reserved bits are undefined on read access.

6.1 Network Control Register (00H)

| Bit | Name | Default | Description |
|-----|----------|--------------|--|
| 7 | RESERVED | PH0,RW | Reserved |
| 6 | WAKEEN | P0,RW | Wakeup Event Enable work in 8-bit mode When set, it enables the wakeup function. Clearing this bit will also clears all wakeup event status This bit will not be affected after a software reset |
| 5 | RESERVED | 0,RO | Reserved |
| 4 | FCOL | PHS0,RW | Force Collision Mode, used for testing |
| 3 | FDX | PHS0,RO | Full-Duplex Mode of the internal PHY. |
| 2:1 | LBK | PHS00, RW | Loopback Mode Bit 2 1 0 0 Normal 0 1 MAC Internal loopback 1 0 Internal PHY 100M mode digital loopback 1 1 (Reserved) |
| 0 | RST | PH0,RW | Software reset and auto clear after 10us |

6.2 Network Status Register (01H)

| Bit | Name | Default | Description |
|-----|----------|----------------|---|
| 7 | SPEED | X,RO | Media Speed 0:100Mbps 1:10Mbps, when Internal PHY is used. This bit has no meaning when LINKST=0 |
| 6 | LINKST | X,RO | Link Status 0:link failed 1:link OK, |
| 5 | WAKEST | P0, RW/C1 | Wakeup Event Status. Clears by read or write 1 (work in 8-bit mode) This bit will not be affected after software reset |
| 4 | RESERVED | 0,RO | Reserved |
| 3 | TX2END | PHS0, RW/C1 | TX Packet 2 Complete Status. Clears by read or write 1 Transmit completion of packet index 2 |
| 2 | TX1END | PHS0, RW/C1 | TX Packet 1 Complete status. Clears by read or write 1 Transmit completion of packet index 1 |
| 1 | RXOV | PHS0,RO | RX FIFO Overflow |
| 0 | RESERVED | 0,RO | Reserved |

6.3 TX Control Register (02H)

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7 | RESERVED | 0,RO | Reserved |
| 6 | TJDIS | PHS0,RW | Transmit Jabber Disable When set, the transmit Jabber Timer (2048 bytes) is disabled. Otherwise it is Enable |
| 5 | EXCECM | PHS0,RW | Excessive Collision Mode Control : 0:aborts this packet when excessive collision counts more than 15, 1: still tries to transmit this packet |
| 4 | PAD_DIS2 | PHS0,RW | PAD Appends Disable for Packet Index 2 |
| 3 | CRC_DIS2 | PHS0,RW | CRC Appends Disable for Packet Index 2 |
| 2 | PAD_DIS1 | PHS0,RW | PAD Appends Disable for Packet Index 1 |
| 1 | CRC_DIS1 | PHS0,RW | CRC Appends Disable for Packet Index 1 |
| 0 | TXREQ | PHS0,RW | TX Request. Auto clears after sending completely |

6.4 TX Status Register I (03H) for packet index I

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7 | TJTO | PHS0,RO | Transmit Jabber Time Out It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted |
| 6 | LC | PHS0,RO | Loss of Carrier It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode |
| 5 | NC | PHS0,RO | No Carrier It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode |
| 4 | LC | PHS0,RO | Late Collision It is set when a collision occurs after the collision window of 64 bytes |
| 3 | COL | PHS0,RO | Collision Packet It is set to indicate that the collision occurs during transmission |
| 2 | EC | PHS0,RO | Excessive Collision It is set to indicate that the transmission is aborted due to 16 excessive collisions |
| 1:0 | RESERVED | 0,RO | Reserved |

6.5 TX Status Register II (04H) for packet index I I

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7 | TJTO | PHS0,RO | Transmit Jabber Time Out It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted |
| 6 | LC | PHS0,RO | Loss of Carrier It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode |
| 5 | NC | PHS0,RO | No Carrier It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode |
| 4 | LC | PHS0,RO | Late Collision It is set when a collision occurs after the collision window of 64 bytes |
| 3 | COL | PHS0,RO | Collision packet, collision occurs during transmission |
| 2 | EC | PHS0,RO | Excessive Collision It is set to indicate that the transmission is aborted due to 16 excessive collisions |
| 1:0 | RESERVED | 0,RO | Reserved |

6.6 RX Control Register (05H)

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7 | RESERVED | PHS0,RW | Reserved |
| 6 | WTDIS | PHS0,RW | Watchdog Timer Disable When set, the Watchdog Timer (2048 bytes) is disabled. Otherwise it is enabled |
| 5 | DIS_LONG | PHS0,RW | Discard Long Packet Packet length is over 1522byte |
| 4 | DIS_CRC | PHS0,RW | Discard CRC Error Packet |
| 3 | ALL | PHS0,RW | Pass All Multicast |
| 2 | RUNT | PHS0,RW | Pass Runt Packet |
| 1 | PRMSC | PHS0,RW | Promiscuous Mode |
| 0 | RXEN | PHS0,RW | RX Enable |

6.7 RX Status Register (06H)

| Bit | Name | Default | Description |
|-----|------|---------|---|
| 7 | RF | PHS0,RO | Runt Frame It is set to indicate that the size of the received frame is smaller than 64 bytes |
| 6 | MF | PHS0,RO | Multicast Frame It is set to indicate that the received frame has a multicast address |
| 5 | LCS | PHS0,RO | Late Collision Seen It is set to indicate that a late collision is found during the frame reception |
| 4 | RWTO | PHS0,RO | Receive Watchdog Time-Out It is set to indicate that it receives more than 2048 bytes |
| 3 | PLE | PHS0,RO | Physical Layer Error It is set to indicate that a physical layer error is found during the frame reception |
| 2 | AE | PHS0,RO | Alignment Error It is set to indicate that the received frame ends with a non-byte boundary |
| 1 | CE | PHS0,RO | CRC Error It is set to indicate that the received frame ends with a CRC error |
| 0 | FOE | PHS0,RO | FIFO Overflow Error It is set to indicate that a FIFO overflow error happens during the frame reception |

6.8 Receive Overflow Counter Register (07H)

| Bit | Name | Default | Description |
|-----|------|----------|--|
| 7 | RXFU | PHS0,R/C | Receive Overflow Counter Overflow This bit is set when the ROC has an overflow condition |
| 6:0 | ROC | PHS0,R/C | Receive Overflow Counter This is a statistic counter to indicate the received packet count upon FIFO overflow |

6.9 Back Pressure Threshold Register (08H)

| Bit | Name | Default | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|------|-------------|--|-------|------|------|------|------|---|---|---|---|-----|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|---|---|---|---|-------|
| 7:4 | BPHW | PHS3, RW | Back Pressure High Water Overflow Threshold. MAC will generate the jam pattern when RX SRAM free space is lower than this threshold value The default is 3K-byte free space. Please do not exceed SRAM size (1 unit=1K bytes) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3:0 | JPT | PHS7, RW | Jam Pattern Time. Default is 200us <table border="1"> <thead> <tr> <th>bit3</th> <th>bit2</th> <th>bit1</th> <th>bit0</th> <th>time</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>5us</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>10us</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>15us</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25us</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>50us</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>100us</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>150us</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>200us</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>250us</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>300us</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>350us</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>400us</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>450us</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>500us</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>550us</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>600us</td></tr> </tbody> </table> | bit3 | bit2 | bit1 | bit0 | time | 0 | 0 | 0 | 0 | 5us | 0 | 0 | 0 | 1 | 10us | 0 | 0 | 1 | 0 | 15us | 0 | 0 | 1 | 1 | 25us | 0 | 1 | 0 | 0 | 50us | 0 | 1 | 0 | 1 | 100us | 0 | 1 | 1 | 0 | 150us | 0 | 1 | 1 | 1 | 200us | 1 | 0 | 0 | 0 | 250us | 1 | 0 | 0 | 1 | 300us | 1 | 0 | 1 | 0 | 350us | 1 | 0 | 1 | 1 | 400us | 1 | 1 | 0 | 0 | 450us | 1 | 1 | 0 | 1 | 500us | 1 | 1 | 1 | 0 | 550us | 1 | 1 | 1 | 1 | 600us |
| bit3 | bit2 | bit1 | bit0 | time | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 5us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 10us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 15us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 25us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | 50us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 100us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 150us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | 200us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 250us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 300us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 350us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 400us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 450us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | 500us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 550us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 600us | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

6.10 Flow Control Threshold Register (09H)

| Bit | Name | Default | Description |
|-----|------|-------------|---|
| 7:4 | HWOT | PHS3, RW | RX FIFO High Water Overflow Threshold Send a pause packet with pause_time=FFFFH when the RX RAM free space is less than this value., If this value is zero, its means no free RX SRAM space. The default value is 3K-byte free space. Please do not exceed SRAM size (1 unit=1K bytes) |
| 3:0 | LWOT | PHS8, RW | RX FIFO Low Water Overflow Threshold Send a pause packet with pause_time=0000 when RX SRAM free space is larger than this value. This pause packet is enabled after the high water pause packet is transmitted. The default SRAM free space is 8K-byte. Please do not exceed SRAM size (1 unit=1K bytes) |

6.11 RX/TX Flow Control Register (0AH)

| Bit | Name | Default | Description |
|-----|-------|----------|---|
| 7 | TXP0 | HPS0,RW | TX Pause Packet Auto clears after pause packet transmission completion. Set to TX pause packet with time = 0000h |
| 6 | TXPF | HPS0,RW | TX Pause packet Auto clears after pause packet transmission completion. Set to TX pause packet with time = FFFFH |
| 5 | TXPEN | HPS0,RW | Force TX Pause Packet Enable Enables the pause packet for high/low water threshold control |
| 4 | BKPA | HPS0,RW | Back Pressure Mode This mode is for half duplex mode only. It generates a jam pattern when any packet comes and RX SRAM is over BPHW of register 8. |
| 3 | BKPM | HPS0,RW | Back Pressure Mode This mode is for half duplex mode only. It generates a jam pattern when a packet's DA matches and RX SRAM is over BPHW of register 8. |
| 2 | RXPS | HPS0,R/C | RX Pause Packet Status, latch and read clearly |
| 1 | RXPCS | HPS0,RO | RX Pause Packet Current Status |
| 0 | FLCE | HPS0,RW | Flow Control Enable Set to enable the flow control mode (i.e. can disable DM9000A TX function) |

6.12 EEPROM & PHY Control Register (0BH)

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7:6 | RESERVED | 0,RO | Reserved |
| 5 | REEP | PH0,RW | Reload EEPROM. Driver needs to clear it up after the operation completes |
| 4 | WEP | PH0,RW | Write EEPROM Enable |
| 3 | EPOS | PH0,RW | EEPROM or PHY Operation Select When reset, select EEPROM; when set, select PHY |
| 2 | ERPRR | PH0,RW | EEPROM Read or PHY Register Read Command. Driver needs to clear it up after the operation completes. |
| 1 | ERPRW | PH0,RW | EEPROM Write or PHY Register Write Command. Driver needs to clear it up after the operation completes. |
| 0 | ERRE | PH0,RO | EEPROM Access Status or PHY Access Status When set, it indicates that the EEPROM or PHY access is in progress |

6.13 EEPROM & PHY Address Register (0CH)

| Bit | Name | Default | Description |
|-----|---------|---------|---|
| 7:6 | PHY_ADR | PH01,RW | PHY Address bit 1 and 0, the PHY address bit [4:2] is force to 0. Force to 01 in application. |
| 5:0 | EROA | PH0,RW | EEPROM Word Address or PHY Register Number. |

6.14 EEPROM & PHY Data Register (EE_PHY_L : 0DH EE_PHY_H : 0EH)

| Bit | Name | Default | Description |
|-----|----------|---------|---|
| 7:0 | EE_PHY_L | PH0,RW | EEPROM or PHY Low Byte Data The low-byte data read from or write to EEPROM or PHY. |
| 7:0 | EE_PHY_H | PH0,RW | EEPROM or PHY High Byte Data The high-byte data read from or write to EEPROM or PHY. |

6.15 Wake Up Control Register (0FH) (in 8-bit mode)

| Bit | Name | Type | Description |
|-----|----------|-------|--|
| 7:6 | RESERVED | 0,RO | Reserved |
| 5 | LINKEN | P0,RW | When set, it enables Link Status Change Wake up Event This bit will not be affected after software reset |
| 4 | SAMPLEEN | P0,RW | When set, it enables Sample Frame Wake up Event This bit will not be affected after software reset |
| 3 | MAGICEN | P0,RW | When set, it enables Magic Packet Wake up Event This bit will not be affected after software reset |
| 2 | LINKST | P0,RO | When set, it indicates that Link Change and Link Status Change Event occurred This bit will not be affected after software reset |
| 1 | SAMPLEST | P0,RO | When set, it indicates that the sample frame is received and Sample Frame Event occurred. This bit will not be affected after software reset |
| 0 | MAGICST | P0,RO | When set, indicates the Magic Packet is received and Magic packet Event occurred. This bit will not be affected after a software reset |

6.16 Physical Address Register (10H~15H)

| Bit | Name | Default | Description |
|-----|------|---------|-------------------------------|
| 7:0 | PAB5 | E,RW | Physical Address Byte 5 (15H) |
| 7:0 | PAB4 | E,RW | Physical Address Byte 4 (14H) |
| 7:0 | PAB3 | E,RW | Physical Address Byte 3 (13H) |
| 7:0 | PAB2 | E,RW | Physical Address Byte 2 (12H) |
| 7:0 | PAB1 | E,RW | Physical Address Byte 1 (11H) |
| 7:0 | PAB0 | E,RW | Physical Address Byte 0 (10H) |

6.17 Multicast Address Register (16H~1DH)

| Bit | Name | Default | Description |
|-----|------|---------|--------------------------------|
| 7:0 | MAB7 | X,RW | Multicast Address Byte 7 (1DH) |
| 7:0 | MAB6 | X,RW | Multicast Address Byte 6 (1CH) |
| 7:0 | MAB5 | X,RW | Multicast Address Byte 5 (1BH) |
| 7:0 | MAB4 | X,RW | Multicast Address Byte 4 (1AH) |
| 7:0 | MAB3 | X,RW | Multicast Address Byte 3 (19H) |
| 7:0 | MAB2 | X,RW | Multicast Address Byte 2 (18H) |
| 7:0 | MAB1 | X,RW | Multicast Address Byte 1 (17H) |
| 7:0 | MAB0 | X,RW | Multicast Address Byte 0 (16H) |

6.18 General purpose control Register (1EH) (in 8-bit mode)

| Bit | Name | Default | Description |
|-----|----------|---------------|--|
| 7 | RESERVED | PH0,RO | Reserved |
| 6:4 | GPC64 | PH, 111,RO | General Purpose Control 6~4 Define the input/output direction of pins GP6~4 respectively. These bits are all forced to "1"s, so pins GP6~4 are output only. |
| 3:1 | GPC31 | PH, 000,RW | General Purpose Control 3~1 Define the input/output direction of pins GP 3~1 respectively. When a bit is set 1, the direction of correspondent bit of General Purpose Register is output. Other defaults are input |
| 0 | RESERVED | PH1,RO | Reserved |

6.19 General purpose Register (1FH)

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7 | RESERVED | 0,RO | Reserved |
| 6-4 | GPO | PH0,RW | General Purpose Output 6~4 (in 8-bit mode) These bits are reflect to pin GP6~4 respectively. |
| 3:1 | GPIO | PH0,RW | General Purpose (in 8-bit mode) When the correspondent bit of General Purpose Control Register is 1, the value of the bit is reflected to pin GP3~1 respectively. When the correspondent bit of General Purpose Control Register is 0, the value of the bit to be read is reflected from correspondent pins of GP3~1 respectively. |
| 0 | PHYPD | ET1,RW | PHY Power Down Control 1: power down PHY 0: power up PHY |

6.20 TX SRAM Read Pointer Address Register (22H~23H)

| Bit | Name | Default | Description |
|-----|-------|---------|--|
| 7:0 | TRPAH | PS0,RO | TX SRAM Read Pointer Address High Byte (23H) |
| 7:0 | TRPAL | PS0,RO | TX SRAM Read Pointer Address Low Byte (22H) |

6.21 RX SRAM Write Pointer Address Register (24H~25H)

| Bit | Name | Default | Description |
|-----|-------|-----------|---|
| 7:0 | RWPAH | PS,0CH,RO | RX SRAM Write Pointer Address High Byte (25H) |
| 7:0 | RWPAL | PS,00H,RO | RX SRAM Write Pointer Address Low Byte (24H) |

6.22 Vendor ID Register (28H~29H)

| Bit | Name | Default | Description |
|-----|------|------------|---------------------------|
| 7:0 | VIDH | PHE,0AH,RO | Vendor ID High Byte (29H) |
| 7:0 | VIDL | PHE,46H,RO | Vendor ID Low Byte (28H) |

6.23 Product ID Register (2AH~2BH)

| Bit | Name | Default | Description |
|-----|------|------------|----------------------------|
| 7:0 | PIDH | PHE,90H,RO | Product ID High Byte (2BH) |
| 7:0 | PIDL | PHE,00H,RO | Product ID Low Byte (2AH) |

6.24 Chip Revision Register (2CH)

| Bit | Name | Default | Description |
|-----|-------|---------|---------------|
| 7:0 | CHIPR | 18H,RO | CHIP Revision |

6.25 Transmit Control Register 2 (2DH)

| Bit | Name | Default | Description |
|-----|------|---------|--|
| 7 | LED | PH0,RW | Led Mode When set, the LED pins act as led mode 1. When cleared, the led mode is default mode 0 or depending EEPROM setting. |
| 6 | RLCP | PH0,RW | Retry Late_Collision Packet Re-transmit the packet with late-collision |
| 5 | DTU | PH0,RW | Disable TX Underrun Retry Disable to re-transmit the underruned packet |

| | | | |
|-----|-------|--------|--|
| 4 | ONEPM | PH0,RW | One Packet Mode When set, only one packet transmit command can be issued before transmit completed. When cleared, at most two packet transmit command can be issued before transmit completed. |
| 3~0 | IFGS | PH0,RW | Inter-Frame Gap Setting 0XXX: 96-bit 1000: 64-bit 1001: 72-bit 1010:80-bit 1011:88-bit 1100:96-bit 1101:104-bit 1110: 112-bit 1111:120-bit |

6.26 Operation Test Control Register (2EH)

| Bit | Name | Default | Description |
|-----|----------|---------|--|
| 7~6 | SCC | PH0,RW | System Clock Control Set the internal system clock. 00: 50Mhz 01: 20MHz 10: 100MHz 11: Reserved |
| 5 | RESERVED | PH0,RW | Reserved |
| 4 | SOE | PH0,RW | Internal SRAM Output-Enable Always ON |
| 3 | SCS | PH0,RW | Internal SRAM Chip-Select Always ON |
| 2~0 | PHYOP | PH0,RW | Internal PHY operation mode for testing |

6.27 Special Mode Control Register (2FH)

| Bit | Name | Default | Description |
|-----|----------|---------|------------------------------|
| 7 | SM_EN | PH0,RW | Special Mode Enable |
| 6~3 | RESERVED | PH0,RW | Reserved |
| 2 | FLC | PH0,RW | Force Late Collision |
| 1 | FB1 | PH0,RW | Force Longest Back-off time |
| 0 | FB0 | PH0,RW | Force Shortest Back-off time |

6.28 Early Transmit Control/Status Register (30H)

| Bit | Name | Default | Description |
|-----|----------|----------|---|
| 7 | ETE | HPS0, RW | Early Transmit Enable Enable bits[2:0] |
| 6 | ETS2 | HPS0, RO | Early Transmit Status II |
| 5 | ETS1 | HPS0, RO | Early Transmit Status I |
| 4~2 | RESERVED | 000, RO | Reserved |
| 1~0 | ETT | HPS0, RW | Early Transmit Threshold Start transmit when data write to TX FIFO reach the byte-count threshold Bit-1 bit-0 threshold ——— ——— ——— 0 0 : 12.5% 0 1 : 25% 1 0 : 50% 1 1 : 75% |

6.29 Check Sum Control Register (31H)

| Bit | Name | Default | Description |
|-----|----------|----------|--------------------------------|
| 7~3 | RESERVED | 0, RO | Reserved |
| 2 | UDPCSE | HPS0, RW | UDP CheckSum Generation Enable |
| 1 | TCPCSE | HPS0, RW | TCP CheckSum Generation Enable |
| 0 | IPCSE | HPS0, RW | IP CheckSum Generation Enable |

6.30 Receive Check Sum Status Register (32H)

| Bit | Name | Default | Description |
|-----|--------|----------|---|
| 7 | UDPS | HPS0, RO | UDP CheckSum Status 1: checksum fail, if UDP packet |
| 6 | TCPS | HPS0, RO | TCP CheckSum Status 1: checksum fail, if TCP packet |
| 5 | IPS | HPS0, RO | IP CheckSum Status 1: checksum fail, if IP packet |
| 4 | UDPP | HPS0, RO | UDP Packet |
| 3 | TCPP | HPS0, RO | TCP Packet |
| 2 | IPP | HPS0, RO | IP Packet |
| 1 | RCSSEN | HPS0, RW | Receive CheckSum Checking Enable When set, the checksum status (bit 7~2) will be stored in packet's first byte(bit 7~2) of status header respectively. |
| 0 | DCSE | HPS0, RW | Discard CheckSum Error Packet When set, if IP/TCP/UDP checksum field is error, this packet will be discarded. |

6.31 Memory Data Pre-Fetch Read Command without Address Increment Register (F0H)

| Bit | Name | Default | Description |
|-----|--------|---------|---|
| 7:0 | MRCMDX | X,RO | Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. And the DM9000A starts to pre-fetch the SRAM data to internal data buffers. |

6.32 Memory Data Read Command without Address Increment Register (F1H)

| Bit | Name | Default | Description |
|-----|---------|---------|--|
| 7:0 | MRCMDX1 | X,RO | Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged |

6.33 Memory Data Read Command with Address Increment Register (F2H)

| Bit | Name | Default | Description |
|-----|-------|---------|---|
| 7:0 | MRCMD | X,RO | Read data from RX SRAM. After the read of this command, the read pointer is increased by 1 or 2 depends on the operator mode (8-bit or 16-bit respectively) |

6.34 Memory Data Read address Register (F4H~F5H)

| Bit | Name | Default | Description |
|-----|-------|---------|---|
| 7:0 | MDRAH | PHS0,RW | Memory Data Read address High Byte. It will be set to 0Ch, when IMR bit7 =1 |
| 7:0 | MDRAL | PHS0,RW | Memory Data Read address Low Byte |

6.35 Memory Data Write Command without Address Increment Register (F6H)

| Bit | Name | Default | Description |
|-----|--------|---------|--|
| 7:0 | MWCMDX | X,WO | Write data to TX SRAM. After the write of this command, the write pointer is unchanged |

6.36 Memory data write command with address increment Register (F8H)

| Bit | Name | Default | Description |
|-----|-------|---------|--|
| 7:0 | MWCMD | X,WO | Write Data to TX SRAM After the write of this command, the write pointer is increased by 1 or 2, depends on the operator mode. (8-bit or 16-bit respectively) |

6.37 Memory data write address Register (FAH~FBH)

| Bit | Name | Default | Description |
|-----|-------|---------|-------------------------------------|
| 7:0 | MDRAH | PHS0,RW | Memory Data Write address High Byte |
| 7:0 | MDRAL | PHS0,RW | Memory Data Write address Low Byte |

6.38 TX Packet Length Register (FCH~FDH)

| Bit | Name | Default | Description |
|-----|-------|---------|----------------------------|
| 7:0 | TXPLH | X,R/W | TX Packet Length High byte |
| 7:0 | TXPLL | X,R/W | TX Packet Length Low byte |

6.39 Interrupt Status Register (FEH)

| Bit | Name | Default | Description |
|-----|----------|------------|-----------------------------------|
| 7 | IOMODE | T0, RO | 0 : 16-bit mode 1 : 8-bit mode |
| 6 | RESERVED | RO | Reserved |
| 5 | LNKCHG | PHS0,RW/C1 | Link Status Change |
| 4 | UDRUN | PHS0,RW/C1 | Transmit Underrun |
| 3 | ROO | PHS0,RW/C1 | Receive Overflow Counter Overflow |
| 2 | ROS | PHS0,RW/C1 | Receive Overflow |
| 1 | PT | PHS0,RW/C1 | Packet Transmitted |
| 0 | PR | PHS0,RW/C1 | Packet Received |

6.40 Interrupt Mask Register (FFH)

| Bit | Name | Default | Description |
|-----|----------|---------|---|
| 7 | PAR | HPS0,RW | Enable the SRAM read/write pointer to automatically return to the start address when pointer addresses are over the SRAM size. Driver needs to set. When driver sets this bit, REG_F5 will set to 0Ch automatically |
| 6 | RESERVED | RO | Reserved |
| 5 | LNKCHGI | PHS0,RW | Enable Link Status Change Interrupt |
| 4 | UDRUNI | PHS0,RW | Enable Transmit Underrun Interrupt |
| 3 | ROOI | PHS0,RW | Enable Receive Overflow Counter Overflow Interrupt |
| 2 | ROI | PHS0,RW | Enable Receive Overflow Interrupt |
| 1 | PTI | PHS0,RW | Enable Packet Transmitted Interrupt |
| 0 | PRI | PHS0,RW | Enable Packet Received Interrupt |

7. EEPROM Format

| name | Word | offset | Description |
|----------------------|------|--------|---|
| MAC address | 0 | 0~5 | 6 Byte Ethernet Address |
| Auto Load Control | 3 | 6-7 | Bit 1:0=01: Update vendor ID and product ID Bit 3:2=01: Accept setting of WORD6 [8:0] Bit 5:4=01: reserved Bit 7:6=01: Accept setting of WORD7 [3:0] (in 8-bit mode) Bit 9:8=01: reserved Bit 11:10=01: Accept setting of WORD7 [7] Bit 13:12=01: Accept setting of WORD7 [8] Bit 15:14=01: Accept setting of WORD7 [15:12] |
| Vendor ID | 4 | 8-9 | 2 byte vendor ID (Default: 0A46H) |
| Product ID | 5 | 10-11 | 2 byte product ID (Default: 9000H) |
| pin control | 6 | 12-13 | When word 3 bit [3:2]=01, these bits can control the CS#, IOR#, IOW# and INT pins polarity. Bit0: CS# pin is active low when set (default active low) Bit1: IOR# pin is active low when set (default: active low) Bit2: IOW# pin is active low when set (default: active low) Bit3: INT pin is active low when set (default: active high) Bit4: INT pin is open-collected (default: force output) Bit 15:5: Reserved |
| Wake-up mode control | 7 | 14-15 | Bit0: The WAKE pin is active low when set (default: active high) Bit1: The WAKE pin is in pulse mode when set (default: level mode) Bit2: magic wakeup event is enabled when set. (default: disable) Bit3: link_change wakeup event is enabled when set (default disable) Bit6:4: reserved Bit7: LED mode 1 (default: mode 0) Bit8: internal PHY is enabled after power-on (default: disable) Bit11:9: reserved Bit13:12: 01 = LED2 act as IOWAIT in 16-bit mode Bit13:12: 10 = LED2 act as WAKE in 16-bit mode Bit14: 1: AUTO-MDIX ON, 0: AUTO-MDIX OFF(default ON) Bit 15: LED1 act as IO16 in 16-bit mode |

8. PHY Register Description

| ADD | Name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---------------------|--------------|-------------|--------------|---------------|-------------|-----------|----------------|----------------|--------------|--------------|----------------|--------------------------------------|---------------|--------------|---------------|------------------|
| 00 | CONTR OL | Reset | Loop back | Speed select | Auto-N Enable | Power Down | Isolate | Restart Auto-N | Full Duplex | Coll. Test | Reserved | | | | | | |
| | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 000_0000 | | | | | | |
| 01 | STATUS | T4 Cap. | TX FDX Cap. | TX HDX Cap. | 10 FDX Cap. | 10 HDX Cap. | Reserved | | | | Pream. Supr. | Auto-N Compl. | Remote Fault | Auto-N Cap. | Link Status | Jabber Detect | Extd Cap. |
| | | 0 | 1 | 1 | 1 | 1 | 0000 | | | | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 02 | PHYID1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 03 | PHYID2 | 1 | 0 | 1 | 1 | 1 | 0 | Model No. | | | | Version No. | | | | | |
| | | | | | | 01010 | | | | 0000 | | | | | | | |
| 04 | Auto-Neg. Advertise | Next Page | FLP Rcv Ack | Remote Fault | Reserved | | FC Adv | T4 Adv | TX FDX Adv | TX HDX Adv | 10 FDX Adv | 10 HDX Adv | Advertised Protocol Selector Field | | | | |
| 05 | Link Part. Ability | LP Next Page | LP Ack | LP RF | Reserved | | LP FC | LP T4 | LP TX FDX | LP TX HDX | LP 10 FDX | LP 10 HDX | Link Partner Protocol Selector Field | | | | |
| 06 | Auto-Neg. Expansion | Reserved | | | | | | | | | | Pardet Fault | LP Next Pg Able | Next Pg Able | New Pg Rcv | LP AutoN Cap. | |
| 16 | Specified Config. | BP 4B5B | BP SCR | BP ALIGN | BP_AD P OK | Reserve dr | TX | Reserve d | Reserve d | Force 100LNK | Reserve d | Reserve d | RPDCTR -EN | Reset St. Mch | Pream. Supr. | Sleep mode | Remote LoopOut |
| 17 | Specified Conf/Stat | 100 FDX | 100 HDX | 10 FDX | 10 HDX | Reserve d | Reverse d | Reverse d | PHY ADDR [4:0] | | | | Auto-N. Monitor Bit [3:0] | | | | |
| 18 | 10T Conf/Stat | Rsvd | LP Enable | HBE Enable | SQUE Enable | JAB Enable | Reserve d | Reserved | | | | | | | | | Polarity Reverse |
| 19 | PWDOR | Reserved | | | | | | | PD10DRV | PD100I | PDchip | PDorm | PDaeq | PDdrv | PDekli | PDeco | PD10 |
| 20 | Specified config | TSTSE1 | TSTSE2 | FORCE_TXSD | FORCE_FEF | Reserved | | | | MDIX_C NTL | AutoNeg_lpbk | Mdix_fix Value | Mdix_do wn | MonSel1 | MonSel0 | Reserve d | PD_valu e |

Key to Default

In the register description that follows, the default column takes the form:
 <Reset Value>, <Access Type> / <Attribute(s)>

RO = Read only
 RW = Read/Write

Where :

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

<Attribute (s)>:

- SC = Self clearing
- P = Value permanently set
- LL = Latching low
- LH = Latching high

<Access Type>:

8.1 Basic Mode Control Register (BMCR) - 00

| Bit | Bit Name | Default | Description |
|------|--------------------------|----------|--|
| 0.15 | Reset | 0, RW/SC | Reset 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed |
| 0.14 | Loopback | 0, RW | Loopback Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before receive |
| 0.13 | Speed selection | 1, RW | Speed Select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type |
| 0.12 | Auto-negotiation enable | 1, RW | Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status |
| 0.11 | Power down | 0, RW | Power Down While in the power-down state, the PHY should respond to management transactions. 1=Power down 0=Normal operation |
| 0.10 | Isolate | 0,RW | Isolate Force to 0 in application. |
| 0.9 | Restart Auto-negotiation | 0,RW/SC | Restart Auto-negotiation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM9000A. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation |

| | | | |
|---------|----------------|------|---|
| 0.8 | Duplex mode | 1,RW | Duplex Mode 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation |
| 0.7 | Collision test | 0,RW | Collision Test 1 = Collision test enabled. When set, this bit will cause the collision asserted during the transmit period. 0 = Normal operation |
| 0.6-0.0 | Reserved | 0,RO | Reserved Read as 0, ignore on write |

8.2 Basic Mode Status Register (BMSR) - 01

| Bit | Bit Name | Default | Description |
|----------|------------------------|---------|--|
| 1.15 | 100BASE-T4 | 0,RO/P | 100BASE-T4 Capable 1 = DM9000A is able to perform in 100BASE-T4 mode 0 = DM9000A is not able to perform in 100BASE-T4 mode |
| 1.14 | 100BASE-TX full-duplex | 1,RO/P | 100BASE-TX Full Duplex Capable 1 = DM9000A is able to perform 100BASE-TX in full duplex mode 0 = DM9000A is not able to perform 100BASE-TX in full duplex mode |
| 1.13 | 100BASE-TX half-duplex | 1,RO/P | 100BASE-TX Half Duplex Capable 1 = DM9000A is able to perform 100BASE-TX in half duplex mode 0 = DM9000A is not able to perform 100BASE-TX in half duplex mode |
| 1.12 | 10BASE-T full-duplex | 1,RO/P | 10BASE-T Full Duplex Capable 1 = DM9000A is able to perform 10BASE-T in full duplex mode 0 = DM9000A is not able to perform 10BASE-TX in full duplex mode |
| 1.11 | 10BASE-T half-duplex | 1,RO/P | 10BASE-T Half Duplex Capable 1 = DM9000A is able to perform 10BASE-T in half duplex mode 0 = DM9000A is not able to perform 10BASE-T in half duplex mode |
| 1.10-1.7 | Reserved | 0,RO | Reserved Read as 0, ignore on write |
| 1.6 | MF preamble | 1,RO | Frame Preamble Suppression |

| | | | |
|-----|---------------------------|----------|---|
| | suppression | | 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed |
| 1.5 | Auto-negotiation Complete | 0,RO | Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed |
| 1.4 | Remote fault | 0, RO/LH | Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9000A implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected |
| 1.3 | Auto-negotiation ability | 1,RO/P | Auto Configuration Ability 1 = DM9000A is able to perform auto-negotiation 0 = DM9000A is not able to perform auto-negotiation |
| 1.2 | Link status | 0,RO/LL | Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface |
| 1.1 | Jabber detect | 0, RO/LH | Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9000A reset. This bit works only in 10Mbps mode |
| 1.0 | Extended capability | 1,RO/P | Extended Capability 1 = Extended register capable 0 = Basic register capable only |

8.3 PHY ID Identifier Register #1 (PHYID1) - 02



The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9000A. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

| Bit | Bit Name | Default | Description |
|----------|----------|---------|---|
| 2.15-2.0 | OUI_MSB | <0181h> | OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2) |

8.4 PHY ID Identifier Register #2 (PHYID2) - 03

| Bit | Bit Name | Default | Description |
|---------------|----------|-------------------|---|
| 3.15-3.1 0 | OUI_LSB | <101110>, RO/P | OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively |
| 3.9-3.4 | VNDR_MDL | <001010>, RO/P | Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9) |
| 3.3-3.0 | MDL_REV | <0000>, RO/P | Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4) |

8.5 Auto-negotiation Advertisement Register (ANAR) - 04

This register contains the advertised abilities of this DM9000A device as they will be transmitted to its link partner during Auto-negotiation.

| Bit | Bit Name | Default | Description |
|-----------|----------|---------|--|
| 4.15 | NP | 0,RO/P | Next page Indication 0 = No next page available 1 = Next page available The DM9000A has no next page, so this bit is permanently set to 0 |
| 4.14 | ACK | 0,RO | Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9000A's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit. |
| 4.13 | RF | 0, RW | Remote Fault 1 = Local device senses a fault condition 0 = No fault detected |
| 4.12-4.11 | Reserved | X, RW | Reserved Write as 0, ignore on read |
| 4.10 | FCS | 0, RW | Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability |
| 4.9 | T4 | 0, RO/P | 100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM9000A does not support 100BASE-T4 so this bit is permanently set to 0 |
| 4.8 | TX_FDX | 1, RW | 100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported |
| 4.7 | TX_HDX | 1, RW | 100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported |
| 4.6 | 10_FDX | 1, RW | 10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported |
| 4.5 | 10_HDX | 1, RW | 10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported |

| | | | |
|---------|----------|-------------|---|
| 4.4-4.0 | Selector | <00001>, RW | Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD |
|---------|----------|-------------|---|

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

| Bit | Bit Name | Default | Description |
|---------------|----------|---------|--|
| 5.15 | NP | 0, RO | Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available |
| 5.14 | ACK | 0, RO | Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9000A's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit |
| 5.13 | RF | 0, RO | Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner |
| 5.12-5.1 1 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 5.10 | FCS | 0, RO | Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner |
| 5.9 | T4 | 0, RO | 100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner |
| 5.8 | TX_FDX | 0, RO | 100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner |
| 5.7 | TX_HDX | 0, RO | 100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner |

| | | | |
|---------|----------|-------------|--|
| 5.6 | 10_FDX | 0, RO | 10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner |
| 5.5 | 10_HDX | 0, RO | 10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner |
| 5.4-5.0 | Selector | <00000>, RO | Protocol Selection Bits Link partner's binary encoded protocol selector |

8.7 Auto-negotiation Expansion Register (ANER)- 06

| Bit | Bit Name | Default | Description |
|----------|------------|----------|---|
| 6.15-6.5 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 6.4 | PDF | 0, RO/LH | Local Device Parallel Detection Fault PDF = 1: A fault detected via parallel detection function. PDF = 0: No fault detected via parallel detection function |
| 6.3 | LP_NP_ABLE | 0, RO | Link Partner Next Page Able LP_NP_ABLE = 1: Link partner, next page available LP_NP_ABLE = 0: Link partner, no next page |
| 6.2 | NP_ABLE | 0,RO/P | Local Device Next Page Able NP_ABLE = 1: DM9000A, next page available NP_ABLE = 0: DM9000A, no next page DM9000A does not support this function, so this bit is always 0 |
| 6.1 | PAGE_RX | 0, RO/LH | New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management |
| 6.0 | LP_AN_ABLE | 0, RO | Link Partner Auto-negotiation Able A "1" in this bit indicates that the link partner supports Auto-negotiation |

8.8 DAVICOM Specified Configuration Register (DSCR) - 16

| Bit | Bit Name | Default | Description |
|-------|----------|---------|--|
| 16.15 | BP_4B5B | 0,RW | Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation |
| 16.14 | BP_SCR | 0, RW | Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation |

| | | | |
|-------|------------|-------|--|
| 16.13 | BP_ALIGN | 0, RW | Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation |
| 16.12 | BP_ADPOK | 0, RW | BYPASS ADPOK Force signal detector (SD) active. This register is for debug only, not release to customer 1=Forced SD is OK, 0=Normal operation |
| 16.11 | Reserved | 0, RW | Reserved Force to 0 in application. |
| 16.10 | TX | 1, RW | 100BASE-TX Mode Control 1 = 100BASE-TX operation |
| 16.9 | Reserved | 0, RO | Reserved |
| 16.8 | Reserved | 0, RW | Reserved Force to 0 in application. |
| 16.7 | F_LINK_100 | 0, RW | Force Good Link in 100Mbps 0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes |
| 16.6 | SPLED_CTL | 0, RW | Reserved Force to 0 in application. |
| 16.5 | COLLED_CTL | 0, RW | Reserved Force to 0 in application. |
| 16.4 | RPDCTR-EN | 1, RW | Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 0 = Disable automatic reduced power down 1 = Enable automatic reduced power down |
| 16.3 | SMRST | 0, RW | Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed |
| 16.2 | MFPS | 1, RW | MF Preamble Suppression Control Frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off |
| 16.1 | SLEEP | 0, RW | Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock |



| | | | |
|------|-------|-------|--|
| | | | generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset |
| 16.0 | RLOUT | 0, RW | Remote Loopout Control When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing |

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) - 17

| Bit | Bit Name | Default | Description |
|------------|--------------|--------------|--|
| 17.15 | 100FDX | 1, RO | 100M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode |
| 17.14 | 100HDX | 1, RO | 100M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode |
| 17.13 | 10FDX | 1, RO | 10M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode |
| 17.12 | 10HDX | 1, RO | 10M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode |
| 17.11-17.9 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 17.8-17.4 | PHYADR [4:0] | (PHYADR), RW | PHY Address Bit 4:0 The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY |
| 17.3-17.0 | ANMB[3:0] | 0, RO | Auto-negotiation Monitor Bits These bits are for debug only. The auto-negotiation status will be |

| | | | written to these bits. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----|----|----|---|---|----|----|----|--|---|---|---|---|---------------|---|---|---|---|---------------|---|---|---|---|-------------------|---|---|---|---|------------------------|---|---|---|---|-------------------|---|---|---|---|------------------------|---|---|---|---|------------------------------------|---|---|---|---|---|
| | | | <table border="1"> <thead> <tr> <th>B3</th> <th>b2</th> <th>b1</th> <th>B0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>In IDLE state</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Ability match</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Acknowledge match</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Acknowledge match fail</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>Consistency match</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>Consistency match fail</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Parallel detects signal_link_ready</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Parallel detects signal_link_ready fail</td> </tr> </tbody> </table> | B3 | b2 | b1 | B0 | | 0 | 0 | 0 | 0 | In IDLE state | 0 | 0 | 0 | 1 | Ability match | 0 | 0 | 1 | 0 | Acknowledge match | 0 | 0 | 1 | 1 | Acknowledge match fail | 0 | 1 | 0 | 0 | Consistency match | 0 | 1 | 0 | 1 | Consistency match fail | 0 | 1 | 1 | 0 | Parallel detects signal_link_ready | 0 | 1 | 1 | 1 | Parallel detects signal_link_ready fail |
| B3 | b2 | b1 | B0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | In IDLE state | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | Ability match | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | Acknowledge match | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | Acknowledge match fail | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | Consistency match | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | Consistency match fail | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | Parallel detects signal_link_ready | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | Parallel detects signal_link_ready fail | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.10 10BASE-T Configuration/Status (10BTCSR) - 18

| Bit | Bit Name | Default | Description |
|-----------|----------|---------|---|
| 18.15 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 18.14 | LP_EN | 1, RW | Link Pulse Enable 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation |
| 18.13 | HBE | 1, RW | Heartbeat Enable 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DM9000A is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode) |
| 18.12 | SQUELCH | 1, RW | Squelch Enable 1 = Normal squelch 0 = Low squelch |
| 18.11 | JABEN | 1, RW | Jabber Enable Enables or disables the Jabber function when the DM9000A is in 10BASE-T full duplex or 10BASE-T transceiver Loopback mode 1 = Jabber function enabled 0 = Jabber function disabled |
| 18.10 | Reserved | 0, RW | Reserved Force to 0, in application. |
| 18.9-18.1 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 18.0 | POLR | 0, RO | Polarity Reversed |

| | | | |
|--|--|--|--|
| | | | When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module |
|--|--|--|--|

8.11 Power Down Control Register (PWDOR) - 19

| Bit | Bit Name | Default | Description |
|------------|----------|---------|--|
| 19.15-19.9 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 19.8 | PD10DRV | 0, RW | Vendor power down control test |
| 19.7 | PD100DL | 0, RW | Vendor power down control test |
| 19.6 | PDchip | 0, RW | Vendor power down control test |
| 19.5 | PDcom | 0, RW | Vendor power down control test |
| 19.4 | PDaeq | 0, RW | Vendor power down control test |
| 19.3 | PDdrv | 0, RW | Vendor power down control test |
| 19.2 | PDedi | 0, RW | Vendor power down control test |
| 19.1 | PDedo | 0, RW | Vendor power down control test |
| 19.0 | PD10 | 0, RW | Vendor power down control test |

* when selected, the power down value is control by Register 20.0

8.12 (Specified config) Register – 20

| Bit | Bit Name | Default | Description |
|------------|----------------|--------------|---|
| 20.15 | TSTSE1 | 0,RW | Vendor test select control |
| 20.14 | TSTSE2 | 0,RW | Vendor test select control |
| 20.13 | FORCE_TXSD | 0,RW | Force Signal Detect 1: force SD signal OK in 100M 0: normal SD signal. |
| 20.12 | FORCE_FEF | 0,RW | Vendor test select control |
| 20.11-20.8 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 20.7 | MDIX_CNTL | MDI/MDIX, RO | The polarity of MDI/MDIX value 1: MDIX mode 0: MDI mode |
| 20.6 | AutoNeg_lpbk | 0,RW | Auto-negotiation Loopback 1: test internal digital auto-negotiation Loopback 0: normal. |
| 20.5 | Mdix_fix Value | 0, RW | MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value. |
| 20.4 | Mdix_down | 0,RW | AUTO-MDIX Down |



DM9000A

Ethernet Controller with General Processor Interface

| | | | |
|------|----------|------|---|
| | | | Manual force MDI/MDIX. 0: Enable AUTO-MDIX 1: Disable AUTO-MDIX , MDIX_CNTL value depend on 20.5 |
| 20.3 | MonSel1 | 0,RW | Vendor monitor select |
| 20.2 | MonSel0 | 0,RW | Vendor monitor select |
| 20.1 | Reserved | 0,RW | Reserved Force to 0, in application. |
| 20.0 | PD_value | 0,RW | Power down control value Decision the value of each field Register 19. 1: power down 0: normal |

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9. Functional Description

9.1 Host Interface

The host interface is a general processor local bus that using chip select (pin CS#) to access DM9000A. Pin CS# is default low active which can be re-defined by EEPROM setting.

There are only two addressing ports through the access of the host interface. One port is the INDEX port and the other is the DATA port. The INDEX port is decoded by the pin $CMD = 0$ and the DATA port by the pin $CMD = 1$. The contents of the INDEX port are the register address of the DATA port. Before the access of any register, the address of the register must be saved in the INDEX port.

9.2 Direct Memory Access Control

The DM9000A provides DMA capability to simplify the access of the internal memory. After the programming of the starting address of the internal memory and then issuing a dummy read/write command to load the current data to internal data buffer, the desired location of the internal memory can be accessed by the read/write command registers. The memory's address will be increased with the size that equals to the current operation mode (i.e. the 8-bit or 16-bit mode) and the data of the next location will be loaded into internal data buffer automatically. It is noted that the data of the first access (the dummy read/write command) in a sequential burst should be ignored because that the data was the contents of the last read/write command.

The internal memory size is 16K bytes. The first location of 3K bytes is used for the data buffer of the packet transmission. The other 13K bytes are used for the buffer of the receiving packets. So in the write memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0 if the end of address (i.e. 3K) is reached. In a similar way, in the read memory operation, when the bit 7 of

IMR is set, the memory address increment will wrap to location 0x0C00 if the end of address (i.e. 16K) is reached.

9.3 Packet Transmission

There are two packets, sequentially named as index I and index II, can be stored in the TX SRAM at the same time. The index register 02h controls the insertion of CRC and pads. Their statuses are recorded at index registers 03h and 04h respectively.

The start address of transmission is 00h and the current packet is index I after software or hardware reset. Firstly write data to the TX SRAM using the DMA port and then write the byte count to byte_count register at index register 0fch and 0fdh. Set the bit 1 of control register. The DM9000A starts to transmit the index I packet. Before the transmission of the index I packet ends, the data of the next (index II) packet can be moved to TX SRAM. After the index I packet ends the transmission, write the byte count data of the index II to BYTE_COUNT register and then set the bit 1 of control register to transmit the index II packet. The following packets, named index I, II, I, II, ..., use the same way to be transmitted.

9.4 Packet Reception

The RX SRAM is a ring data structure. The start address of RX SRAM is 0C00h after software or hardware reset. Each packet has a 4-byte header followed with the data of the reception packet which CRC field is included. The format of the 4-byte header is 01h, status, BYTE_COUNT low, and BYTE_COUNT high. It is noted that the start address of each packet is in the proper address boundary which depends on the operation mode (the 8-bit or 16-bit).

9.5 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.5.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9000A includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters which do not require 4B5B conversion.

9.5.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.5.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block.

9.5.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

9.5.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic one event.

9.5.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.5.7 4B5B Code Group

| Symbol | Meaning | 4B code 3210 | 5B Code 43210 |
|--------|---------|-----------------|------------------|
| 0 | Data 0 | 0000 | 11110 |
| 1 | Data 1 | 0001 | 01001 |
| 2 | Data 2 | 0010 | 10100 |
| 3 | Data 3 | 0011 | 10101 |
| 4 | Data 4 | 0100 | 01010 |
| 5 | Data 5 | 0101 | 01011 |
| 6 | Data 6 | 0110 | 01110 |
| 7 | Data 7 | 0111 | 01111 |
| 8 | Data 8 | 1000 | 10010 |
| 9 | Data 9 | 1001 | 10011 |
| A | Data A | 1010 | 10110 |
| B | Data B | 1011 | 10111 |
| C | Data C | 1100 | 11010 |
| D | Data D | 1101 | 11011 |
| E | Data E | 1110 | 11100 |
| F | Data F | 1111 | 11101 |
| I | Idle | undefined | 11111 |
| J | SFD (1) | 0101 | 11000 |
| K | SFD (2) | 0101 | 10001 |
| T | ESD (1) | undefined | 01101 |
| R | ESD (2) | undefined | 00111 |
| H | Error | undefined | 00100 |
| V | Invalid | undefined | 00000 |
| V | Invalid | undefined | 00001 |
| V | Invalid | undefined | 00010 |
| V | Invalid | undefined | 00011 |
| V | Invalid | undefined | 00101 |
| V | Invalid | undefined | 00110 |
| V | Invalid | undefined | 01000 |
| V | Invalid | undefined | 01100 |
| V | Invalid | undefined | 10000 |
| V | Invalid | undefined | 11001 |

Table 1

9.6 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.

The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.6.1 Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.6.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.6.3 MLT-3 to NRZI Decoder

The DM9000A decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.6.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125Mhz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.6.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.6.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.6.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.6.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

9.6.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.7 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9000A is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.8 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.9 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during receive operations.

9.10 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

9.11 Power Reduced Mode

The Signal detect circuit is always turned to monitor whether there is any signal on the media (cable disconnected). The DM9000A automatically turns off the power and enters the Power Reduced mode, whether its operation mode is N-way or force mode. When enters the Power Reduced mode, the transmit circuit still sends out fast link pulses with minimum power consumption. If a valid signal is detected from the media, which might be N-ways fast link pulses, 10Base-T normal link pulses, or 100Base-TX MLT3 signals, the device will wake up and resume a normal operation mode.

That can be writing Zero to PHY Reg. 16.4 to disable Power Reduced mode.

9.11.1 Power Down Mode

The PHY Reg.0.11 can be set high to enter the Power Down mode, which disables all transmit and receive functions, except the access of PHY registers.

9.11.2 Reduced Transmit Power Mode

The additional Transmit power reduction can be gained by designing with 1.25:1 turns ration magnetic on its TX side and using a 8.5K resistor on BGRES and AGND pins, and the TXO+/TXO- pulled high resistors should be changed from 50 to 78 . This configuration could be reduced about 20% transmit power.

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10. DC and AC Electrical Characteristics

10.1 Absolute Maximum Ratings (25°C)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|--------|---|------|------|------|------------|
| DVDD | Supply Voltage | -0.3 | 3.6 | V | |
| VIN | DC Input Voltage (VIN) | -0.5 | 5.5 | V | |
| VOUT | DC Output Voltage(VOUT) | -0.3 | 3.6 | V | |
| Tstg | Storage Temperature range | -65 | +150 | | |
| TC | Case Temperature | 0 | +85 | | asTA : 70 |
| TA | Ambient Temperature | 0 | +70 | | |
| LT | Lead Temperature (TL,soldering,10 sec.). | - | +235 | | |

10.1.1 Operating Conditions

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---------------------------|-----------------------------------|-------|-------|------|------------|
| DVDD | Supply Voltage | 3.135 | 3.465 | V | |
| Tc | Case <small>Reserve</small> | --- | 85 | °C | |
| PD (Power Dissipation) | 100BASE-TX | --- | 87 | mA | 3.3V |
| | 10BASE-T TX (100% utilization) | --- | 92 | mA | 3.3V |
| | 10BASE-T idle | --- | 38 | mA | 3.3V |
| | Auto-negotiation | --- | 56 | mA | 3.3V |
| | Power Reduced Mode(without cable) | --- | 31 | mA | 3.3V |
| | Power Down Mode | --- | 21 | mA | 3.3V |

10.2 DC Electrical Characteristics (VDD = 3.3V)

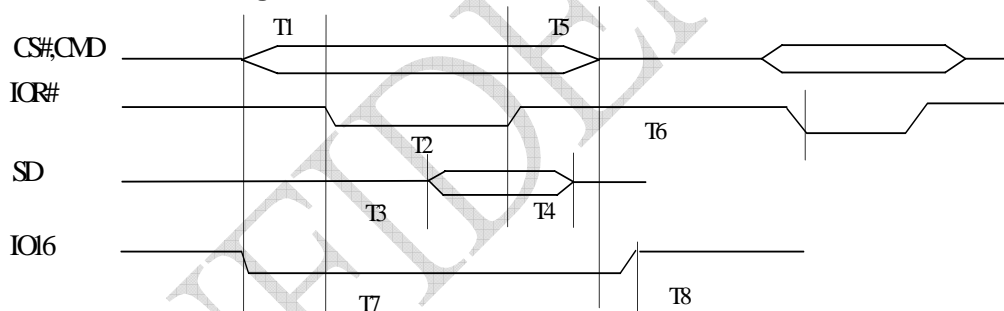
| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|--------------------|--------------------------------------|------|------|------|------|--------------------------|
| Inputs | | | | | | |
| VIL | Input Low Voltage | - | - | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | - | - | V | |
| IIL | Input Low Leakage Current | -1 | - | - | uA | VIN = 0.0V |
| IiH | Input High Leakage Current | - | - | 1 | uA | VIN = 3.3V |
| Outputs | | | | | | |
| VOL | Output Low Voltage | - | - | 0.4 | V | IOL = 4mA |
| VOH | Output High Voltage | 2.4 | - | - | V | IOH = -4mA |
| Receiver | | | | | | |
| VICM | RX+/RX- Common Mode Input Voltage | - | 2.5 | - | V | 100 Ω Termination Across |
| Transmitter | | | | | | |
| VTD100 | 100TX+/- Differential Output Voltage | 1.9 | 2.0 | 2.1 | V | Peak to Peak |
| VTD10 | 10TX+/- Differential Output Voltage | 4.4 | 5 | 5.6 | V | Peak to Peak |
| ITD100 | 100TX+/- Differential Output Current | 19 | 20 | 21 | mA | Absolute Value |
| ITD10 | 10TX+/- Differential Output Current | 44 | 50 | 56 | mA | Absolute Value |

10.3 AC Electrical Characteristics & Timing Waveforms
10.3.1 TP Interface

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|-------------------|--|------|------|------|------|------------|
| t _{TR/F} | 100TX+/- Differential Rise/Fall Time | 3.0 | - | 5.0 | ns | |
| t _{TM} | 100TX+/- Differential Rise/Fall Time Mismatch | 0 | - | 0.5 | ns | |
| t _{TDC} | 100TX+/- Differential Output Duty Cycle Distortion | 0 | - | 0.5 | ns | |
| T _{t/T} | 100TX+/- Differential Output Peak-to-Peak Jitter | 0 | - | 1.4 | ns | |
| XOST | 100TX+/- Differential Voltage Overshoot | 0 | - | 5 | % | |

10.3.2 Oscillator/Crystal Timing

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|------------------|----------------------|--------|------|--------|------|------------|
| T _{CKC} | OSC Clock Cycle | 39.998 | 40 | 40.002 | ns | 50ppm |
| TP _{WH} | OSC Pulse Width High | 16 | 20 | 24 | ns | |
| TP _{WL} | OSC Pulse Width Low | 16 | 20 | 24 | ns | |

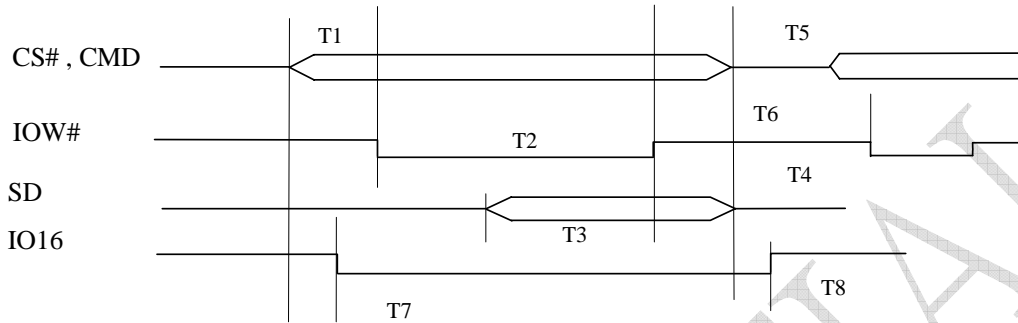
10.3.3 Processor I/O Read Timing


| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|--|------|------|------|------|
| T1 | CS#,CMD valid to IOR# valid | 0 | | | ns |
| T2 | IOR# width | 10 | | | ns |
| T3 | System Data(SD) Delay time | | | 3 | ns |
| T4 | IOR# invalid to System Data(SD) invalid | | | 3 | ns |
| T5 | IOR# invalid to CS#,CMD invalid | 0 | | | ns |
| T6 | IOR# invalid to next IOR#/IOW# valid When read DM9000A register | 2 | | | clk* |
| T6 | IOR# invalid to next IOR#/IOW# valid When read DM9000A memory with F0h register | 4 | | | clk* |
| T2+T6 | IOR# invalid to next IOR#/IOW# valid When read DM9000A memory with F2h register | 1 | | | clk* |
| T7 | CS#,CMD valid to IO16 valid | | | 3 | ns |
| T8 | CS#,CMD invalid to IO16 invalid | | | 3 | ns |

***Note : (the default clk period is 20ns)**

1. The IO16 is valid when the SD bus width is 16-bit and the system address is DATA port (i.e. CMD is

high) and the value of INDEX port is memory data register index. (ex. F0H, F2H, F6H or F8H)

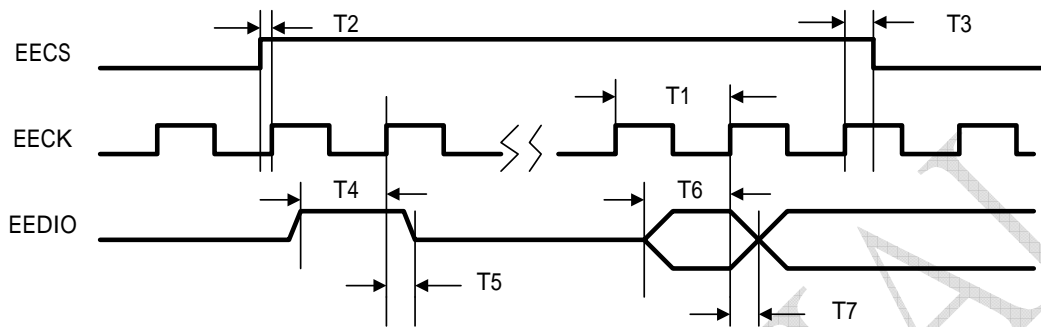
10.3.4 Processor I/O Write Timing


| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|---|------|------|------|------|
| T1 | CS#,CMD valid to IOW# valid | 0 | | | ns |
| T2 | IOW# Width | 10 | | | ns |
| T3 | System Data(SD) Setup Time | 10 | | | ns |
| T4 | System Data(SD) Hold Time | 3 | | | ns |
| T5 | IOW# Invalid to CS#,CMD Invalid | 0 | | | ns |
| T6 | IOW# Invalid to next IOW#/IOR# valid When write DM9000A INDEX port | 1 | | | clk* |
| T6 | IOW# Invalid to next IOW#/IOR# valid When write DM9000A DATA port | 2 | | | clk* |
| T2+T6 | IOW# Invalid to next IOW#/IOR# valid When write DM9000A memory | 1 | | | clk* |
| T7 | CS#,CMD Valid to IO16 valid | | | 3 | ns |
| T8 | CS#,CMD Invalid to IO16 Invalid | | | 3 | ns |

Note : (the default clk period is 20ns)

1. The IO16 is valid when the SD bus width is 16-bit and system address is DATA port (i.e. CMD is high) and the value of INDEX port is memory data

register index (ex. F0H, F2H, F6H or F8H)

10.3.5 EEPROM Interface Timing


| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|------------------------------|------|-------|------|------|
| T1 | EECK Frequency | | 0.375 | | Mhz |
| T2 | EECS Setup Time | | 500 | | ns |
| T3 | EECS Hold Time | | 2166 | | ns |
| T4 | EEDIO Setup Time when output | | 480 | | ns |
| T5 | EEDIO Hold Time when output | | 2200 | | ns |
| T6 | EEDIO Setup Time when input | 8 | | | ns |
| T7 | EEDIO Hold Time when input | 8 | | | ns |

11. Application Notes

11.1 Network Interface Signal Routing

Place the transformer as close as possible to the RJ-45 connector. Place all the 50 Ω resistors as close as possible to the DM9000A RXI± and TXO± pins. Traces routed from RXI± and TXO± to the transformer should run in close pairs directly to the transformer. The designer should be careful not to cross the transmit and receive pairs. As always, vias should be avoided as much as possible. The network interface should be void of any signals other than the TXO± and RXI± pairs between the RJ-45 to the transformer and the transformer to the DM9000A. There should be no power or ground planes in the area under the

network side of the transformer to include the area under the RJ-45 connector. (Refer to Figure 11-4 and 11-5) Keep chassis ground away from all active signals. The RJ-45 connector and any unused pins should be tied to chassis ground through a resistor divider network and a 2KV bypass capacitor.

The Band Gap resistor should be placed as physically close as pins 1 and 48 as possible (refer to Figure 11-1 and 11-2). The designer should not run any high-speed signal near the Band Gap resistor placement.

11.2 10Base-T/100Base-TX Auto MDIX Application

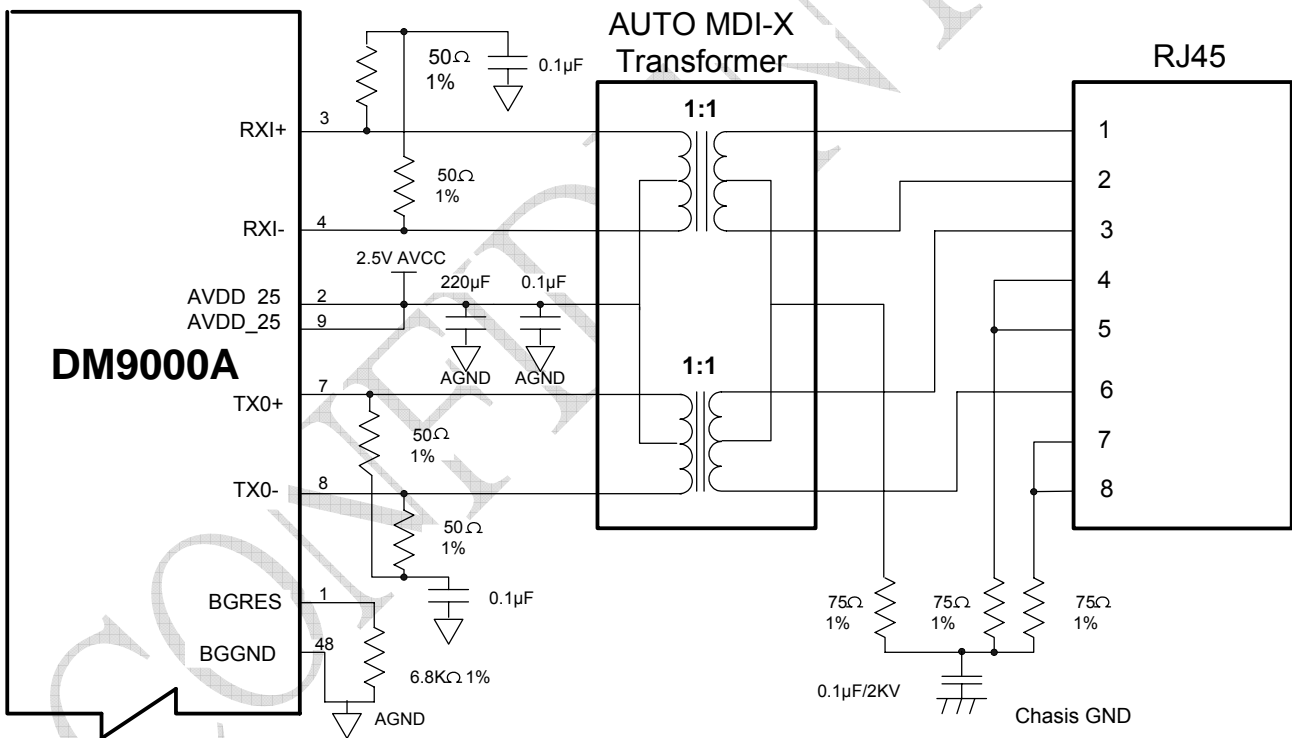


Figure 11-1 Auto MDIX Application

11.3 10Base-T/100Base-TX (Non Auto MDIX Transformer Application)

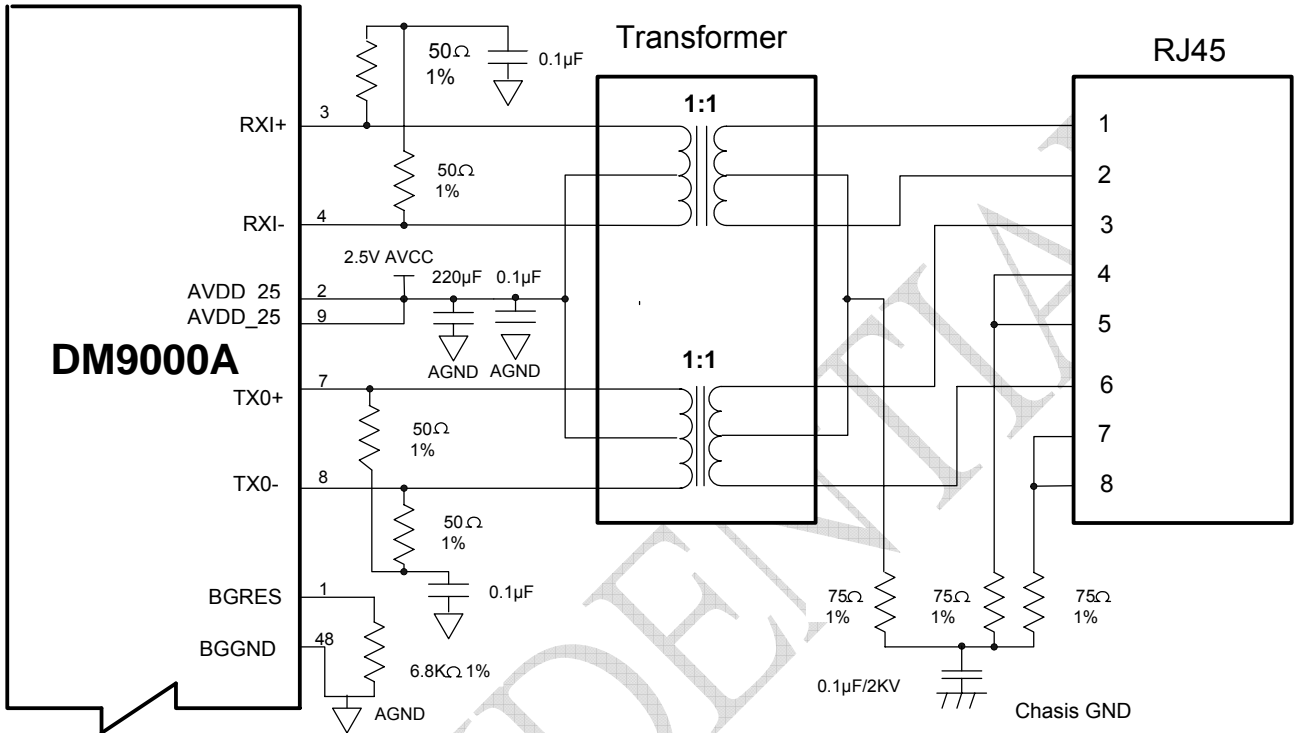
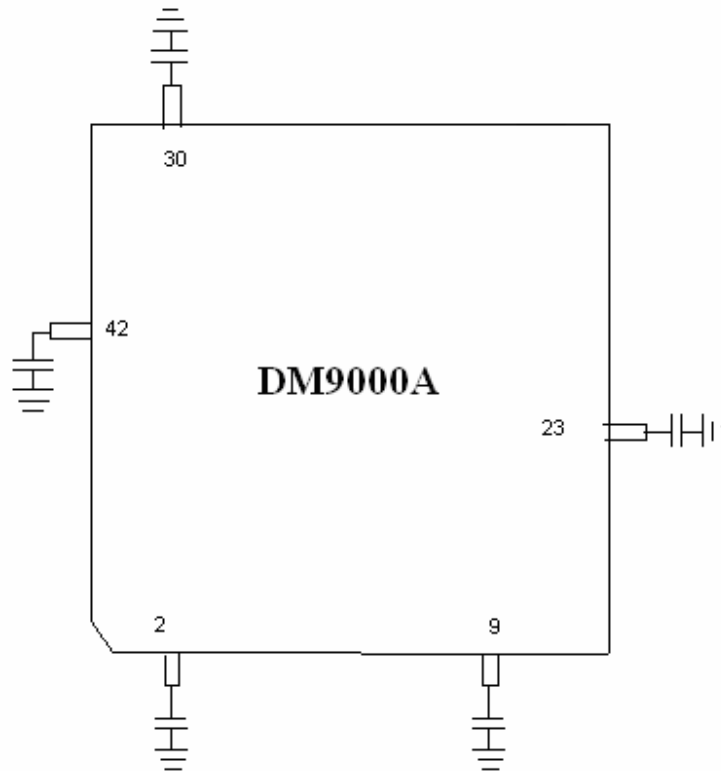


Figure 11-2 Non Auto MDIX Transformer Application

11.4 Power Decoupling Capacitors

Davicom Semiconductor recommends placing all the decoupling capacitors for all power supply pins as close as possible to the power pads of the DM9000A (The best placed distance is < 3mm from pin). The recommended decoupling capacitor is 0.1 μ F or 0.01 μ F, as required by the design layout.

**Figure 11-3 Power Decoupling Capacitors**

11.5 Ground Plane Layout

Davicom Semiconductor recommends a single ground plane approach to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface card not comply with specific FCC

regulations (part 15). Figure 11-4 shows a recommended ground layout scheme.

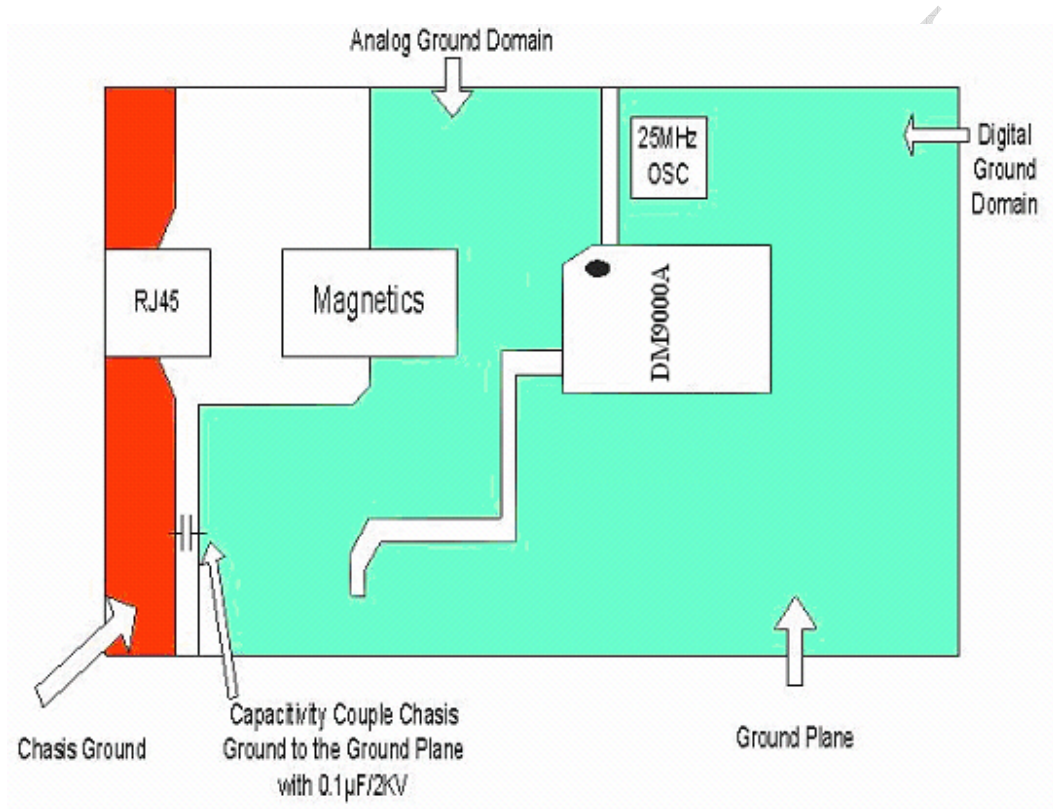


Figure 11-4 Ground Plane Layout

11.6 Power Plane Partitioning

The power planes should be approximately illustrated in Figure 11-5.

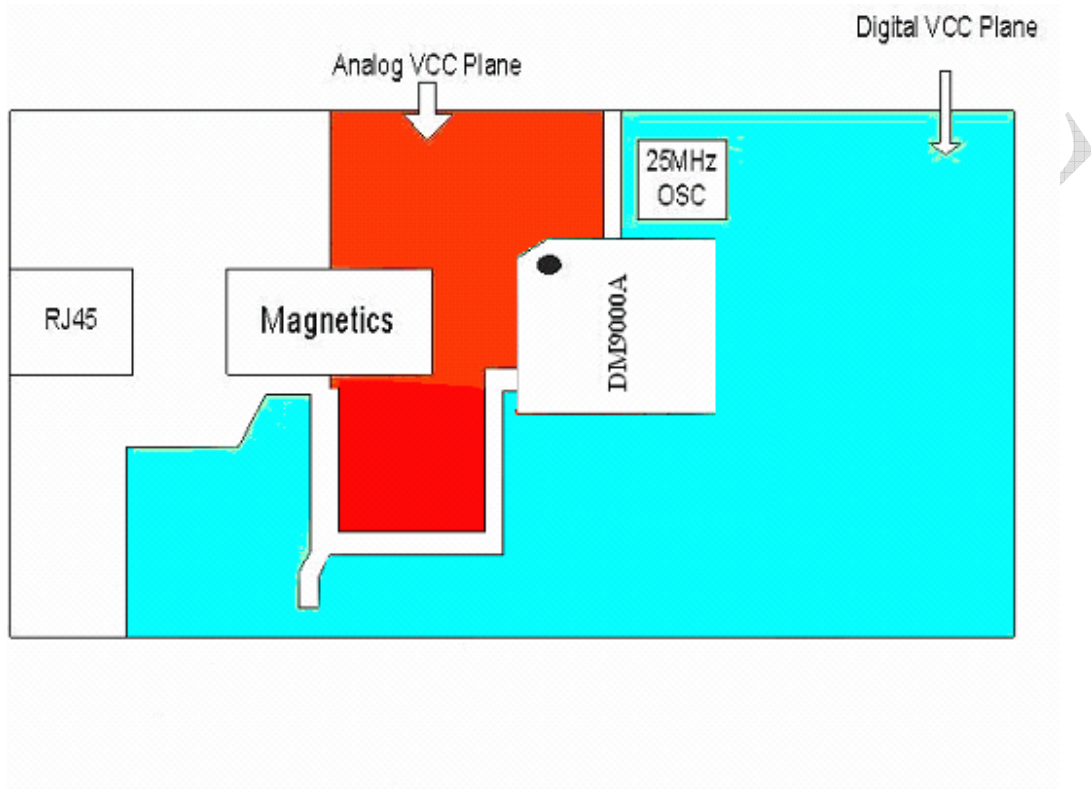


Figure 11-5 Power Plane Partitioning

11.7 Magnetics Selection Guide

Refer to Table 2 for transformer requirements. Transformers, meeting these requirements, are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics

before using them in an application. The transformers listed in Table 2 are electrical equivalents, but may not be pin-to-pin equivalents.

| Manufacturer | Part Number |
|--------------------------|--|
| Pulse Engineering | PE-68515, H1078, H1012, H1102 |
| Delta | LF8200, LF8221x |
| YCL | 20PMT04, 20PMT05, PH163112, YCL 0303 PH163539 *(Auto MDIX) |
| Halo | TG22-3506ND, TD22-3506G1, TG22-S010ND, TG22-S012ND TG110-S050N2 |
| Nano Pulse Inc. | NPI 6181-37, NPI 6120-30, NPI 6120-37 NPI 6170-30 |
| Fil-Mag | PT41715 |
| Bel Fuse | S558-5999-01, S558-5999-W2 |
| Valor | ST6114, ST6118 |
| Macronics | HS2123, HS2213 |
| Bothhand | TS6121C, 16ST8515, 16ST1086 |

Table 2

11.8 Crystal Selection Guide

A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, and series-resonant.

Connects to pins X1 and X2, and shunts each crystal lead to ground with a 22pf capacitor (see figure 11-6).

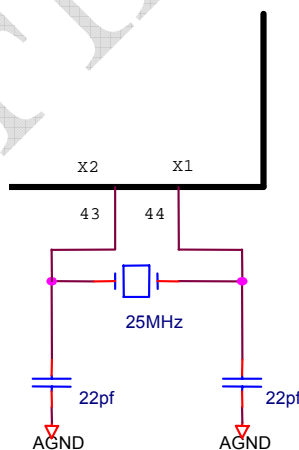
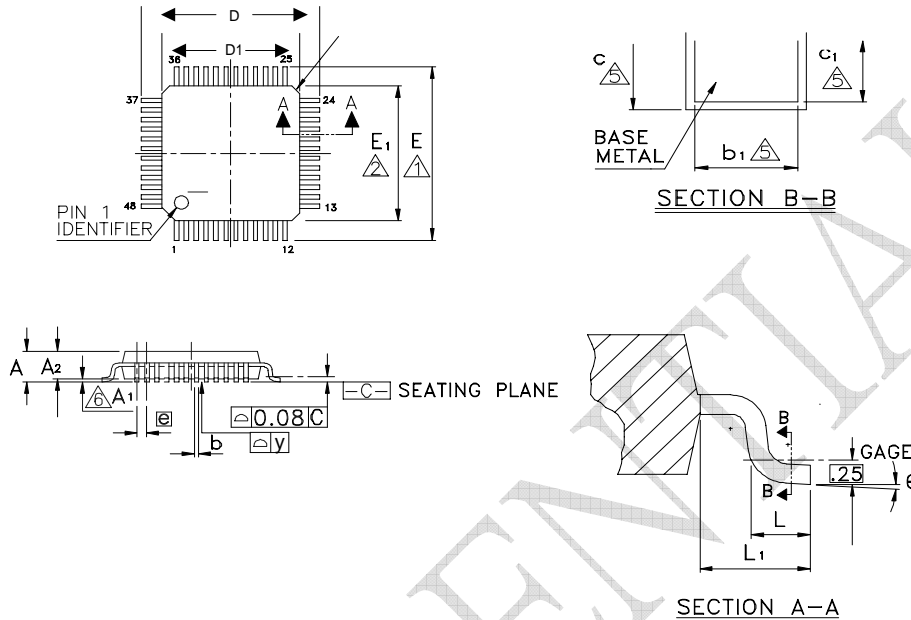


Figure 11-6
Crystal Circuit Diagram

12. Package Information
LQFP 48L (F.P. 2mm) Outline Dimensions

unit: inches/mm



| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|----------------------|-------|-------|------------------|------|------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | - | - | 0.063 | - | - | 1.60 |
| A1 | 0.002 | - | 0.006 | 0.05 | - | 0.15 |
| A2 | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| b1 | 0.007 | 0.008 | 0.009 | 0.17 | 0.20 | 0.23 |
| C | 0.004 | - | 0.008 | 0.09 | - | 0.20 |
| C1 | 0.004 | - | 0.006 | 0.09 | - | 0.16 |
| D | 0.354BSC | | | 9.00BSC | | |
| D1 | 0.276BSC | | | 7.00BSC | | |
| E | 0.354BSC | | | 9.00BSC | | |
| E1 | 0.276BSC | | | 7.00BSC | | |
| e | 0.020BSC | | | 0.50BSC | | |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| | 0-12° | | | 0-12° | | |

| | | |
|----|----------|---------|
| L1 | 0.039REF | 1.00REF |
| y | 0.003MAX | 0.08MAX |

Notes:

- To be determined at seating plane.
- Dimensions D1 and E 1do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
- Dimensions b does not include dambar protrusion. Total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
- Exact shape of each corner is optional.
- These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
- A1 is defined as the distance from the seating plane to the lowest point of the package body.
- Controlling dimension: millimeter.
- Reference documents: JEDEC MS-026, BBC.



13. Ordering Information

| Part Number | Pin Count | Package |
|-------------|-----------|-------------------|
| DM9000AE | 48 | LQFP |
| DM9000AEP | 48 | LQFP (Pb-Free) |

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.