DAVICOM Semiconductor, Inc.

DM9003

10/100 Mbps 2-port Ethernet Switch Controller

with General Processor Interface

DATA SHEET

Preliminary

Version: DM9003-DS-P04

May 15, 2008

CONTENT

1. GENERAL DESCRIPTION

The DM9003 is a fully integrated, high-performance, and cost-effective Fast Ethernet switch controller with one general processor bus interface, two port 10M/100Mbps PHYs.

The general processor bus connects directly to internal host MAC with 8-bit or 16-bit data to access internal memory. The host MAC has the similar functions as other 10M/100Mbps MAC do. This makes the DM9003 to act as an extended three port switch and to shorten the latency from processor port to destination port.

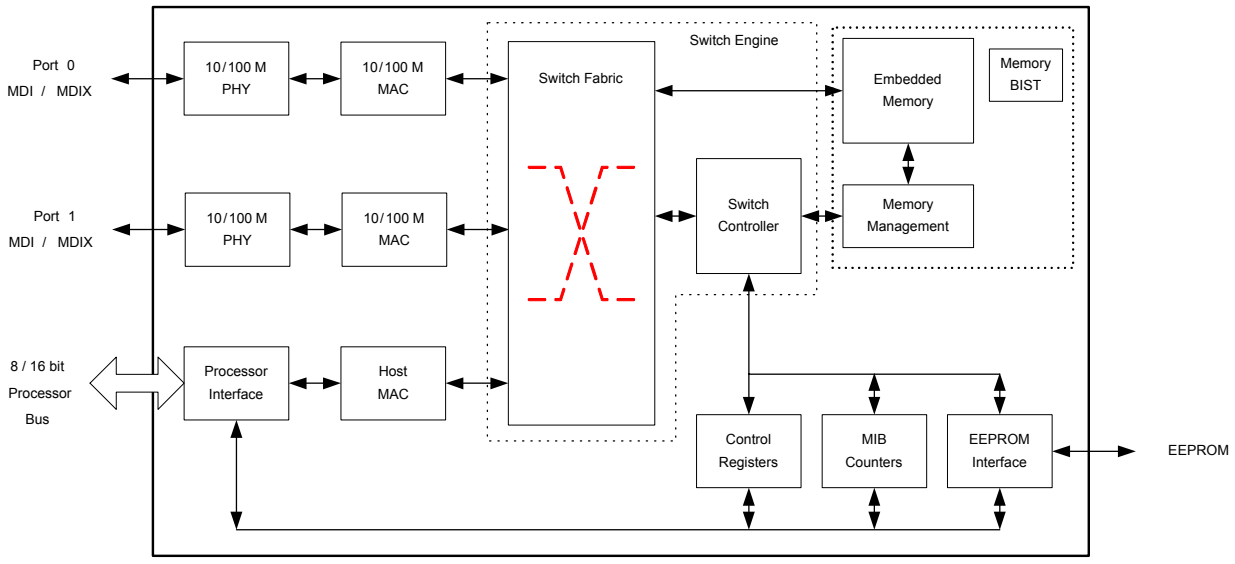
The internal memory of the DM9003 supports up to 1K uni-cast MAC address table, and serves two ports' and processor port's transmit and receive buffers. For efficient memory usage algorithm, total 48KB memory is shared with two ports and processor port by link list data structure.

Each port of the DM9003 provides four priorities transmit queues, which can be defined as port-based, 802.1p VLAN, or IP packet ToS field, to fit the various bandwidth and latency requirement of data, voice, and video applications. Each port also supports ingress and/or egress rate control to provide proper bandwidth. And up to 16 groups of 802.1Q VLAN with Tag/Un-tag functions are supported to provide efficient packet forwarding.

The TCP/UDP/IPv4 checksum generation and checking functions are also provided by processor port to offload the processor's computing load. In addition to the packet transmit and receive functions, the processor port also provides various registers to control and get status of the DM9003's operation. Each port, including the processor port, provides the MIB counters, loop-back capability and the memory Build-in Self Test (BIST) for system and board level diagnostic.

The integrated two ports PHY are compliant with IEEE 802.3u standards and supports *HP* Auto-MDIX capabilities for twisted-pair cable transmit/receive direction automatic switching.

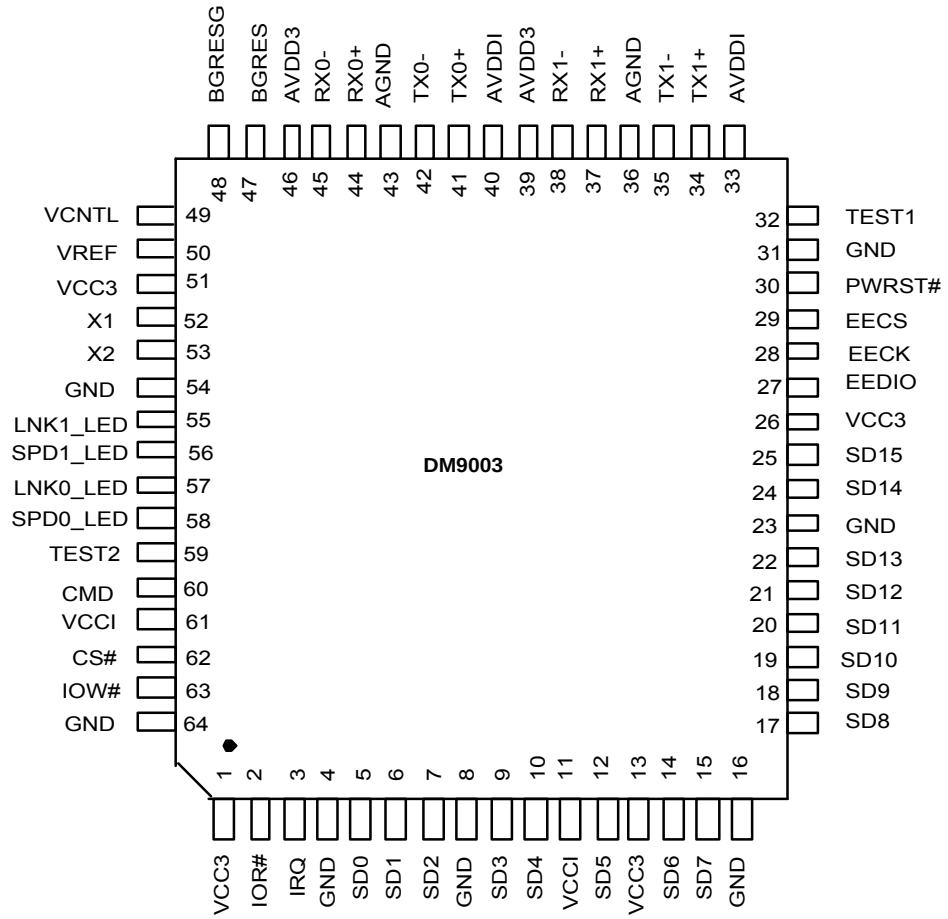
2. BLOCK DIAGRAM



3. FEATURES

- Ethernet Switch with two 10/100Mbps PHYs and general processor bus interface
- Processor bus slave architecture
- EEPROM interface for power-up configuration
- TCP/UDP/IPv4 checksum offload
- Support *HP* Auto-MDIX
- IEEE 802.3x Flow Control in Full-duplex mode
- Back Pressure Flow Control in Half-duplex mode
- Each port supports 4 priority queues by Port-based, 802.1P QoS, and IP TOS priority
- Support 802.1Q VLAN up to 16 VLAN groups
- Support VLAN ID tag/untag option
- Each port supports bandwidth, ingress and egress rate control
- Support Broadcast Storming filter function
- Support Store and Forward switching approach
- Support up to 1K uni-cast MAC addresses
- Automatic aging scheme
- Support MIB counters for diagnostic
- uP data driving capability adjustable
- 64-pin LQFP 1.8V internal core, 3.3V I/O with 5V tolerant

4. Pin Configuration : 64 pin LQFP



5. PIN DESCRIPTION

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power, PD=internal pull-low (approx. 50K ohm)
# = asserted Low

5.1 Processor Bus interface

Pin No.	Pin Name	I/O	Description
2	IOR#	I	Processor Read Command Default is low active. The polarity can be changed by setting EEPROM.
3	IRQ	O	Interrupt Request Default is high active and non-open collector type. Its polarity and output type can be changed by strap pins or EEPROM setting.
5,6,7,9,10,12,14,15, 17,18,19,20,21,22,24,25	SD0~15	I/O	Processor Data Bus bit 0~15
60	CMD	I	Command Type Upon the IO transaction, when CMD is high, SD0~15 reflect the value of DATA port when CMD is low, SD0~15 reflect the value of INDEX port
62	CS#	I	Processor Chip Select Command Default is low active. Its polarity can be changed by EEPROM setting.
63	IOW#	I	Processor Write Command Default is low active. Its polarity can be changed by EEPROM setting.

5.2 EEPROM Interfaces

Pin No.	Pin Name	I/O	Description
27	EEDIO	I,/O	EEPROM Data In/Out
28	EECK	O,PD	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer.
29	EECS	O,PD	EEPROM Chip Selection.

5.3 LED Pins

Pin No.	Pin Name	I/O	Description
55	LNK1_LED	O/D	Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the port 1.
56	SPD1_LED	O/D	Port 1 Speed LED It's low to indicate that the port 1 operates in 100M mode. It's floating to indicate that the port 1 operates in 10M mode.
57	LNK0_LED	O/D	Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the port 0.
58	SPD0_LED	O/D	Port 0 Speed LED It's low to indicate that the port 0 operates in 100M mode. It's floating to indicate that the port 0 operates in 10M mode.

5.4 Clock Interface

Pin No.	Pin Name	I/O	Description
52	X1	I	Crystal 25MHz In
53	X2	O	Crystal 25MHz Out

5.5 Network Interface

Pin No.	Pin Name	I/O	Description
34,35	TX1+/-	I/O	Port 1 TP TX These two pins are the transmit output in MDI mode or the receive input in MDIX mode.
37,38	RX1+/-	I/O	Port 1 TP RX These two pins are the receive input in MDI mode or the transmit output in MDIX mode.
41,42	TX0+/-	I/O	Port 0 TP TX These two pins are the transmit output in MDI mode or the receive input in MDIX mode.
44,45	RX0+/-	I/O	Port 0 TP RX These two pins are the receive input in MDI mode or the transmit output in MDIX mode.
47	BGRES	I/O	Band gap Pin Connect a 1.4Kohm ±1% resistor to BGRESG in application.
48	BGRESG	P	Band gap Ground
49	VCNTL	I/O	1.8V Voltage control
50	VREF	O	Voltage Reference Connect a 0.1uF capacitor to ground in application.

5.6 Miscellaneous Pins

Pin No.	Pin Name	I/O	Description
30	PWRST#	I	Power-on Reset Low active with minimum 1ms
32	TEST1	I,PD	Tie to ground in application
59	TEST2	I,PD	Tie to ground in application

5.7 Power Pins

Pin No.	Pin Name	I/O	Description
1,13,26,51	VCC3	P	Digital 3.3V
11,61	VCCI	P	Internal 1.8V core power
4,8,16,23,31,54,64	GND	P	Digital GND
39,46	AVDD3	P	Analog 3.3V power
33,40	AVDDI	P	Analog 1.8V power
36,43	AGND	P	Analog GND

5.8 Strap pins table

1: pull-high 1K~10K, 0: floating (default).

Pin No.	Pin Name	Description
28	EECK	Processor Data Bus Width 0: 16-bit, SD 0-15 is used as processor data bus (default) 1: 8-bit, SD 0-7 is used as processor data bus; SD 8-15 is left floating.
29	EECS	Polarity of IRQ 0: IRQ pin high active (default) 1: IRQ pin low active

6. CONTROL AND STATUS REGISTER SET

The DM9003 implements several control and status registers (CSR), which can be accessed by the host.

All CSR are set to their default values by power on or software reset unless specified.

Register	Description	Offset	Default value after reset
NCR	Network Control Register	00H	00H
NSR	Network Status Register	01H	00H
TCR	TX Control Register	02H	00H
RCR	RX Control Register	05H	00H
RSR	RX Status Register	06H	00H
ROCR	Receive Overflow Counter Register	07H	00H
FCR	Flow Control Register	0AH	00H
EPCR	EEPROM & PHY Control Register	0BH	00H
EPAR	EEPROM & PHY Address Register	0CH	40H
EPDRL	EEPROM & PHY Low Byte Data Register	0DH	00H
EPDRH	EEPROM & PHY High Byte Data Register	0EH	00H
WUCR	Wake Up Control Register (0FH)	0FH	00H
PAR	Processor Port Physical Address Registers	10H-15H	by EEPROM
MAR	Processor Port Multicast Address Registers	16H-1DH	XXH
RXPLLR	RX Packet Length Low Register	20H	00H
RXPLHR	RX Packet Length High Register	21H	00H
RASR	RX Additional Status Register	26H	00H
RACR	RX Additional Control Register	27H	00H
VID	Vendor ID Registers	28H-29H	0A46H
PID	Product ID Registers	2AH-2BH	9003H
CHIPR	CHIP Revision Registers	2CH	01H
TCSCR	Transmit Check Sum Control Register	31H	00H
RCSCSR	Receive Check Sum Control Status Register	32H	00H
DRIVER	uP Data Bus driving capability Register	38H	00H
IRQCR	IRQ Pin Control Register	39H	00H
SWITCHCR	Switch Control Register	52H	00H
VLANCR	VLAN Control Register	53H	00H
P_INDEX	Per Port Control/Status Index Register	60H	00H
P_CTRL	Per Port Control Data Register	61H	00H
P_STUS	Per Port Status Data Register	62H	00H
P_RATE	Per Port Ingress and Egress Rate Control Register	66H	00H
P_BW	Per Port Bandwidth Control Setting Register	67H	00H
P_UNICAST	Per Port Block Unicast Ports Control Register	68H	00H
P_MULTI	Per Port Block Multicast Ports Control Register	69H	00H
P_BCAST	Per Port Block Broadcast Ports Control Register	6AH	00H
P_UNKNWN	Per Port Block Unknown Ports Control Register	6BH	00H
P_PRI	Per Port Priority Queue Control Register	6DH	00H
VLAN_TAGL	Per Port VLAN Tag Low Byte Register	6EH	01H
VLAN_TAGH	Per Port VLAN Tag High Byte Register	6FH	00H

P_MIB_IDX	Per Port MIB counter Index Register	80H	00H
MIB_DAT	MIB counter Data Register bit 0~7	81H	00H
	MIB counter Data Register bit 8~15	82H	00H
	MIB counter Data Register bit 16~23	83H	00H
	MIB counter Data Register bit 24~31	84H	00H
PVLAN	Port-based VLAN mapping table registers	B0-BFH	0FH
TOS_MAP	TOS Priority Map Registers	C0-CFH	00H~FFH
VLAN_MAP	VLAN Priority Map Registers	D0-D1H	50H,FAH
MRCMDX	Memory Data Pre-Fetch Read Command Without Address Increment Register	F0H	XXH
MRCMD	Memory Data Read Command With Address Increment Register	F2H	XXH
MRRL	Memory Data Read_ address Register Low Byte	F4H	00H
MRRH	Memory Data Read_ address Register High Byte	F5H	00H
MWCMDX	Memory Data Write Command Without Address Increment Register	F6H	XXH
MWCMD	Memory Data Write Command With Address Increment Register	F8H	XXH
MWRL	Memory Data Write_ address Register Low Byte	FAH	00H
MWRH	Memory Data Write _ address Register High Byte	FBH	00H
TXPLL	TX Packet Length Low Byte Register	FCH	XXH
TXPLH	TX Packet Length High Byte Register	FDH	XXH
ISR	Interrupt Status Register	FEH	00H
IMR	Interrupt Mask Register	FFH	00H

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where:
<Reset Value>:
1 Bit set to logic one
0 Bit set to logic zero
X No default value
P = power on reset, by PWRST# pin, default value
H = hardware reset, by Reg. 52H bit 6, default value
S = software reset, by Reg. 00H bit 0, default value
E = default value from EEPROM setting
T = default value from strap pin
<Access Type>:
RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1=Read/Write and Cleared by write 1
WO = Write only
Reserved bits should be written with 0.
Reserved bits are undefined on read access.

6.1 Network Control Register (00H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	WAKEEN	P0,WO	Wakeup Event Enable When set, it enables the wakeup function. Clearing this bit will also clear all wakeup event status This bit will not be affected after a software reset
5	CLR1	PH0,RW	0: REG. 01H auto-cleared after read 1: REG. 01H cleared by writing 1 to respected bit.
4:2	RESERVED	0,RO	Reserved
1	LBK	PH0, RW	Loopback test Mode All transmit packets from processor port are forward to processor port itself.
0	RST	PH0,RW	Software reset and auto clear after 10us

6.2 Network Status Register (01H)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	WAKEST	PH0, W/C1	Wakeup Event Status. This bit is set after wake-up event (link change) occurred. If bit 5 of NCR is set, this bit is cleared by write 1; Otherwise it can be cleared by read or write 1.
4	RESERVED	0,RO	Reserved
3	TX2END	PHS0, RW/C1	TX Packet 2 Complete Status. This bit is set after transmit completion of packet index 2 If bit 5 of NCR is set, this bit is cleared by write 1; Otherwise it can be cleared by read or write 1.
2	TX1END	PHS0, RW/C1	TX Packet 1 Complete status. This bit is set after transmit completion of packet index 1 If bit 5 of NCR is set, this bit is cleared by write 1; Otherwise it can be cleared by read or write 1.
1:0	RESERVED	0,RO	Reserved

6.3 TX Control Register (02H)

Bit	Name	Default	Description
7:4	RESERVED	0,RO	Reserved
3	CRC_DIS2	PHS0,RW	CRC Appends Disable for Packet Index 2
2	RESERVED	0,RO	Reserved
1	CRC_DIS1	PHS0,RW	CRC Appends Disable for Packet Index 1
0	TXREQ	PHS0,RW	TX Request. Auto clears after transmit completely

6.4 RX Control Register (05H)

Bit	Name	Default	Description
7	HASHALL	PHS0,RW	Filter All address in Hash Table
6	RESERVED	PHS0,RW	Reserved
5:4	RESERVED	PHS0,RW	Reserved
3	ALL	PHS0,RW	Pass All Multicast Packets All received packets with bit 0 is “1” of Destination Address (DA) field are accepted and save to receive memory.
2	RESERVED	PHS0,RW	Reserved
1	PRMSC	PHS0,RW	Promiscuous Mode All received packets are accepted and save to receive memory without DA field filter.
0	RXEN	PHS0,RW	RX Enable

6.5 RX Status Register (06H)

Bit	Name	Default	Description
7:4	RESERVED	0,RO	Reserved
3:2	SRCP	0,RO	Source Port Number
1	CE	PH0,RO	CRC Error It is set to indicate that the received frame ends with a CRC error
0	RESERVED	0,RO	Reserved

6.6 Receive Overflow Counter Register (07H)

Bit	Name	Default	Description
7	RXFU	PHS0,R/C	Receive Overflow Counter Overflow This bit is set when the ROC has an overflow condition
6:0	ROC	PHS0,R/C	Receive Overflow Counter This is a statistic counter to indicate the received packet count upon FIFO overflow

6.7 Flow Control Register (0AH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	FLOW_EN	PHS0,RW	RX Flow Control Enable Enables the pause packet for high/low water threshold control
4:0	RESERVED	0,RO	Reserved

6.8 EEPROM & PHY Control Register (0BH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	REEP	PH0,RW	Reload EEPROM. Driver needs to clear it up after the operation completes
4	WEP	PH0,RW	Write EEPROM Enable

3	EPOS	PH0,RW	EEPROM or PHY Operation Select When reset, select EEPROM; when set, select PHY
2	ERPRR	PH0,RW	EEPROM Read or PHY Register Read Command. Driver needs to clear it up after the operation completes.
1	ERPRW	PH0,RW	EEPROM Write or PHY Register Write Command. Driver needs to clear it up after the operation completes.
0	ERRE	PH0,RO	EEPROM Access Status or PHY Access Status When set, it indicates that the EEPROM or PHY access is in progress

6.9 EEPROM & PHY Address Register (0CH)

Bit	Name	Default	Description
7:6	PHY_ADR	PH01,RW	PHY Address bit 1 and 0; the PHY address bit [4:2] is force to 0.
5:0	EROA	PH0,RW	EEPROM Word Address or PHY Register Address

6.10 EEPROM & PHY Data Registers (0DH~0EH)

Bit	Name	Default	Description
7:0	EPDRL	PH0,RW	EEPROM or PHY Low Byte Data (0DH) This data is made to write/read low byte of word address defined in Reg. 0CH to EEPROM or PHY
7:0	EPDRH	PH0,RW	EEPROM or PHY High Byte Data (0EH) This data is made to write/read high byte of word address defined in Reg. 0CH to EEPROM or PHY

6.11 Wake Up Control Register (0FH)

Bit	Name	Type	Description
7:6	RESERVED	0,RO	Reserved
5	LINKEN	PE0,RW	Link Change Event Enable When set, it enables Link Status Change Wake up Event
4:3	RESERVED	0,RO	Reserved
2	LINKST	PH0,RO	Link Change Event Status When set, it indicates that Link Status Change Event (link of port 0 or 1) occurred This bit can be cleared by write 1 to bit 5 of NSR or write 0 to bit 6 of NCR.
1:0	RESERVED	0,RO	Reserved

6.12 Processor Port Physical Address Registers (10H~15H)

Bit	Name	Default	Description
7:0	PAB5	E,RW	Physical Address Byte 5 (15H)
7:0	PAB4	E,RW	Physical Address Byte 4 (14H)
7:0	PAB3	E,RW	Physical Address Byte 3 (13H)
7:0	PAB2	E,RW	Physical Address Byte 2 (12H)
7:0	PAB1	E,RW	Physical Address Byte 1 (11H)
7:0	PAB0	E,RW	Physical Address Byte 0 (10H)

6.13 Processor Port Multicast Address Registers (16H~1DH)

Bit	Name	Default	Description
7:0	MAB7	X,RW	Multicast Address Byte 7 (1DH)
7:0	MAB6	X,RW	Multicast Address Byte 6 (1CH)
7:0	MAB5	X,RW	Multicast Address Byte 5 (1BH)

7:0	MAB4	X,RW	Multicast Address Byte 4 (1AH)
7:0	MAB3	X,RW	Multicast Address Byte 3 (19H)
7:0	MAB2	X,RW	Multicast Address Byte 2 (18H)
7:0	MAB1	X,RW	Multicast Address Byte 1 (17H)
7:0	MAB0	X,RW	Multicast Address Byte 0 (16H)

6.14 RX Packet Length Low Register (20H)

Bit	Name	Default	Description
7:0	RXPLL	PH,RO	RX Packet Length Low byte

6.15 RX Packet Length High Register (21H)

Bit	Name	Default	Description
7:0	RXPLH	PH,RO	RX Packet Length High byte

6.16 RX Additional Status Register (26H)

Bit	Name	Default	Description
7:4	RESERVED	0,RO	Reserved
1:0	RPTRS	PH,RO	uP received pointer status, only available when RX pointer restriction is enabled (Reg27h.7=0). 00: Within buffer 01: End of buffer 1x: Exceed buffer

6.17 RX Additional Control Register (27H)

Bit	Name	Default	Description
7	RPRD	PHS0,RW	RX pointer restriction disable
6:0	RESERVED	0,RO	Reserved

6.18 Vendor ID Registers (28H~29H)

Bit	Name	Default	Description
7:0	VIDH	PE,0AH,RO	Vendor ID High Byte (29H)
7:0	VIDL	PE,46H.RO	Vendor ID Low Byte (28H)

6.19 Product ID Registers (2AH~2BH)

Bit	Name	Default	Description
7:0	PIDH	PE,90H,RO	Product ID High Byte (2BH)
7:0	PIDL	PE,03H.RO	Product ID Low Byte (2AH)

6.20 Chip Revision Register (2CH)

Bit	Name	Default	Description
7:0	CHIPR	01H,RO	CHIP Revision

6.21 Transmit Check Sum Control Register (31H)

Bit	Name	Default	Description
7~3	RESERVED	0,RO	Reserved
2	UDPCSE	HP0,RW	UDP Checksum Generation Enable
1	TCPCSE	HP0,RW	TCP Checksum Generation Enable
0	IPCSE	HP0,RW	IP Checksum Generation Enable

6.22 Receive Check Sum Control Status Register (32H)

Bit	Name	Default	Description
7	UDPS	HP0,RO	UDP Checksum Status 1: UDP packet checksum is fail. 0: UDP packet checksum is OK or it is not a UDP packet.
6	TCPS	HP0,RO	TCP Checksum Status 1: TCP packet checksum is fail. 0: TCP packet checksum is OK or it is not a TCP packet.
5	IPS	HP0,RO	IP Checksum Status 1: IP packet checksum is ail 0: IP packet checksum is OK or it is not an IP packet.
4	UDPP	HP0,RO	This is an UDP Packet
3	TCPP	HP0,RO	This is a TCP Packet
2	IPP	HP0,RO	This is an IP Packet
1	RCSEN	HPS0,RW	Receive Checksum Checking Enable When set, the checksum status will store in packet first byte of status header.
0	DCSE	HPS0,RW	Discard Checksum Error Packet When set, IP/TCP/UDP checksum field is error, this packet will be discarded.

6.23 uP Data Bus driving capability Register (38H)

Bit	Name	Default	Description
7	RESERVED	0,RW	reserved
6:5	ISA_CURR	P01,RW	SD Bus Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
4:3	Reserved	P0,RW	Reserved
2	STEP	P0,RW	Data Bus Output stepping 1: disabled 0: enabled
1	IOW_SPIKE	P0,RW	Eliminate IOW spike 1: eliminate about 2ns IOW spike
0	IOR_SPIKE	P1,RW	Eliminate IOR spike 1: eliminate about 2ns IOR spike

6.24 IRQ Pin Control Register (39H)

Bit	Name	Default	Description
7:2	Reserved	PS0,RO	Reserved
1	IRQ_TYPE	PET0,RW	IRQ Pin Output Type Control 1: IRQ Open-Collector output 0: IRQ direct output
0	IRQ_POL	PET0,RW	IRQ Pin Polarity Control 1: IRQ active low 0: IRQ active high

6.25 TX/RX Memory Size Control Register (3FH)

Bit	Name	Default	Description
7:6	Reserved	PS0,RO	Reserved
5:0	TX_SIZE	P20h,RW	TX block size This value defines the transmit block size in 256-byte unit. TX memory size = TX_SIZE * 256 bytes And then RX memory size = 16KB – (TX_SIZE + 1)*256-Byte

6.26 Switch Control Register (52H)

Bit	Name	Default	Description
7	MEM_BIST	PH0,RO	Address Memory Test BIST Status 0: OK 1: Fail
6	RST_SW	P0,RW	Reset Switch Core and auto clear after 10us
5	RST_ANLG	P0,RW	Reset Analog PHY Core and auto clear after 10us
4:3	SNF_PORT	PE00,RW	Sniffer Port Number Define the port number to act as the sniffer port
2	CRC_DIS	PE0,RW	CRC Checking Disable When set, the received CRC error packet also accepts to receive memory.
1:0	AGE	PE0,RW	Aging 00: no aging 01: 64 ± 32 sec 10: 128 ± 64 sec 11: 256 ±128 sec

6.27 VLAN Control Register (53H)

Bit	Name	Default	Description
7	TOS6	PE0,RW	Full ToS Using Enable 1: check most significant 6-bit of TOS 0: check most significant 3-bit only of TOS
6	RESERVED	0,RO	Reserved
5	UNICAST	PE0,RW	Unicast packet can across VLAN boundary
4	VIDFF	PE0,RW	Replace VIDFF If the received packet is a tagged VLAN with VID equal to “FFF”, its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH.
3	VID1	PE0,RW	Replace VID01 If the received packet is a tagged VLAN with VID equal to “001”, its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH.
2	VID0	PE0,RW	Replace VID0 If the received packet is a tagged VLAN with VID equal to “000”, its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH.
1	PRI	PE0,RW	Replace priority field in the tag with value define in Reg 6FH bit 7~5.
0	VLAN	PE0,RW	VLAN mode enable 1: 802.1Q base VLAN mode enable 0: port-base VLAN only

6.28 Per Port Control/Status Index Register (60H)

Bit	Name	Default	Description
7:5	reserved	PHS0,RW	reserved
4:2	reserved	0,RO	reserved
1:0	INDEX	PHS0,RW	Port index for register 61H~84H Write the port number to this register before write/read register 61H~84H. Note: The processor port INDEX number is 3

6.29 Per Port Control Data Register (61H)

Bit	Name	Default	Description
7	RESERVED	PE0,RW	Reserved
6	PARTI_EN	PE0,RW	Enable Partition Detection
5	NO_DIS_RX	PE0,RW	Not Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control.
4	FLOW_DIS	PE0,RW	Flow control in full duplex mode, or back pressure in half duplex mode enable 0: enable 1: disable
3	BANDWIDTH	PE0,RW	Bandwidth Control 0: Control with Ingress and Egress separately, ref to Register 66H. 1: Control with Ingress or Egress, ref to Register 67H
2	BP_DIS	PE0,RW	Broadcast packet filter 0: accept broadcast packets 1: reject broadcast packets
1	MP_DIS	PE0,RW	Multicast packet filter 0: accept multicast packets 1: reject multicast packets
0	MP_STORM	PE0,RW	Broadcast Storm Control 0: only broadcast packets storm are controlled 1: multicast packets also same as broadcast storm control.

6.30 Per Port Status Data Register (62H)

Bit	Name	Default	Description
7:6	RESERVED	P0,RO	Reserved
5	LP_FCS	P0,RO	Link Partner Flow Control Enable Status
4	BIST	P0,RO	BIST status 1: SRAM BIST fail 0: SRAM BIST pass
3	RESERVED	0,RO	Reserved
2	SPEED2	P0,RO	PHY Speed Status 0: 10Mbps, 1: 100Mbps
1	FDX2	P0,RO	PHY Duplex Status 0: half-duplex, 1: full-duplex
0	LINK2	P0,RO	PHY Link Status 0: link fail, 1: link OK

6.31 Per Port Forward Control Register (65H)

Bit	Name	Default	Description
7	LOOPBACK	PH0,RW	Loop-Back Mode The received packet will be forward to this port itself.
6	MONI_TX	PH0,RW	TX Packet Monitored The transmitted packets are also forward to sniffer port.
5	MONI_RX	PH0,RW	RX Packet Monitored The received packets are also forward to sniffer port.
4	DIS_BMP	PH0,RW	Broad/Multicast Not Monitored The received broadcast or multicast packets are not forward to sniffer port.
3	Reserved	PH0,RW	Reserved
2	TX_DIS	PH0,RW	Packet Transmit Disabled All packets can not be forward to this port.
1	RX_DIS	PH0,RW	Packet receive Disabled All received packets are discarded.
0	ADR_DIS	PH0,RW	Address Learning Disabled The Source Address (SA) field of packet is not learned to address table.

6.32 Per Port Ingress and Egress Control Register (66H)

Bit	Name	Default	Description
7:4	INGRESS	PE0,RW	Ingress Rate Control These bits define the bandwidth threshold that received packets over the threshold are discarded. Ingress Rate table below 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps
3:0	EGRESS	PE0,RW	Egress Rate Control These bits define the bandwidth threshold that transmitted packets over the threshold are discarded. Egress Rate table below 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

6.33 Per Port Bandwidth Control Setting Register (67H)

Bit	Name	Default	Description
7:4	BSTH	PE0,RW	Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded. Threshold table below 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control
3:0	BW CTRL	PE0,RW	Received packet length counted. Bandwidth table below These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded. Bandwidth table below 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

6.34 Per Port Block Unicast Ports Control Register (68H)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_UP	PH0,RW	Ports of Unicast Packet Be Blocked The received unicast packets are not forward to the assigned ports. Note: that the assigned port definition: bit 0 for port 0, bit 1 for port 1, bit 2 reserved, and bit 3 for processor port.

6.35 Per Port Block Multicast Ports Control Register (69H)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_MP	PH0,RW	Ports of Multicast Packet Be Blocked The received multicast packets are not forward to the assigned ports.

6.36 Per Port Block Broadcast Ports Control Register (6AH)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_BP	PH0,RW	Ports of Broadcast Packet Be Blocked The received broadcast packets are not forward to the assigned ports.

6.37 Per Port Block Unknown Ports Control Register (6BH)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_UKP	PH0,RW	Ports of Unknown Packet Be Blocked The packets with DA field not found in address table are not forward to the assigned ports.

6.38 Per Port Priority Queue Control Register (6DH)

Bit	Name	Default	Description
7	TAG_OUT	PE0,RW	Output Packet Tagging Enable The transmitted packets are containing VLAN tagged field.
6	PRI_DIS	PE0,RW	Priority Queue Disable Only one transmit queue is supported in this port.
5	WFQUE	PE0,RW	Weighted Round-Robin Queuing 1: The priority weight for queue 3, 2, 1, and 0 is 8, 4, 2, and 1 respectively. 0: The queue 3 has the highest priority, and the next priorities are queue 2, 1, and 0 respectively.
4	TOS_PRI	PE0,RW	Priority ToS over VLAN If an IP packet with VLAN tag, the priority of this packet is decode from ToS field.
3	TOS_OFF	PE0,RW	ToS Priority Classification Disable The priority information from ToS field of IP packet is ignored.
2	PRI_OFF	PE0,RW	802.1 p Priority Classification Disable The priority information from VLAN tag field is ignored.

1:0	P_PRI	PE0,RW	Port Base priority The priority queue number in port base. 00 : queue 0, 01 : queue 1, 10 : queue 2, 11 : queue 3

6.39 Per Port VLAN Tag Low Byte Register (6EH)

Bit	Name	Default	Description
7:0	VID70	PE01,RW	VID[7:0]

6.40 Per Port VLAN Tag High Byte Register (6FH)

Bit	Name	Default	Description
7:5	PRI	PE0,RW	Tag [15:13]
4	CFI	PE0,RW	Tag[12]
3:0	VID118	PE0,RW	VID[11:8]

6.41 MIB Counter Port Index Register (80H)

Bit	Name	Default	Description
7	READY	P0,RO	MIB counter data is ready When this register is written with INDEX data, this bit is cleared and the MIB counter reading is in progress. After end of read MIB counter, the MIB data is loaded into registers 81H~ 84H and this bit is set to indicate that the MIB data is ready, and then the MIB data of this INDEX is cleared.
6:5	reserved	0,RO	Reserved
4:0	INDEX	PHS0,RW	MIB counter index 0~9, each counter is 32-bit in Register 81H~84H. Write the MIB counter index to this register before read them.

6.42 MIB Counter Data Registers (81H~84H)

Register	Name	Default	Description
81H	MIB_DAT	X,RO	MIB counter Data Register bit 0~7
82H	MIB_DAT	X,RO	MIB counter Data Register bit 8~15
83H	MIB_DAT	X,RO	MIB counter Data Register bit 16~23
84H	MIB_DAT	X,RO	MIB counter Data Register bit 24~31

MIB counter: RX Byte Counter Registers (INDEX 00H)

MIB counter: RX Uni-cast Packet Counter Registers (INDEX 01H)

MIB counter: RX Multi-cast Packet Counter Registers (INDEX 02H)

MIB counter: RX Discard Packet Counter Registers (INDEX 03H)

MIB counter: RX Error Packet Counter Registers (INDEX 04H)

MIB counter: TX Byte Counter Registers (INDEX 05H)

MIB counter: TX Uni-cast Packet Counter Registers (INDEX 06H)

MIB counter: TX Multi-cast Packet Counter Registers (INDEX 07H)

MIB counter: TX Discard Packet Counter Registers (INDEX 08H)

MIB counter: TX Error Packet Counter Registers (INDEX 09H)

6.43 Port-Based VLAN Mapping Table Registers (B0H~BFH)

Define the port member in VLAN group
There are 16 VLAN group that defined in Reg. B0H~BFH.
Group 0 defined in Reg. B0H, and group 1 defined in Reg. B1H, and so on.

Bit	Name	Default	Description
7:4	RESERVED	PE0,RO	Reserved
3	PORT_UP	PE1,RW	Mapping to processor
2	RESERVED	PE1,RW	Reserved
1	PORT_P1	PE1,RW	Mapping to port 1
0	PORT_P0	PE1,RW	Mapping to port 0

6.44 TOS Priority Map Registers (C0H~CFH)

Define the 6-bit or 3-bit of ToS field mapping to 2-bit priority queue number.
In 6-bit type, the Reg. 53H bit 7 is "1", Reg. C0H bit [1:0] define the mapping for ToS value 0, Reg. 60H bit [3:2] define the mapping for ToS value 1, and so on, till Reg. CFH bit [7:6] define ToS value 63.
In 3-bit type, Reg. 53H bit 7 is "0" define the mapping for ToS value 0, Reg. 60H bit [3:2] define the mapping for ToS value 1, and so on, till Reg. C1H bit [7:6] define ToS value 7.

Reg. C0H:

Bit	Name	Default	Description
7:6	TOS3	PE0/1,RW	If Reg. 53H. bit 7 =1 :TOS[7:2]=03H, otherwise TOS]7:5]=03H
5:4	TOS2	PE0,/1RW	If Reg. 53H. bit 7 =1 :TOS[7:2]=02H, otherwise TOS]7:5]=02H
3:2	TOS1	PE0,RW	If Reg.53H. bit 7 =1 :TOS[7:2]=01H, otherwise TOS]7:5]=01H
1:0	TOS0	PE0,RW	If Reg.53H. bit 7 =1 :TOS[7:2]=00H, otherwise TOS]7:5]=00H

Reg. C1H:

Bit	Name	Default	Description
7:6	TOS7	PE0/3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=07H, otherwise TOS]7:5]=07H
5:4	TOS6	PE0/3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=06H, otherwise TOS]7:5]=06H
3:2	TOS5	PE0/2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=05H, otherwise TOS]7:5]=05H
1:0	TOS4	PE0/2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=04H, otherwise TOS]7:5]=04H

Reg. C2H:

Bit	Name	Default	Description
7:6	TOSB	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=0BH
5:4	TOSA	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=0AH
3:2	TOS9	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=09H
1:0	TOS8	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=08H

Reg. C3H:

Bit	Name	Default	Description
7:6	TOSF	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=0FH
5:4	TOSE	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=0EH
3:2	TOSD	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=0DH
1:0	TOSC	PE0,RW	If Reg.53H. bit 7=1 :TOS[7:2]=0CH

Reg. C4H:

Bit	Name	Default	Description
7:6	TOS13	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=13H
5:4	TOS12	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=12H
3:2	TOS11	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=11H
1:0	TOS10	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=10H

Reg. C5H:

Bit	Name	Default	Description
7:6	TOS17	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=17H
5:4	TOS16	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=16H
3:2	TOS15	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=15H
1:0	TOS14	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=14H

Reg. C6H:

Bit	Name	Default	Description
7:6	TOS1B	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=1BH
5:4	TOS1A	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=1AH
3:2	TOS19	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=19H
1:0	TOS18	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=18H

Reg. C7H:

Bit	Name	Default	Description
7:6	TOS1F	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=1FH
5:4	TOS1E	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=1EH
3:2	TOS1D	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=1DH
1:0	TOS1C	PE1,RW	If Reg.53H. bit 7=1 :TOS[7:2]=1CH

Reg. C8H:

Bit	Name	Default	Description
7:6	TOS23	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=23H
5:4	TOS22	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=22H
3:2	TOS21	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=21H
1:0	TOS20	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=20H

Reg. C9H:

Bit	Name	Default	Description
7:6	TOS27	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=27H
5:4	TOS26	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=26H
3:2	TOS25	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=25H
1:0	TOS24	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=24H

Reg. CAH:

Bit	Name	Default	Description
7:6	TOS2B	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=2BH
5:4	TOS2A	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=2AH
3:2	TOS29	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=29H
1:0	TOS28	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=28H

Reg. CBH:

Bit	Name	Default	Description
7:6	TOS2F	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=2FH
5:4	TOS2E	PE2,RW	If Reg.53H. bit 7=1 :TOS[7:2]=2EH
3:2	TOS2D	PE2,RW	If Reg.53H. bit 7 =1 :TOS[7:2]=2DH
1:0	TOS2C	PE2,RW	If Reg.53H. bit 7 =1 :TOS[7:2]=2CH

Reg. CCH:

Bit	Name	Default	Description
7:6	TOS33	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=33H
5:4	TOS32	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=32H
3:2	TOS31	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=31H
1:0	TOS30	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=30H

Reg. CDH:

Bit	Name	Default	Description
7:6	TOS37	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=37H
5:4	TOS36	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=36H
3:2	TOS35	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=35H
1:0	TOS34	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=34H

Reg. CEH:

Bit	Name	Default	Description
7:6	TOS3B	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=3BH
5:4	TOS3A	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=3AH
3:2	TOS39	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=39H
1:0	TOS38	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=38H

Reg. CFH:

Bit	Name	Default	Description
7:6	TOS3F	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=3FH
5:4	TOS3E	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=3EH
3:2	TOS3D	PE3,RW	If Reg.53H. bit 7=1 :TOS[7:2]=3DH
1:0	TOS3C	PE3,RW	If Reg.53H. bit 7 =1 :TOS[7:2]=3CH

6.45 VLAN Priority Map Registers (D0H~D1H)

Define the 3-bit of priority field VALN mapping to 2-bit priority queue number.

Reg. D0H:

Bit	Name	Default	Description
7:6	TAG3	PE1,RW	VLAN priority tag value = 03H
5:4	TAG2	PE1,RW	VLAN priority tag value = 02H
3:2	TAG1	PE0,RW	VLAN priority tag value = 01H
1:0	TAG0	PE0,RW	VLAN priority tag value = 00H

Reg. D1H:

Bit	Name	Default	Description
7:6	TAG7	PE3,RW	VLAN priority tag value = 07H
5:4	TAG6	PE3,RW	VLAN priority tag value = 06H
3:2	TAG5	PE2,RW	VLAN priority tag value = 05H
1:0	TAG4	PE2,RW	VLAN priority tag value = 04H

6.46 Memory Data Pre-Fetch Read Command without Address Increment Register (F0H)

Bit	Name	Default	Description
7:0	MRCMDX	X,RO	Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. And the DM9003 starts to pre-fetch the SRAM data to internal data buffers.

6.47 Memory Data Read Command with Address Increment Register (F2H)

When register FFH bit 7 is “0”, register F5H value will be returned to 0000H, if 16K-byte boundary is reached.
When register FFH bit 7 is “1”, register F5H value will be returned to 0000H, if processor port receive memory byte boundary address RX memory size, defined in register 3FH with default 1F00H, is reached.

Bit	Name	Default	Description
7:0	MRCMD	X,RO	Read data from RX SRAM. After the read of this command, the read pointer is increased by 1,2, or 4, depends on the operator mode (8-bit,16-bit and 32-bit respectively)

6.48 Memory Data Read Address Register (F4H)

When register FFH bit 7 is “0”, register F5H and F4H can be used as memory byte address to read internal 64K-byte memory.
When register FFH bit 7 is “1”, register F5H and F4H can be used as processor port receive memory byte address with memory space range from 0 to (RX memory size - 1), defined in register 3FH with default 1EFFH.

Bit	Name	Default	Description
7:0	MDRAL	PHS0,RW	Memory Data Read Address Low Byte[7:0]

6.49 Memory Data Read Address Register (F5H)

Bit	Name	Default	Description
7:0	MDRAH50	PHS0,RW	Memory Data Read Byte Address High Byte[15:8]

6.50 Memory Data Write Command without Address Increment Register (F6H)

Bit	Name	Default	Description
7:0	MWCMDX	X,WO	Write data to TX SRAM. After the write of this command, the write pointer is unchanged

6.51 Memory Data Write Command with Address Increment Register (F8H)

When register FFH bit 7 is "0", register FBH value will be returned to 0000H, if 16K-byte boundary is reached.

Bit	Name	Default	Description
7:0	MWCMD	X,WO	Write Data to TX SRAM After the write of this command, the write pointer is increased by 1, 2, or 4, depends on the operator mode. (8-bit, 16-bit,32-bit respectively)

6.52 Memory Data Write Address Register (FAH)

When register FFH bit 7 is "0", register FBH and FAH can be used as memory byte address to write internal 64K-byte memory.

When register FFH bit 7 is "1", register FBH and FAH are reserved. The processor port transmit memory address is generated by DM9003 automatically.

Bit	Name	Default	Description
7:0	MDWAL	PHS0,RW	Memory Data Write_address Low Byte[7:0]

6.53 Memory Data Write Address Register (FBH)

Bit	Name	Default	Description
7:0	MDWAH	PHS0,RW	Memory Data Write Byte Address High Byte[15:8]

6.54 TX Packet Length Registers (FCH~FDH)

Bit	Name	Default	Description
7:0	TXPLH	PHS0,RW	TX Packet Length High byte
7:0	TXPLL	PHS0,RW	TX Packet Length Low byte

6.55 Interrupt Status Register (FEH)

Bit	Name	Default	Description
7	IOMODE	T0, RO	Width Processor Data Bus 0: 16-bit mode 1: 8-bit mode
6	RESERVED	PHS0,RO	Reserved
5	LNKCHG	PHS0,RW/C1	Link Status Change of port 0 or 1
4	CNT_ERR	PHS0,RW/C1	Memory Management error
3	ROO	PHS0,RW/C1	Receive Overflow Counter Overflow
2	ROS	PHS0,RW/C1	Receive Overflow
1	PT	PHS0,RW/C1	Packet Transmitted
0	PR	PHS0,RW/C1	Packet Received

6.56 Interrupt Mask Register (FFH)

Bit	Name	Default	Description
7	TXRX_EN	PHS0,RW	Enable the SRAM read/write pointer used as transmit /receive address.
6	RESERVED	P0,RO	Reserved
5	LNKCHGI	PHS0,RW	Enable Link Status Change of port 0 or 1Interrupt
4	CNT_ERR	PHS0,RW/C1	Enable Memory Management error interrupt
3	ROOI	PHS0,RW	Enable Receive Overflow Counter Overflow Interrupt
2	ROI	PHS0,RW	Enable Receive Overflow Interrupt
1	PTI	PHS0,RW	Enable Packet Transmitted Interrupt
0	PRI	PHS0,RW	Enable Packet Received Interrupt

7. EEPROM FORMAT

name	Word	Description
MAC address	0~2	6 byte Ethernet Address
Auto Load Control	3	Bit 1:0=01: Update vendor ID and product ID Bit 3:2=01: Accept setting of WORD6 [4:0] Bit 5:4= reserved Bit 7:6= reserved, set to 00 in application Bit 9:8=Reserved Bit 11:10= Reserved, set to 00 in application Bit 13:12= Reserved Bit 15:14=01: Accept setting of WORD7 [15:12]
Vendor ID	4	2-byte vendor ID (Default: 0A46H)
Product ID	5	2-byte product ID (Default: 9003H)
pin control	6	When word 3 bit [3:2] =01, these bits can control the CS#, IOR#, IOW# and IRQ pins polarity. Bit0: CS# pin is active high when set (default active low) Bit1: IOR# pin is active high when set (default: active low) Bit2: IOW# pin is active high when set (default: active low) Bit3: IRQ pin is active low when set (default: active high) Bit4: IRQ pin is open-collected (default: force output) Bit 15:5: Reserved
PHY control	7	Bit11:0: reserved Bit 13:12 reserved, set 00 in application Bit14: Port 1 AUTO-MDIX control 1: ON, 0: OFF(default ON) Bit15: Port 0 AUTO-MDIX control 1: ON, 0: OFF(default ON)
RESERVED	8~15	Reserved
Control	16	Bit 1:0=01: Accept setting of WORD 17,18 Bit 3:2=01: Accept setting of WORD 19~26 Bit 5:4=01: Accept setting of WORD 27~30 Bit 7:6=01: Accept setting of WORD 31 Bit 9:8=01: Accept setting of WORD 32~39 Bit 11:10=01: Accept setting of WORD 40~47 Bit 15:12 = Reserved, set 0000 in application
Switch Control 1	17	When word 16 bit 1:0 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. 52H bit 7~0 This word bit 15~8 will be loaded to Reg. 53H bit 7~0
Switch Control 2	18	When word 16 bit 1:0 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. 58H bit 7~0 This word bit 15~8 will be loaded to Reg. 59H bit 7~0
Port 0 Control 1	19	When word 16 bit 3:2 is “01”, after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 61H bit 7~0 This word bit 15~8 will be loaded to port 0 Reg. 66H bit 7~0
Port 0 Control 2	20	When word 16 bit 3:2 is “01”, after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 67H bit 7~0 This word bit 15~8 will be loaded to port 0 Reg. 6DH bit 7~0
Port 1 Control 1	21	When word 16 bit 3:2 is “01”, after power on reset: This word bit 7~0 will be loaded to port 1 Reg. 61H bit 7~0 This word bit 15~8 will be loaded to port 1 Reg. 66H bit 7~0

Port 1 Control 2	22	When word 16 bit 3:2 is “01”, after power on reset: This word bit 7~0 will be loaded to port 1 Reg. 67H bit 7~0 This word bit 15~8 will be loaded to port 1 Reg. 6DH bit 7~0
RESERVED	23~24	Reserved
uP Port Control 1	25	When word 16 bit 3:2 is “01”, after power on reset: This word bit 7~0 will be loaded to port 3 Reg. 61H bit 7~0 This word bit 15~8 will be loaded to port 3 Reg. 66H bit 7~0
uP Port Control 2	26	When word 16 bit 3:2 is “01”, after power on reset: This word bit 7~0 will be loaded to port 3 Reg. 67H bit 7~0 This word bit 15~8 will be loaded to port 3 Reg. 6DH bit 7~0
Port 0 VLAN Tag	27	When word 16 bit 5:4 is “01”, after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 6EH bit 7~0 This word bit 15~8 will be loaded to port 0 Reg. 6FH bit 7~0
Port 1 VLAN Tag	28	When word 16 bit 5:4 is “01”, after power on reset: This word bit 7~0 will be loaded to port 1 Reg. 6EH bit 7~0 This word bit 15~8 will be loaded to port 1 Reg. 6FH bit 7~0
RESERVED	29	Reserved
uP Port VLAN Tag	30	When word 16 bit 5:4 is “01”, after power on reset: This word bit 7~0 will be loaded to port 3 Reg. 6EH bit 7~0 This word bit 15~8 will be loaded to port 3 Reg. 6FH bit 7~0
VLAN Priority Map	31	When word 16 bit 7:6 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. D0H bit 7~0 This word bit 15~8 will be loaded to Reg. D1H bit 7~0
Port VLAN Group 0,1	32	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. B0H bit 7~0 This word bit 15~8 will be loaded to Reg. B1H bit 7~0
Port VLAN Group 2,3	33	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. B2H bit 7~0 This word bit 15~8 will be loaded to Reg. B3H bit 7~0
Port VLAN Group 4,5	34	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. B4H bit 7~0 This word bit 15~8 will be loaded to Reg. B5H bit 7~0
Port VLAN Group 6,7	35	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. B6H bit 7~0 This word bit 15~8 will be loaded to Reg. B7H bit 7~0
Port VLAN Group 8,9	36	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. B8H bit 7~0 This word bit 15~8 will be loaded to Reg. B9H bit 7~0
Port VLAN Group 10,11	37	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. BAH bit 7~0 This word bit 15~8 will be loaded to Reg. BBH bit 7~0
Port VLAN Group 12,13	38	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. BCH bit 7~0 This word bit 15~8 will be loaded to Reg. BDH bit 7~0
Port VLAN Group 14,15	39	When word 16 bit 9:8 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. BEH bit 7~0 This word bit 15~8 will be loaded to Reg. BFH bit 7~0
ToS Priority Map 0	40	When word 16 bit 11:10 is “01”, after power on reset: This word bit 7~0 will be loaded to Reg. C0H bit 7~0

		This word bit 15~8 will be loaded to Reg. C1H bit 7~0
ToS Priority Map 1	41	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C2H bit 7~0 This word bit 15~8 will be loaded to Reg. C3H bit 7~0
ToS Priority Map 2	42	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C4H bit 7~0 This word bit 15~8 will be loaded to Reg. C5H bit 7~0
ToS Priority Map 3	43	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C6H bit 7~0 This word bit 15~8 will be loaded to Reg. C7H bit 7~0
ToS Priority Map 4	44	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C8H bit 7~0 This word bit 15~8 will be loaded to Reg. C9H bit 7~0
ToS Priority Map 5	45	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. CAH bit 7~0 This word bit 15~8 will be loaded to Reg. CBH bit 7~0
ToS Priority Map 6	46	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. CCH bit 7~0 This word bit 15~8 will be loaded to Reg. CDH bit 7~0
ToS Priority Map 7	47	When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. CEH bit 7~0 This word bit 15~8 will be loaded to Reg. CFH bit 7~0
RESERVED	53	Set to 0 in application

8. PHY REGISTERS

MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01H	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02H	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03H	PHYID2	OUI_LSB						VNDR_MDL						MDL_REV			
		101110						001011						0000			
04H	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05H	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06H	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
10H	Specified Config.	BP 4B5B	BP SCR	BP ALIGN	BP_ADPOK	Reservedr	TX	Reserved	RMII mode	Force 100LNK	Rsvd.	COL LED	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
11H	Specified Conf/Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserved	Reversed	Reversed	PHY ADDR [4:0]					Auto-N. Monitor Bit [3:0]			
12H	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Serial	Reserved									Polarity Reverse
13H	PWDOR	Reserved							PD10DRV	PD100I	PDchip	PDcrm	PDaeq	PDdrv	PDecli	PDeclo	PD10
14H	Specified config	TSTSE1	TSTSE2	FORCE_TXSD	FORCE_FEF	PREAMBLEX	TX10M_PWR	NWAY_PWR	Reserved	MDIX_CNTL	AutoNeg_dlpbk	Mdix_fix Value	Mdix_down	MonSel1	MonSel0	Reserved	PD_value
16H	RCVER	Receiver Error Counter															
17H	DIS_connect	Reversed						Disconnect_counter									
1DH	PSCR	Reversed				PREAMBLEX	AMPLITUDE	TX_PWR	Reversed								

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type> / <Attribute(s)>

Where:

<Reset Value>:

1 Bit set to logic one

0 Bit set to logic zero

X No default value

<Access Type>:

RO = Read only, RW = Read/Write

<Attribute (s)>:

SC = Self clearing, P = Value permanently set

8.1 Basic Mode Control Register (BMCR) – 00H

Bit	Bit Name	Default	Description
15	Reset	0, RW/SC	Reset 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
14	Loopback	0, RW	Loopback Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs
13	Speed selection	1, RW	Speed Select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type
12	Auto-negotiation enable	1, RW	Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status
11	Power down	0, RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1=Power down 0=Normal operation
10	Isolate	0,RW	Isolate Force to 0 in application.
9	Restart Auto-negotiation	0,RW/SC	Restart Auto-negotiation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM9003. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation
8	Duplex mode	1,RW	Duplex Mode 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation

7	Collision test	0,RW	Collision Test 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN in internal MII interface. 0 = Normal operation
6-0	Reserved	0,RO	Reserved Read as 0, ignore on write

8.2 Basic Mode Status Register (BMSR) – 01H

Bit	Bit Name	Default	Description
15	100BASE-T4	0,RO/P	100BASE-T4 Capable 1 = DM9003 is able to perform in 100BASE-T4 mode 0 = DM9003 is not able to perform in 100BASE-T4 mode
14	100BASE-TX full-duplex	1,RO/P	100BASE-TX Full Duplex Capable 1 = DM9003 is able to perform 100BASE-TX in full duplex mode 0 = DM9003 is not able to perform 100BASE-TX in full duplex mode
13	100BASE-TX half-duplex	1,RO/P	100BASE-TX Half Duplex Capable 1 = DM9003 is able to perform 100BASE-TX in half duplex mode 0 = DM9003 is not able to perform 100BASE-TX in half duplex mode
12	10BASE-T full-duplex	1,RO/P	10BASE-T Full Duplex Capable 1 = DM9003 is able to perform 10BASE-T in full duplex mode 0 = DM9003 is not able to perform 10BASE-TX in full duplex mode
11	10BASE-T half-duplex	1,RO/P	10BASE-T Half Duplex Capable 1 = DM9003 is able to perform 10BASE-T in half duplex mode 0 = DM9003 is not able to perform 10BASE-T in half duplex mode
10-7	Reserved	0,RO	Reserved Read as 0, ignore on write
6	MF preamble suppression	1,RO	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
4	Remote fault	0, RO	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9003 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
3	Auto-negotiation ability	1,RO/P	Auto Configuration Ability 1 = DM9003 is able to perform auto-negotiation 0 = DM9003 is not able to perform auto-negotiation
2	Link status	0,RO	Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that

			the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1	Jabber detect	0, RO	Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9003 reset. This bit works only in 10Mbps mode
0	Extended capability	1,RO/P	Extended Capability 1 = Extended register capable 0 = Basic register capable only

8.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9003. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15-0	OUI_MSB	<0181H>	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

8.4 PHY ID Identifier Register #2 (PHYID2) – 03H

Bit	Bit Name	Default	Description
15-10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9-4	VNDR_MDL	<001011>, RO/P	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3-0	MDL_REV	<0000>, RO/P	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

8.5 Auto-negotiation Advertisement Register (ANAR) – 04H

This register contains the advertised abilities of this DM9003 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	0,RO/P	Next page Indication 1 = Next page available 0 = No next page available The DM9003 has no next page, so this bit is permanently set to 0
14	ACK	0,RO	Acknowledge 1 = Link partner ability data reception acknowledged

			0 = Not acknowledged The DM9003's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit.
13	RF	0, RW	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
12-11	Reserved	X, RW	Reserved Write as 0, ignore on read
10	FCS	1, RW	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	0, RO/P	100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM9003 does not support 100BASE-T4 so this bit is permanently set to 0
8	TX_FDX	1, RW	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
7	TX_HDX	1, RW	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported
6	10_FDX	1, RW	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
5	10_HDX	1, RW	10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported
4-0	Selector	<00001>, RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05H

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	0, RO	Next Page Indication 1 = Link partner, next page available 0 = Link partner, no next page available
14	ACK	0, RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9003's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit
13	RF	0, RO	Remote Fault

			1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12-11	Reserved	0, RO	Reserved Read as 0, ignore on write
10	FCS	0, RO	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	0, RO	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	0, RO	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
7	TX_HDX	0, RO	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
6	10_FDX	0, RO	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5	10_HDX	0, RO	10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
4-0	Selector	<00000>, RO	Protocol Selection Bits Link partner's binary encoded protocol selector

8.7 Auto-negotiation Expansion Register (ANER) - 06H

Bit	Bit Name	Default	Description
15-5	Reserved	0, RO	Reserved Read as 0, ignore on write
4	PDF	0, RO/LH	Local Device Parallel Detection Fault PDF = 1: A fault detected via parallel detection function. PDF = 0: No fault detected via parallel detection function
3	LP_NP_ABLE	0, RO	Link Partner Next Page Able LP_NP_ABLE = 1: Link partner, next page available LP_NP_ABLE = 0: Link partner, no next page
2	NP_ABLE	0,RO/P	Local Device Next Page Able NP_ABLE = 1: DM9003, next page available NP_ABLE = 0: DM9003, no next page DM9003 does not support this function, so this bit is always 0
1	PAGE_RX	0, RO	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able A "1" in this bit indicates that the link partner supports Auto-negotiation

8.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Bit Name	Default	Description
15	BP_4B5B	0,RW	Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
14	BP_SCR	0, RW	Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
13	BP_ALIGN	0, RW	Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
12	BP_ADPOK	0, RW	BYPASS ADPOK Force signal detector (SD) active. This register is for debug only, not release to customer 1: Forced SD is OK, 0: Normal operation
11	Reserved	RW	Reserved Force to 0 in application
10	TX	1, RW	100BASE-TX Mode Control 1 = 100BASE-TX operation 0 = 100BASE-FX operation
9	Reserved	0, RO	Reserved
8	Reserved	0, RW	Reserved
7	F_LINK_100	0, RW	Force Good Link in 100Mbps 1 = Force 100Mbps good link status 0 = Normal 100Mbps operation This bit is useful for diagnostic purposes
6	Reserved	0, RW	Reserved Force to 0 in application.
5	COL_LED	0, RW	COL LED Control (valid in PHY test mode)
4	RPDCTR-EN	1, RW	Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 1 = Enable automatic reduced power down 0 = Disable automatic reduced power down
3	SMRST	0, RW	Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed
2	MFPSC	1, RW	MF Preamble Suppression Control MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
1	SLEEP	0, RW	Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset

0	RLOUT	0, RW	Remote Loop out Control When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

Bit	Bit Name	Default	Description
15	100FDX	1, RO	100M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
14	100HDX	1, RO	100M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
13	10FDX	1, RO	10M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
12	10HDX	1, RO	10M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
11	Reserved	0, RO	Reserved Read as 0, ignore on write
10	Reserved	0,RW	Reserved
9	Reserved	0,RW	Reserved
8-4	PHYADR[4:0]	1, RW	PHY Address Bit 4:0 The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY
3-0	ANMB[3:0]	0, RO	Auto-negotiation Monitor Bits These bits are for debug only. The auto-negotiation status will be written to these bits.

B3	b2	b1	B0	
0	0	0	0	In IDLE state
0	0	0	1	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detects signal link ready
0	1	1	1	Parallel detects signal link ready fail
1	0	0	0	Auto-negotiation completed successfully

8.10 10BASE-T Configuration/Status (10BTCSR) – 12H

Bit	Bit Name	Default	Description
15	Reserved	0, RO	Reserved Read as 0, ignore on write
14	LP_EN	1, RW	Link Pulse Enable 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation
13	HBE	1,RW	Heartbeat Enable 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DM9003 is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode)
12	SQUELCH	1, RW	Squelch Enable 1 = Normal squelch 0 = Low squelch
11	JABEN	1, RW	Jabber Enable Enables or disables the Jabber function when the DM9003 is in 10BASE-T full duplex or 10BASE-T transceiver Loopback mode 1 = Jabber function enabled 0 = Jabber function disabled
10	SERIAL	0, RW	10M Serial Mode (valid in PHY test mode) Force to 0, in application.
9-1	Reserved	0, RO	Reserved Read as 0, ignore on write
0	POLR	0, RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module

8.11 Power Down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
15-9	Reserved	0, RO	Reserved Read as 0, ignore on write
8	PD10DRV	0, RW	Vendor power down control test
7	PD100DL	0, RW	Vendor power down control test
6	PDchip	0, RW	Vendor power down control test
5	PDcrm	0, RW	Vendor power down control test
4	PDaeq	0, RW	Vendor power down control test
3	PDdrv	0, RW	Vendor power down control test
2	PDedi	0, RW	Vendor power down control test
1	PDedo	0, RW	Vendor power down control test
0	PD10	0, RW	Vendor power down control test

***** When selected, the power down value is control by Register 20.0

8.12 (Specified config) Register – 14H

Bit	Bit Name	Default	Description
15	TSTSE1	0,RW	Vendor test select 1 control
14	TSTSE2	0,RW	Vendor test select 2 control
13	FORCE_TXSD	0,RW	Force Signal Detect 1: force SD signal OK in 100M 0: normal SD signal.
12	FORCE_FEF	0,RW	Vendor test select control
11	PREAMBLEX	0,RW	Preamble Saving Control 0: when bit 10 is set, the 10M TX preamble count is reduced. When bit 11 of register 29 is set, 12-bit preamble bit is reduced; otherwise 22-bit preamble bits is reduced. 1: 10M TX preamble bit count is normal.
10	TX10M_PWR	1,RW	10M TX Power Saving Control 1: enable 10M TX power saving 0: disable 10M TX power saving
9	NWAY_PWR	0,RW	N-Way Power Saving Control 1: disable N-Way power saving 0: enable N-Way power saving
8	Reserved	0, RO	Reserved Read as 0, ignore on write
7	MDIX_CNTL	MDI/MDIX,RO	The polarity of MDI/MDIX value 1: MDIX mode 0: MDI mode
6	AutoNeg_dpbk	0,RW	Auto-negotiation Loopback 1: test internal digital auto-negotiation Loopback 0: normal.
5	Mdix_fix Value	0, RW	MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value.
4	Mdix_down	0,RW	MDIX Down Manual force MDI/MDIX. 0: Enable *HP* Auto-MDIX 1: Disable *HP* Auto-MDIX , MDIX_CNTL value depend on Reg.14H.bit5
3	MonSel1	0,RW	Vendor monitor select 1
2	MonSel0	0,RW	Vendor monitor select 0
1	Reserved	0,RW	Reserved Force to 0, in application.
0	PD_value	0,RW	Power down control value Decision the value of each field Reg.13H. 1: power down 0: normal

8.13 DAVICOM Specified Receive Error Counter Register (RECR) – 16H

Bit	Bit Name	Default	Description
15-0	Rcv_ Err_ Cnt	0, RO	Receive Error Counter Receive error counter that increments upon detection of RXER. Clean by reading this register.

8.14 DAVICOM Specified Disconnect Counter Register (DISCR) – 17H

Bit	Bit Name	Default	Description
15-8	Reserved	0, RO	Reserved
7-0	Disconnect Counter	0, RO	Disconnect Counter that increment upon detection of disconnection. Clean by reading this register.

8.15 Power Saving Control Register (PSCR) – 1DH

Bit	Bit Name	Default	Description
15-12	RESERVED	0,RO	RESERVED
11	PREAMBLEX	0,RW	Preamble Saving Control when both bit 10and 11 of register 20 are set, the 10M TX preamble count is reduced. 1: 12-bit preamble bit is reduced. 0: 22-bit preamble bits is reduced.
10	AMPLITUDE	0,RW	10M TX Amplitude Control Disabled 0: when cable is unconnected with link partner, the TX amplitude is reduced for power saving. 1: disable TX amplitude reduce function
9	TX_PWR	0.RW	TX Power Saving Control Disabled 0: when cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 1: disable TX driving power saving function
8-0	RESERVED	0,RO	RESERVED

9. FUNCTIONAL DESCRIPTION

9.1 Processor bus and memory management function:

9.1.1 Processor Interface

In the general processor mode, the chip selection is just coming from pin CS#. There are only two addressing ports through the access of the host interface.

One port is the INDEX port and the other is the DATA port. The INDEX port is decoded by the CMD pin=0 and the DATA by the CMD pin=1. The contents of the INDEX port are the register address of the DATA port. Before the access of any register, the address of the register must be saved in the INDEX port before.

9.1.2 Direct Memory Access Control

The DM9003 provides DMA capability to simplify the access of the internal memory. After the setting of the starting address of the internal memory and then issuing a dummy read/write command to load the current data to internal data buffer, the desired location of the internal memory can be accessed by the read/write command registers. The memory's address will be increased with the size equal to the current operation mode (i.e. the byte or word mode) and the data of the next location will be loaded to internal data buffer automatically. It is noted that the data of the first access (the dummy read/write command) in a sequential burst should be ignored because that the data was the contents of the last read/write command.

There are two configured types of internal memory which are controlled by bit 7 of IMR. When the bit 7 of IMR is set, the internal memory is used for transmit and receive buffers. The transmit buffer occupies 8K bytes. And the receive buffer occupies 7.75K bytes. Both the transmit and receive buffer address need not to be programmed instead that they are managed by the DM9003 automatically. In transmit function, after power on reset or each time after the transmit command is issued (bit 0 of TCR is set), the next starting transmit buffer address is loaded. In receive function, the 7.75K-byte receive buffer can be treated as a continued logic memory space. The memory address will wrap to address 0 if the end of address is reached.

When the bit 7 of IMR is cleared, there is a 64K-byte memory space in the DM9003 can be accessed. This configured type of internal memory is used for testing only. The memory write address (register FAh/FBh) and the memory read address (register F4h/F5h) represent the physical memory address of the DM9003 internal memory. It is noted that after the memory had been written by memory write command, the switch reset command (bit 6 of register 52h) should be set before normal switch function operation, since the controlled data in internal memory may be corrupted.

9.1.3 Packet Transmission

There are two packets, sequentially named as index I and index II, can be stored in the TX SRAM at the same time. The index register 02h controls the insertion of CRC.

The start address of transmission is 00h and the current packet is index I after software or hardware reset. Firstly write data to the TX SRAM using the DMA port and then write the byte count to byte count register at index register 0fch and 0fdh. Set the bit 1 of control register. The DM9003 starts to transmit the index I packet. Before the transmission of the index I packet ends, the data of the next (index II) packet can be moved to TX SRAM. After the index I packet ends the transmission, write the byte count data of the index II to BYTE_COUNT register and then set the bit 1 of control register to transmit the index II packet. The following packets, named index I, II, I, II… use the same way to be transmitted.

9.1.4 Packet Reception

The RX SRAM is a ring data structure. Each packet has a 4-byte header followed with the data of the reception packet which CRC field is included. The format of the 4-byte header is 01h, status, BYTE_COUNT low, and BYTE_COUNT high. It is noted that the start address of each packet is in the proper address boundary which depends on the operation mode (byte or word mode).

9.2 Switch function:

9.2.1 Address Learning

The DM9003 has a self-learning mechanism for learning the MAC addresses of incoming packets in real time. DM9003 stores MAC addresses, port number and time stamp information in the Hash-based Address Table. It can learn up to 1K unicast address entry.

The switch engine updates address table with new entry if incoming packet's Source Address (SA) does not exist and incoming packet is valid (non-error and legal length).

Besides, DM9003 has an option to disable address learning for individual port. This feature can be set by bit 0 of register 65h

9.2.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time.

The period can be programmed or disabled through bit 0 & 1 of register 52h.

9.2.3 Packet Forwarding

The DM9003 forwards the incoming packet according to following decision:

(1). If DA is Multicast/Broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.

(2). Switch engine would look up address table based on DA when incoming packets is UNICAST. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.

(3). Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM9003 will filter incoming packets under following conditions:

(1). Error packets, including CRC errors, alignment errors, illegal size errors.

(2). PAUSE packets.

(3). If incoming packet is UNICAST and its destination port number is equal to source port number.

9.2.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

9.2.5 Back-off Algorithm

The DM9003 implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

9.2.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

9.2.7 Half Duplex Flow Control

The DM9003 supports IEEE standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, The DM9003 will defer transmitting next normal frames, if it receives a pause frame from link partner.

On the transmit side, The DM9003 issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM9003 sends out a pause frame with zero pause time allows traffic to resume immediately.

9.2.8 Full Duplex Flow Control

The DM9003 supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM9003 sends jam pattern, thus forcing a collision.

The flow control ability can be set in bit 4 of register 61h.

9.2.9 Partition Mode

The DM9003 provides a partition mode for each port, see bit 6 of register 61h. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good

packet is seen on the wire. The detail description of partition mode represent following:

(1). Entering Partition State

A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

(2). While in Partition state:

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

(3). Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

9.2.10 Broadcast Storm Filtering

The DM9003 has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two type of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through bit 1 of register 61h.

The broadcast storm threshold can be programmed by EEPROM or register 67h, the default setting is no broadcast storm protecting.

9.2.11 Bandwidth Control

The DM9003 supports two type of bandwidth control for each port. One is the ingress and egress bandwidth rate can be control separately, the other is combined together, this function can be set through bit 3 of register 61h. The bandwidth control is disabled by default.

For separated bandwidth control mode, the threshold rate is defined in register 66h. For combined mode, it is defined in register 67h.

The behavior of bandwidth control as below:

(1).For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.

(2).For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.

(3).In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

9.2.12 Port Monitoring Support

The DM9003 supports “Port Monitoring” function on per port base, detail as below:

(1). Sniffer Port and Monitor Port

There is only one port can be selected as “sniffer port” by register 52h, multiple ports can be set as “receive monitor port” or “transmit monitor port” in per-port register 65h.

(2).Receive monitor

All packets received on the “receive monitor port” are send a copy to “sniffer port”. For example, port 0 is set as “receive monitor port” and port 3 (processor port) is selected as “sniffer port”. If a packet is received form port 0 and destined to port 1 after forwarding decision, the DM9003 will forward it to port 1 and processor port in the end.

(3).Transmit monitor

All packets transmitted on the “transmit monitor port” are send a copy to “sniffer port”. For example, port 1 is set as “transmit monitor port” and processor port is selected as “sniffer port”. If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM9003 will forward it to port 1 and processor port in the end.

(4).Exception

The DM9003 has an optional setting that broadcast/multicast packets are not monitored (see bit 4 of register 65h). It’s useful to avoid unnecessary bandwidth.

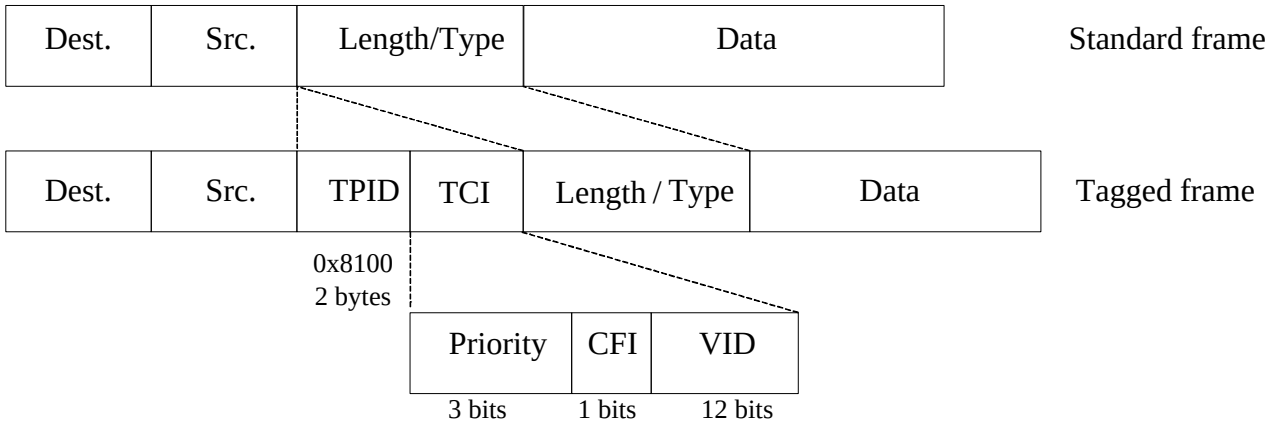
9.2.13 VLAN Support

9.2.13.1 Port-Based VLAN

The DM9003 supports port-based VLAN as default, up to 16 groups. Each port has a default VID called PVID (Port VID, see register 6Fh). The DM9003 used LSB 4-bytes of PVID as index and mapped to register B0h~BFh, to define the VLAN groups.

9.2.13.2 802.1Q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).



The DM9003 also supports 16 802.1Q-based VLAN groups, as specified in bit 1 of register 53h. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM9003 used LSB 4-bytes VID of received packet with VLAN tag and VLAN Group Mapping Register (B0h~BFh) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.

9.2.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by bit 7 of register 6Dh in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

(1). Receive untagged packet and forward to Un-tag port.

Received packet will forward to destination port without modification.

(2). Receive tagged packet and forward to Un-tag port.

The DM9003 will remove the tag from the packet and recalculate CRC before sending it out.

(3). Receive untagged packet and forward to Tag port.

The DM9003 will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

(4). Receive tagged packet and forward to Tag port.

Received packet will forward to destination port without modification.

9.2.14 Priority Support

The DM9003 supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM9003 provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM9003 offers four level queues for transmit on per-port based.

The DM9003 provides two packet scheduling algorithms: Weighted Round-Robin Queuing and

Strict Priority Queuing. Weighted Round-Robin Queuing (WRR) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The Packet on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in bit 5 of register 6Dh.

9.2.14.1 Port-Based Priority

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in bit 0 and 1 of register 6Dh.

9.2.14.2 802.1p-Based Priority

802.1p priority can be disabled by bit 2 of register 6Dh, it is enabled by default.

The DM9003 extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers (D0h~D1h) to determine which transmit queue is designated. The VLAN Priority Map is programmable.

9.2.14.3 DiffServ-Based Priority

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (C0h~CFh) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see bit 7 of register 53h.

9.3 Internal PHY functions

9.3.1 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.3.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

9.3.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.3.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

9.3.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

9.3.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic one event.

9.3.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.3.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

9.3.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.3.2.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.3.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.3.2.3 MLT-3 to NRZI Decoder

The DM9003 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.3.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.3.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.3.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.3.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.3.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected and subsequent data is aligned on a fixed boundary.

9.3.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.3.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9003 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.3.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.3.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during receive operations.

9.3.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

10. DC AND AC ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC3	3.3V Supply Voltage	-0.3	3.6	V	
VCCI	1.8V core power supply	-0.3	1.95	V	
AVDD3	Analog power supply 3.3V	-0.3	3.6	V	
AVDDI	Analog power supply 1.8V	-0.3	1.95	V	
V_{IN}	DC Input Voltage (VIN)	-0.5	5.5	V	
T_{STG}	Storage Temperature range	-65	+150	°C	
T_A	Ambient Temperature	0	+70	°C	
L_T	Lead Temperature (TL, soldering, 10 sec.).	-	+260	°C	Lead-free Device

10.2 Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC3	3.3V Supply Voltage	3.135	3.465	V	
VCCI	1.8V core power supply	1.71	1.89	V	
AVDD3	Analog power supply 3.3V	3.135	3.465	V	
AVDDI	Analog power supply 1.8V	1.71	1.89	V	
P_D (Power Dissipation)	100BASE-TX	-	230	mA	1.8V only
		-	70	mA	3.3V only
	10BASE-TX		140	mA	TX idle, 1.8V only
			250	mA	50% utilization, 1.8V only
			360	mA	100% utilization, 1.8V only
			30	mA	3.3V only
	Auto-negotiation or cable off		170	mA	1.8V only
			40	mA	3.3V only

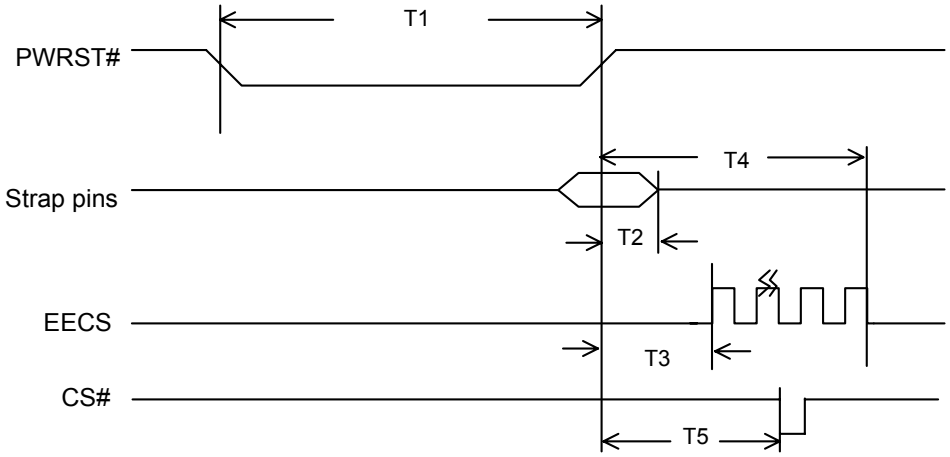
10.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL =4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	19	20	21	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	44	50	56	mA	Absolute Value

Note: Vcond1 = VCC3 = 3.3V, VCCI = 1.8V, AVDD3 = 3.3V, AVDDI = 1.8V.

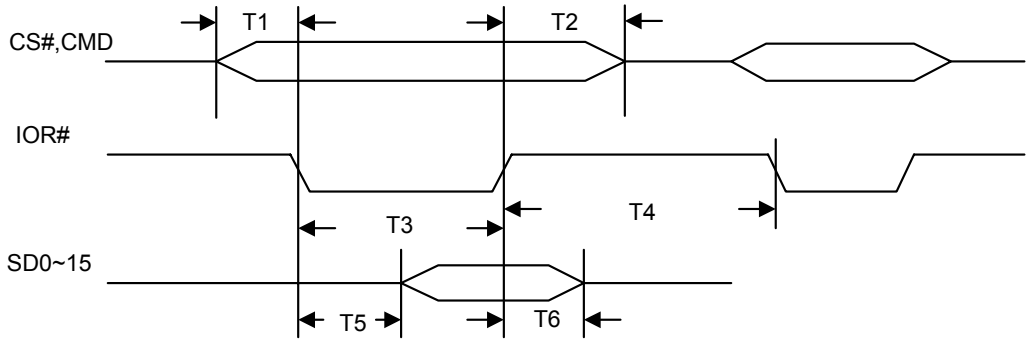
10.4 AC characteristics

10.4.1 Power On Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PWRST# Low Period	1	-	-	ms	-
T2	Strap pin hold time with PWRST#	40	-	-	ns	-
T3	PWRST# high to EECS high	-	5	-	us	-
T4	PWRST# high to EECS burst end	-	--	4	ms	-
T5	PWRST# high to CS# available	--	400	--	us	-

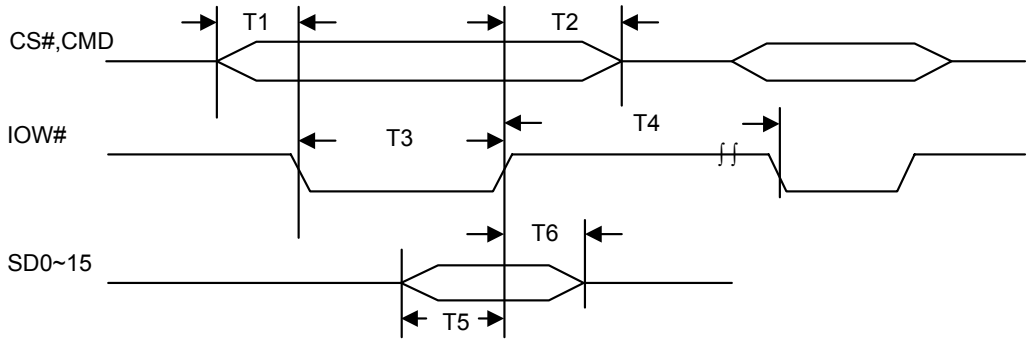
10.4.2 Processor I/O Read Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CS#,CMD valid to IOR# valid	5			ns
T2	IOR# invalid to CS#,CMD invalid	5			ns
T3	IOR# width	20			ns
T4	IOR# invalid to next IOR#/IOW# valid When read DM9003 register	2			clk*
T4	IOR# invalid to next IOR#/IOW# valid When read DM9003 memory with F0h register	4			clk*
T3+T4	IOR# invalid to next IOR#/IOW# valid When read DM9003 memory with F2h register	1			clk*
T5	System Data(SD) Delay time			25	ns
T6	IOR# invalid to System Data(SD) invalid			10	ns

Note: the Unit: clk is under the internal system clock 50MHz.

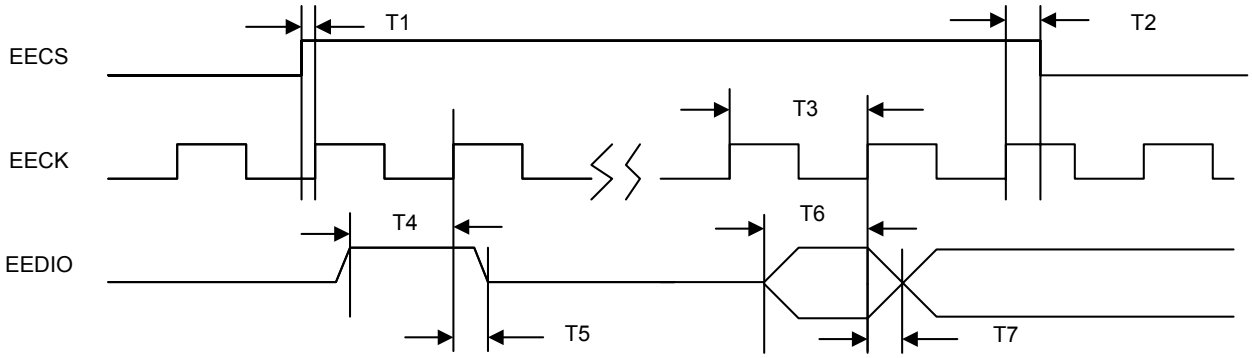
10.4.3 Processor I/O Write Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CS#,CMD valid to IOW# valid	5			ns
T2	IOW# Invalid to CS#,CMD Invalid	5			ns
T3	IOW# Width	20			ns
T4	IOW# Invalid to next IOW#/IOR# valid When write DM9003 INDEX port	1			clk*
T4	IOW# Invalid to next IOW#/IOR# valid When write DM9003 DATA port	2			clk*
T3+T4	IOW# Invalid to next IOW#/IOR# valid When write DM9003 memory	1			clk*
T5	System Data(SD) Setup Time	5			ns
T6	System Data(SD) Hold Time	3			ns

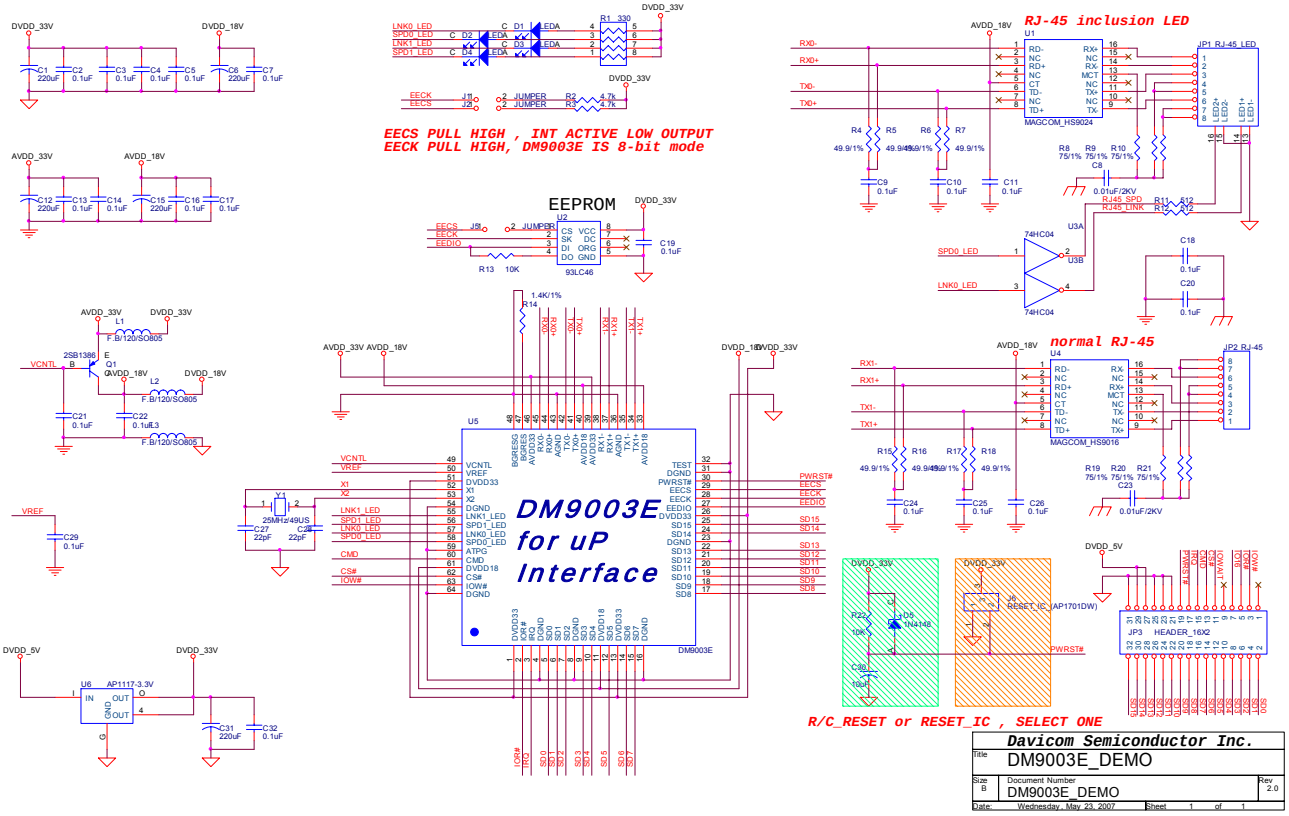
Note: the Unit: clk is under the internal system clock 50MHz.

10.4.4 EEPROM timing



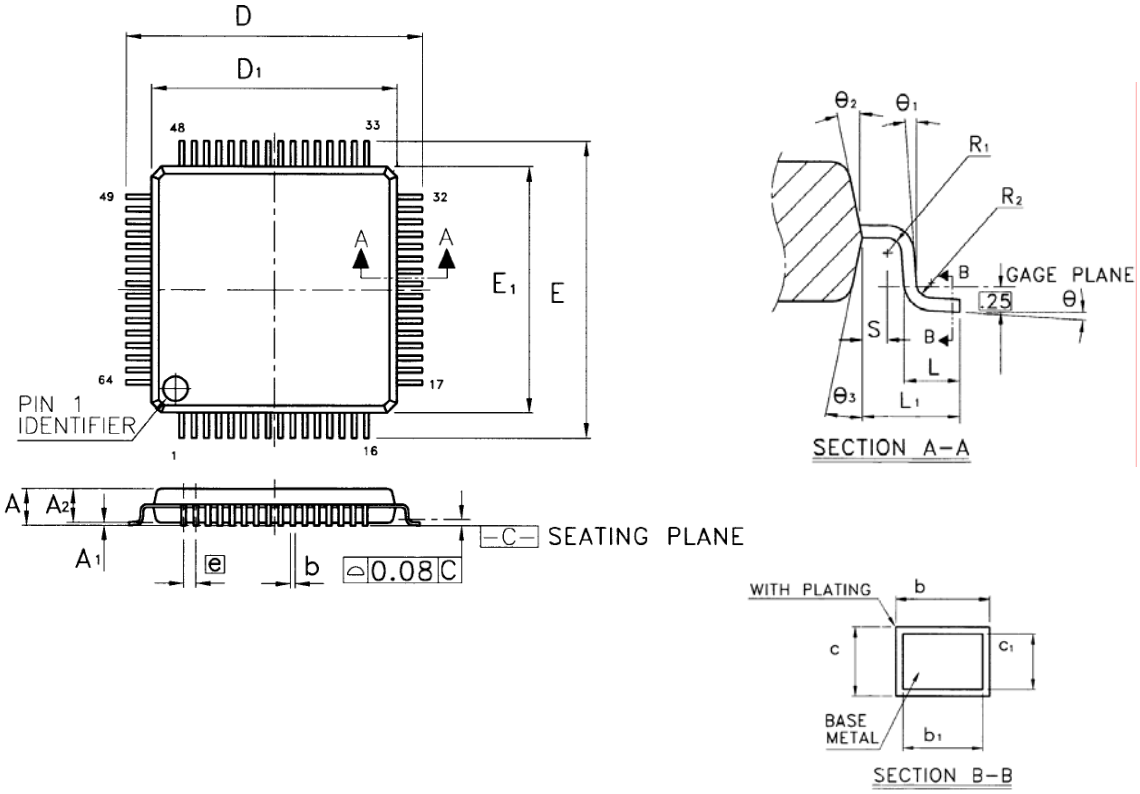
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECS Setup Time		480		ns
T2	EECS Hold Time		2080		ns
T3	EECK Frequency		0.38		MHz
T4	EEDIO Setup Time in output state		460		ns
T5	EEDIO Hold Time in output state		2100		ns
T6	EEDIO Setup Time in input state	8			ns
T7	EEDIO Hold Time in input state	8			ns

11. APPLICATION CIRCUIT



12. PACKAGE INFORMATION

64 Pins LQFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	-	-	1.60		-	-	0.063
A_1	0.05	-	0.15		0.002	-	0.006
A_2	1.35	1.40	1.45		0.053	0.055	0.057
b	0.17	0.22	0.27		0.007	0.009	0.011
b_1	0.17	0.20	0.23		0.007	0.008	0.009
c	0.09	-	0.20		0.004	-	0.008
c_1	0.09	-	0.16		0.004	-	0.006
D	12.00 BSC				0.472 BSC		
D_1	10.00 BSC				0.394 BSC		
E	12.00 BSC				0.472 BSC		
E_1	10.00 BSC				0.394 BSC		
e	0.50 BSC				0.020 BSC		
L	0.45	0.60	0.75		0.018	0.024	0.030
L_1	1.00 REF				0.039 REF		
R_1	0.08	-	-		0.003	-	-
R_2	0.08	-	0.20		0.003	-	0.008
S	0.20	-	-		0.008	-	-
θ	0°	3.5°	7°		0°	3.5°	7°
θ_1	0°	-	-		0°	-	-
θ_2	12° TYP				12° TYP		
θ_3	12° TYP				12° TYP		

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

13. ORDERING INFORMATION

Part Number	Pin Count	Package
DM9003EP	64	LQFP (Pb-free)

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Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.