DAVICOM Semiconductor, Inc.

DM9051(I)

SPI to Ethernet Controller

DATA SHEET

Version: DM9051(I)-12-MCO-DS-P01

March 30, 2015

Content

1 General Description

The DM9051(I) is a fully integrated and cost-effective low pin count single chip Fast Ethernet controller with a Serial Peripheral Interface (SPI), a 10/100M PHY and MAC, and 16K-byte SRAM. It is designed with low power and high performance process interface that support 3.3V with 5V IO tolerance.

The PHY of the DM9051(I) can interface to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX with HP Auto-MDIX.It is fully compliant with the IEEE 802.3u Spec. Its Auto-Negotiation function will automatically configure the DM9051(I) to take the maximum advantage of its 10M or 100M abilities.

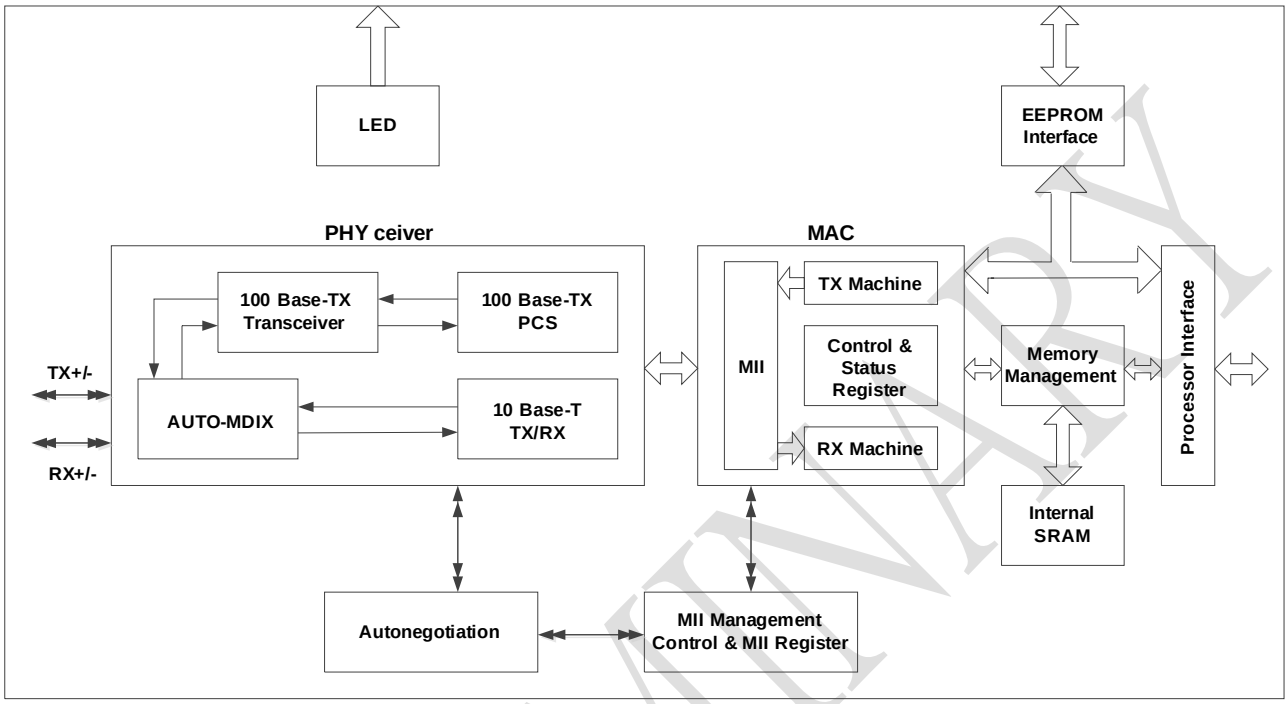
The DM9051(I) supports IEEE 802.3az in PHY and MAC to save power consumption when Ethernet is idle. The IEEE 802.3x Full-Duplex flow control and Half-Duplex back-pressure function also supported to avoid Ethernet packet loss with link partner.

The slave SPI interface is designed to support SPI clock mode 0 and 3 that compatible with the all master SPI interface of CPU. The clock speed can up to 50Mhz to co-operation with most high throughput master SPI. The SPI burst command format is code-effective to minimize the command overhead in access DM9051(I) internal registers and packet data in memory.

2 Features

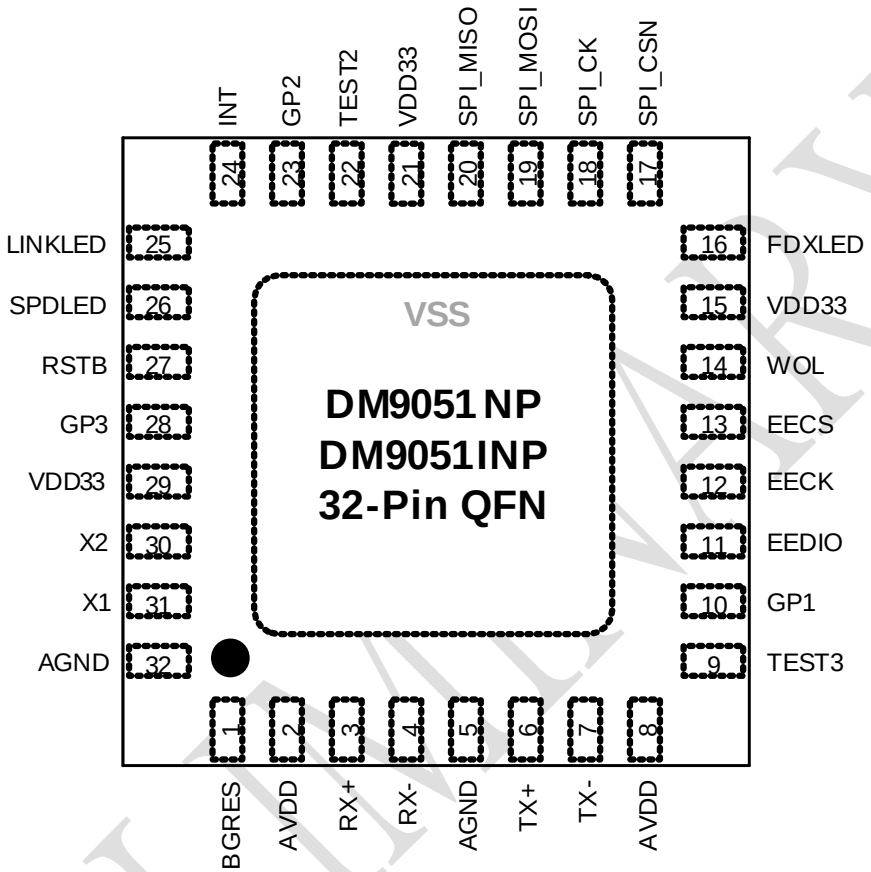
- Slave SPI Interface with clock speeds up to 50MHz for high throughput applications
- Support SPI clock mode 0 and 3
- Support 10BASE-T and 100BASE-TX and 100M Fiber interface
- Support HP Auto-MDIX crossover function in 10BASE-T and 100BASE-TX
- Support IEEE 802.3az Energy Efficient Ethernet (EEE)
- Support interface for EEPROM to configure chip settings
- Support back pressure flow control for Half-Duplex mode
- Support IEEE802.3x flow control for Full-Duplex mode
- Supports wakeup frame, link status change and magic packet events to generate remote wake on LAN (WOL) signal
- Support IPv4/ TCP / UDP checksum generation and checking
- Configurable of internal transmit/receive buffers within 16K-byte memory
- Built-in integrated 3.3V to 1.8V low noise regulator for core and analog blocks
- Support EMI (Class B) and HBM ESD Rating 8KV
- Support Industrial Temperature Range: –40℃ to +85℃ (DM9051I)
- 3.3V I/O with 5V tolerant
- DSP architecture PHY Transceiver
- 0.18um process

3 Block Diagram



4 Pin Configuration

4.1 32-Pin QFN



Note: The DM9051(I) IC employs a QFN package, which means the absence of a pin dedicated to ground (GND). In the QFN package, the GND is located at the bottom of the IC directly in the middle. Exposed pad (VSS) on bottom of package must be connected to ground.

5 Pin Description

Buffer Type			
I = Input	O = Output	I/O = Input/Output	P = Power
O/D = Open Drain		PD = Internal Pull-low about 60K	PU = Internal Pull-high about 60K

5.1 SPI Processor Interface

Pin No.	Pin Name	Type	Description
17	SPI_CSN	I,PU	**SPI Chip Select** The low active chip select pin from master SPI.
18	SPI_CK	I,PD	**SPI Clock** The SPI clock mode 0 or 3 from master SPI.
19	SPI_MOSI	I	**SPI Data In** The data pin from master SPI.
20	SPI_MISO	O,PD	**SPI Data Out** The data pin to master SPI.
24	INT	O,PD	**Interrupt Request** This pin is high active at default; its polarity can be modified by EEPROM setting or by strap pin EECK or by MAC register 39H. See the EEPROM content and MAC register 39H description for detailed.

5.2 EEPROM Interface

Pin No.	Pin Name	Type	Description
11	EEDIO	I/O,PD	**EEPROM IO Data** The IO data pin to or from EEPROM.
12	EECK	O,PD	**EEPROM Clock** The clock pin to EEPROM. This pin is also used as the strap pin of the polarity of the INT pin. When this pin is pulled-high, the INT pin is low active; otherwise the INT pin is high active.
13	EECS	O,PD	**EEPROM Chip Select** The high active chip select to EEPROM.

5.3 Clock Interface

Pin No.	Pin Name	Type	Description
30	X2	O	Crystal 25MHz Out
31	X1	I	Crystal 25MHz In

5.4 LED Interface

Pin No.	Pin Name	Type	Description
16	FDXLED	O/D	**Full-Duplex LED** In LED mode 1, its low output indicates that the internal PHY is operated in Full-Duplex mode, or it is floating for the Half-Duplex mode of the internal PHY. In LED mode 0, its low output indicates that the internal PHY is operated in 10M mode, or it is floating for the 100M mode of the internal PHY. More LED modes are controlled by MAC register 57H
25	LINKLED	O/D	**Link / Active LED** In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY. In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only. More LED modes are controlled by MAC register 57H.
26	SPDLED	O/D	**Speed LED** Its low output indicates that the internal PHY is operated in 100M/S, or it is floating for the 10M mode of the internal PHY. More LED modes are controlled by MAC register 57H.

Note: LED mode 0 or 1 is defined in MAC register 2DH or EEPROM setting.

5.5 10/100 PHY/Fiber

Pin No.	Pin Name	Type	Description
1	BGRES	I/O	**Band gap Pin, 6.8K Resistor** Connect a 6.8K 1% resistor to this pin and pin 5 AGND.
2,8	AVDD	P	**1.8V Power Output** The 1.8V regulator output pin. Please do not use the pin as devices power source except the central tap of transformer.
3,4	RX+/ RX-	I/O	**RX+/-** The RX input in 10BASE-T/100BASE-TX MDI mode or TX output in 10BASE-T/100BASE-TX MDIX mode. In 100M Fiber mode, these pins are for RX input only.
5,32	AGND	P	Analog Ground
6,7	TX+/ TX-	I/O	**TX+/-** The TX output in 10BASE-T/100BASE-TX MDI mode or RX input in 10BASE-T/100BASE-TX MDIX mode. In 100M Fiber mode, these pins are for TX output only.

5.6 Miscellaneous

Pin No.	Pin Name	Type	Description
9	TEST3	I,PD	**Operation Mode** Force to high in normal application
10	GP1	I/O	**General Purpose Pin 1** This is a general purpose pin controlled by bit 1 of MAC register 1EH/1FH.
14	WOL	O,PD	**Wake On Lan** This is a control signal when wake up event occurred. Its polarity and output type can be controlled by EEPROM setting.
22	TEST2	I,PD	**Operation Mode** Force to ground in normal application
23	GP2	I/O	**General Purpose Pin 2** This is a general purpose pin controlled by bit 2 of MAC register 1EH/1FH.
27	RSTB	I	**Power on Reset** Active low signal to initiate the DM9051(I). The DM9051(I) is ready after 5us when this pin disserted.
28	GP3	I/O,PD	**General Purpose Pin 3** This is a general purpose pin controlled by bit 3 of MAC register 1EH/1FH.

5.7 Power Pins

Pin No.	Pin Name	Type	Description
15,21,29	VDD33	P	**VDD** 3.3V power input
33	VSS	P	The QFN package ground

5.8 Strap Pins

Pin No.	Pin Name	Description
12	EECK	**Polarity of INT** 1 = INT pin low active 0 = INT pin high active
13	EECS	**BIST Control** 1 = Enable BIST 0 = Disable BIST
14	WOL	**INT Output Type** 1 = Open-Drain 0 = Push-pull mode

Note: If memory BIST function is enabled, the SPI interface should not active before RSTB go high 2ms.

6 MAC Control and Status Register Set

The DM9051(I) implements several control and status registers, which can be accessed by the host. These CSRs are byte aligned. All CSRs are set to their default values by hardware or software reset unless they are specified.

Register	Description	Offset	Default Value after Reset
NCR	Network Control Register	00H	00H
NSR	Network Status Register	01H	00H
TCR	TX Control Register	02H	00H
TSR I	TX Status Register I	03H	00H
TSR II	TX Status Register II	04H	00H
RCR	RX Control Register	05H	00H
RSR	RX Status Register	06H	00H
ROCR	Receive Overflow Counter Register	07H	00H
BPTR	Back Pressure Threshold Register	08H	37H
FCTR	Flow Control Threshold Register	09H	38H
FCR	RX/TX Flow Control Register	0AH	00H
EPCR	EEPROM & PHY Control Register	0BH	00H
EPAR	EEPROM & PHY Address Register	0CH	40H
EPDRL	EEPROM & PHY Low Byte Data Register	0DH	XXH
EPDRH	EEPROM & PHY High Byte Data Register	0EH	XXH
WCR	Wake Up Control Register	0FH	00H
PAR	Physical Address Register	10H-15H	Determined by EEPROM
MAR	Multicast Address Hash Table Register	16H-1DH	XXH
GPCR	General Purpose Control Register	1EH	71H
GPR	General Purpose Register	1FH	XXH
TRPAL	TX Memory Read Pointer Address Low Byte	22H	00H
TRPAH	TX Memory Read Pointer Address High Byte	23H	00H
RWPAL	RX Memory Write Pointer Address Low Byte	24H	00H
RWPAH	RX Memory Write Pointer Address High Byte	25H	0CH
VID	Vendor ID	28H-29H	0A46H
PID	Product ID	2AH-2BH	9051H
CHIPR	CHIP Revision	2CH	01H
TCR2	Transmit Control Register 2	2DH	00H
ATCR	Auto-Transmit Control Register	30H	00H
TCSCR	Transmit Check Sum Control Register	31H	00H
RCSCSR	Receive Check Sum Control Status Register	32H	00H
SBCR	SPI Bus Control Register	38H	44H
INTCR	INT Pin Control Register	39H	00H
PPCSR	Pause Packet Control Status Register	3DH	01H
EEE_IN	IEEE 802.3az Enter Counter Register	3EH	05H
EEE_OUT	IEEE 802.3az Leave Counter Register	3FH	0FH
ALNCR	SPI Byte Align Error Counter Register	4AH	00H
RLENCR	RX Packet Length Control Register	52H	00H
BCASTCR	RX Broadcast Control Register	53H	00H
INTCKCR	INT Pin Clock Output Control Register	54H	00H
MPTRCR	Memory Pointer Control Register	55H	00H
MLEDCR	More LED Control Register	57H	00H
MEMSCR	Memory Control Register	59H	00H
TMEMR	Transmit Memory Size Register	5AH	03H
MBSR	Memory BIST Status Register	5DH	40H

MRCMDX	Memory Data Pre-Fetch Read Command Without Address Increment Register	70H	XXH
MRCMDX1	Memory Read Command Without Pre-Fetch and Without Address Increment Register	71H	XXH
MRCMD	Memory Data Read Command With Address Increment Register	72H	XXH
SDR_DLY	SPI Data Read Delay Counter Register	73H	00H
MRRL	Memory Data Read Address Register Low Byte	74H	00H
MRRH	Memory Data Read Address Register High Byte	75H	00H
MWCMDX	Memory Data Write Command Without Address Increment Register	76H	XXH
MWCMD	Memory Data Write Command With Address Increment Register	78H	XXH
MWRL	Memory Data Write Address Register Low Byte	7AH	00H
MWRH	Memory Data Write Address Register High Byte	7BH	00H
TXPLL	TX Packet Length Low Byte Register	7CH	XXH
TXPLH	TX Packet Length High Byte Register	7DH	XXH
ISR	Interrupt Status Register	7EH	00H
IMR	Interrupt Mask Register	7FH	00H

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>:
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- P = Power on reset default value
- H = Hardware reset default value
- S = Software reset default value
- E = Default value from EEPROM
- T = Default value from strap pin
- h = Hex, format

<Access Type>:
- RO = Read Only
- RW = Read/Write
- R/C = Read and Clear

RW/C1=Read/Write and Cleared by write 1 WO = Write Only
Reserved bits are shaded and should be written with 0. Reserved bits are undefined on read access.

6.1 Network Control Register (00H)

Bit	Bit Name	Default	Description
7	RESERVED	P0,RW	Reserved
6	WAKEEN	P0,RW	**Enables Wakeup Function** Clearing this bit will also clears all wakeup event status. This bit will not be affected after a software reset. 1 = Enable 0 = Disable
5	RESERVED	0,RO	Reserved
4	FCOL	PS0,RW	**Force Collision Mode** 1 = Force Collision Mode, used for testing 0 = Disable
3	FDX	PS0,RO	**Duplex Mode of the Internal PHY** 1 = Full-Duplex 0 = Half-Duplex
2:1	LBK	PS00,RW	**Loopback Mode** Bit: 2 1 0 0 Normal 0 1 MAC Internal loopback 1 0 Internal PHY 100M mode digital loopback 1 1 (Reserved)
0	RST	P0,RW	**Software Reset and Auto-Clear after 10us** 1 = Reset state 0 = Non-reset state

6.2 Network Status Register (01H)

Bit	Bit Name	Default	Description
7	SPEED	X,RO	**Speed of Internal PHY** This bit has no meaning when LINKST=0 1 = 10Mbps 0 = 100Mbps
6	LINKST	X,RO	**Link Status of Internal PHY** 1 = Link OK 0 = Link failed
5	WAKEST	P0, RW/C1	**Wakeup Event Status** Clears by read or write 1. This bit will not be affected after software reset. 1 = Wakeup event 0 = No wakeup event
4	RESERVED	0,RO	Reserved
3	TX2END	PS1, RW/C1	**TX Packet Index II Complete Status** Auto-Clear at begin transmitting of TX packet index II and Auto-Set at the end of transmitting of TX packet index II. 1 = Transmit completion or idle of packet index II 0 = Packet index II transmit in progress
2	TX1END	PS1, RW/C1	**TX Packet Index I Complete Status** Auto-Clear at begin transmitting of TX packet index I and Auto-Set at the end of transmitting of TX packet index I. 1 = Transmit completion or idle of packet index I 0 = Packet index I transmit in progress

1	RXOV	PS0,RO	**RX Memory Overflow Status** 1 = RX memory Overflow 0 = Non-overflow
0	RXRDY	PS0,RO	**RX Packet Ready** 1 = Have packet in RX memory 0 = No packet in RX memory

6.3 TX Control Register (02H)

Bit	Bit Name	Default	Description
7	RESERVED	0,RO	Reserved
6	TJDIS	PS0,RW	**Transmit Jabber Timer (2048 bytes) Control** 1 = Disabled. 0 = Enable
5	EXCECM	PS0,RW	**Excessive Collision Mode Control** 1 = Still tries to transmit this packet 0 = Aborts this packet when excessive collision counts more than 15
4	PAD_DIS2	PS0,RW	**PAD Appends for Packet Index II** 1 = Disable 0 = Enable
3	CRC_DIS2	PS0,RW	**CRC Appends for Packet Index II** 1 = Disable 0 = Enable
2	PAD_DIS1	PS0,RW	**PAD Appends for Packet Index I** 1 = Disable 0 = Enable
1	CRC_DIS1	PS0,RW	**CRC Appends for Packet Index I** 1 = Disable 0 = Enable
0	TXREQ	PS0,RW	**TX Request. Auto-Clear after Sending Completely** 1 = Transmit in progress 0 = No transmit in progress

6.4 TX Status Register I (03H) for Packet Index I

Bit	Bit Name	Default	Description
7	TJTO	PS0,RO	**Transmit Jabber Time Out** It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted. 1 = Timeout 0 = Non-timeout
6	LC	PS0,RO	**Loss of Carrier** It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode. 1 = Loss of carrier 0 = No carrier have been loss
5	NC	PS0,RO	**No Carrier** It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode. 1 = No carrier during transmit 0 = Normal carrier status during transmit
4	LC	PS0,RO	**Late Collision** It is set when a collision occurs after the collision window of 64 bytes. 1 = Late collision 0 = No late collision
3	COL	PS0,RO	**Collision Packet** It is set to indicate that the collision occurs during transmission. 1 = Have been collision 0 = No collision
2	EC	PS0,RO	**Excessive Collision** It is set to indicate that the transmission is aborted due to 16 excessive collisions. 1 = 16 excessive collisions 0 = Less than 16 collisions
1:0	RESERVED	0,RO	Reserved

6.5 TX Status Register II (04H) for packet index II

Bit	Bit Name	Default	Description
7	TJTO	PS0,RO	**Transmit Jabber Time Out** It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted. 1 = Timeout 0 = Non-timeout
6	LC	PS0,RO	**Loss of Carrier** It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode. 1 = Loss of carrier 0 = No carrier have been loss
5	NC	PS0,RO	**No Carrier** It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode. 1 = No carrier during transmit 0 = Normal carrier status during transmit
4	LC	PS0,RO	**Late Collision** It is set when a collision occurs after the collision window of 64 bytes. 1 = Late collision 0 = No late collision
3	COL	PS0,RO	**Collision Packet** It is set to indicate that the collision occurs during transmission. 1 = Have been collision 0 = No collision
2	EC	PS0,RO	**Excessive Collision** It is set to indicate that the transmission is aborted due to 16 excessive collisions. 1 = 16 excessive collisions 0 = Less than 16 collisions
1:0	RESERVED	0,RO	Reserved

6.6 RX Control Register (05H)

Bit	Bit Name	Default	Description
7	RESERVED	PS0,RW	Reserved
6	WTDIS	PS0,RW	**Watchdog Timer Disable** 1 = When set, the Watchdog Timer (2048 bytes) is disabled 0 = Otherwise it is enabled
5	DIS_LONG	PS0,RW	**Discard Long Packet** If Packet length is over 1522byte 1 = Enable 0 = Disable
4	DIS_CRC	PS0,RW	**Discard CRC Error Packet** 1 = Enable 0 = Disable
3	ALL	PS0,RW	**Receive All Multicast** To receive packet with multicast destination address 1 = Enable 0 = Disable
2	RUNT	PS0,RW	**Receive Runt Packet** To receive packet with size less than 64-bytes 1 = Enable 0 = Disable
1	PRMSC	PS0,RW	**Promiscuous Mode** To receive packet without destination address checking 1 = Enable 0 = Disable
0	RXEN	PS0,RW	**RX Enable** 1 = Enable 0 = Disable

6.7 RX Status Register (06H)

Bit	Bit Name	Default	Description
7	RF	PS0,RO	**Runt Frame** It is set to indicate that the size of the received frame is smaller than 64 bytes. 1 = Affirmative 0 = Negative
6	MF	PS0,RO	**Multicast Frame** It is set to indicate that the received frame has a multicast address. 1 = Affirmative 0 = Negative
5	LCS	PS0,RO	**Late Collision Seen** It is set to indicate that a late collision is found during the frame reception. 1 = Affirmative 0 = Negative
4	RWTO	PS0,RO	**Receive Watchdog Time-Out** It is set to indicate that it receives more than 2048 bytes. 1 = Affirmative 0 = Negative
3	PLE	PS0,RO	**Physical Layer Error** It is set to indicate that a physical layer error is found during the frame reception. 1 = Affirmative 0 = Negative
2	AE	PS0,RO	**Alignment Error** It is set to indicate that the received frame ends with a non-byte aligned. 1 = Affirmative 0 = Negative
1	CE	PS0,RO	**CRC Error** It is set to indicate that the received frame ends with a CRC error. 1 = Affirmative 0 = Negative
0	FOE	PS0,RO	**RX Memory Overflow Error** It is set to indicate that a RX memory overflow error happens during the frame reception. 1 = Affirmative 0 = Negative

6.8 Receive Overflow Counter Register (07H)

Bit	Bit Name	Default	Description
7	RXFU	PS0,R/C	**Receive Overflow Counter Overflow** This bit is set when the ROC has an overflow condition. 1 = Affirmative 0 = Negative
6:0	ROC	PS0,R/C	**Receive Overflow Counter** This is a statistic counter to indicate the received packet count upon FIFO overflow.

6.9 Back Pressure Threshold Register (08H)

Bit	Bit Name	Default	Description
7:4	BPHW	PS3, RW	**Back Pressure High Water Overflow Threshold** MAC will generate the jam pattern when RX SRAM free space is lower than this threshold value. The default is 3K-byte free space. Please do not exceed SRAM size (1 unit=1K bytes).
3:0	JPT	PS7, RW	**Jam Pattern Time** Default is 200us

bit3	bit2	bit1	bit0	time
0	0	0	0	10.3us
0	0	0	1	20.5us
0	0	1	0	30.8us
0	0	1	1	51.4us
0	1	0	0	102us
0	1	0	1	195us
0	1	1	0	288us
0	1	1	1	380us
1	0	0	0	483us
1	0	0	1	576us
1	0	1	0	678us
1	0	1	1	771us
1	1	0	0	867us
1	1	0	1	966us
1	1	1	0	1.06ms
1	1	1	1	1.15ms

6.10 Flow Control Threshold Register (09H)

Bit	Bit Name	Default	Description
7:4	HWOT	PS3, RW	**RX Memory High Water Overflow Threshold** Send a pause packet with pause time=FFFFH when the RX memory free space is less than this value. If this value is zero, its means no fRX flow control. The default value is 3K-byte free space. Please do not exceed RX memory size (1 unit=1K bytes).
3:0	LWOT	PS8, RW	**RX Memory Low Water Overflow Threshold** Send a pause packet with pause time=0000H when RX memory free space is larger than this value. This pause packet is enabled after the high water pause packet is transmitted. The default memory free space is 8K-byte. Please do not exceed RX memory size (1 unit=1K bytes).

6.11 RX/TX Flow Control Register (0AH)

Bit	Bit Name	Default	Description
7	TXP0	PS0,RW	**Force TX Pause Packet with 0000H** Set to TX pause packet with pause time field is 0000H. Auto-Clears after pause packet transmission completion.
6	TXPF	PS0,RW	**Force TX Pause Packet with FFFFH** Set to TX pause packet with pause time field is FFFFH. Auto-Clears after pause packet transmission completion.
5	TXPEN	PS0,RW	**TX Pause Packet Enable** Enables the pause packet for high/low water threshold control in Full-Duplex mode. 1 = Enable 0 = Disable
4	BKPA	PS0,RW	**Back Pressure Mode** This mode is for Half-Duplex mode only. It generates a jam pattern when any packet comes and RX SRAM is over BPHW of MAC register 8H. 1 = Enable 0 = Disable
3	BKPM	PS0,RW	**Back Pressure Mode** This mode is for Half-Duplex mode only. It generates a jam pattern when a packet's DA matches and RX SRAM is over BPHW of MAC register 8H. 1 = Enable 0 = Disable
2	RXPS	PS0,R/C	**RX Pause Packet Status, Latch and Read Clearly** When there has been packet received, this bit will be latched. This bit is cleared after read. 1 = Has been receive pause packet 0 = No pause packet received
1	RXPCS	PS0,RO	**RX Pause Packet Current Status** 1 = Received pause packet timer down-count in progress 0 = Pause packet timer value is zero
0	FLCE	PS0,RW	**Flow Control Enable** Set to enable the flow control mode (i.e. can disable DM9051(I) TX function temperately). 1 = Enable 0 = Disable

6.12 EEPROM & PHY Control Register (0BH)

Bit	Bit Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	REEP	P0,RW	**Reload EEPROM** Set one to reload EEPROM. Driver needs to clear it before to enable this function.
4	WEP	P0,RW	**Write EEPROM Enable** Set this bit to one before the operation of write EEPROM. 1 = Enable 0 = Disable
3	EPOS	P0,RW	**EEPROM or PHY Operation Select** 0 = Select EEPROM 1 = Select PHY
2	ERPRR	P0,RW	**EEPROM Read** or **PHY Register Read Command** Set one to read EEPROM or PHY register. Auto-Cleared after the operation completes.
1	ERPRW	P0,RW	**EEPROM Write** or **PHY Register Write Command** Set one to write EEPROM or PHY register. Auto-Cleared after the operation completes.
0	ERRE	P0,RO	**EEPROM Access Status** or **PHY Access Status** 1 = The EEPROM or PHY access is in progress 0 = Completion of the EEPROM or PHY access

6.13 EEPROM & PHY Address Register (0CH)

Bit	Bit Name	Default	Description
7:6	PHY_ADR	P001,RW	PHY Address bit 1 and 0, the PHY address bit [4:2] is force to 0. Force to 01 in application.
5:0	EROA	P00,RW	EEPROM Word Address or PHY Register Number.

6.14 EEPROM & PHY Data Register (EE_PHY_L:0DH EE_PHY_H:0EH)

Bit	Bit Name	Default	Description
7:0	EE_PHY_L	P00,RW	**EEPROM** or **PHY Low Byte Data** The low byte data read from or write to EEPROM or PHY.
7:0	EE_PHY_H	P00,RW	**EEPROM** or **PHY High Byte Data** The high byte data read from or write to EEPROM or PHY.

6.15 Wake Up Control Register (0FH)

Bit	Bit Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	LINKEN	P0,RW	**Link Status Change Wake up Event** To control the link status change event in WOL pin function. 1 = Enable 0 = Disable
4	SAMPLEEN	P0,RW	**Sample Frame Wake up Event** To control the sample frame matched event in WOL pin function. 1 = Enable 0 = Disable
3	MAGICEN	P0,RW	**Magic Packet Wake up Event** To control the Magic packet event in WOL pin function. 1 = Enable 0 = Disable
2	LINKST	P0,RO	**Link Status Change Event Occurred** 1 = Link change event occurred 0 = No link change event
1	SAMPLEST	P0,RO	**Sample Frame Event Occurred** 1 = Sample frame matched event occurred 0 = No sample frame matched
0	MAGICST	P0,RO	**Magic Packet Event Occurred** 1 = Magic packet received 0 = No magic packet received

6.16 Physical Address Register (10H~15H)

Bit	Bit Name	Default	Description
7:0	PAB5	E,RW	Physical Address Byte 5 (15H)
7:0	PAB4	E,RW	Physical Address Byte 4 (14H)
7:0	PAB3	E,RW	Physical Address Byte 3 (13H)
7:0	PAB2	E,RW	Physical Address Byte 2 (12H)
7:0	PAB1	E,RW	Physical Address Byte 1 (11H)
7:0	PAB0	E,RW	Physical Address Byte 0 (10H)

6.17 Multicast Address Hash Table Register (16H~1DH)

Bit	Bit Name	Default	Description
7:0	MAB7	X,RW	Multicast Address Hash Table Byte 7 (1DH)
7:0	MAB6	X,RW	Multicast Address Hash Table Byte 6 (1CH)
7:0	MAB5	X,RW	Multicast Address Hash Table Byte 5 (1BH)
7:0	MAB4	X,RW	Multicast Address Hash Table Byte 4 (1AH)
7:0	MAB3	X,RW	Multicast Address Hash Table Byte 3 (19H)
7:0	MAB2	X,RW	Multicast Address Hash Table Byte 2 (18H)
7:0	MAB1	X,RW	Multicast Address Hash Table Byte 1 (17H)
7:0	MAB0	X,RW	Multicast Address Hash Table Byte 0 (16H)

6.18 General Purpose Control Register (1EH)

Bit	Bit Name	Default	Description
7:4	RESERVED	PH0,RO	Reserved
3	GPC3	P0,RW	**General Purpose Control 3** Define the input/output direction of pin GP3. 1 = Pin GP3 in output mode 0 = Pin GP3 in input mode
2	GPC2	P0,RW	**General Purpose Control 2** Define the input/output direction of pin GP2. 1 = Pin GP2 in output mode 0 = Pin GP2 in input mode
1	GPC1	P0,RW	**General Purpose Control 1** Define the input/output direction of pins GP 1. 1 = Pin GP1 in output mode 0 = Pin GP1 in input mode
0	RESERVED	P1,RO	Reserved

6.19 General Purpose Register (1FH)

Bit	Bit Name	Default	Description
7:4	RESERVED	0,RO	Reserved
3	GPIO3	P0,RW	**General Purpose Pin Data 3** When GPC3 of register 1EH is 1, the value of this bit is reflected to pin GP3. When GPC3 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP3.
2	GPIO2	P0,RW	**General Purpose Pin Data 2** When GPC2 of register 1EH is 1, the value of this bit is reflected to pin GP2. When GPC2 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP2.
1	GPIO1	P0,RW	**General Purpose Pin Data 1** When GPC1 of register 1EH is 1, the value of this bit is reflected to pin GP1. When GPC1 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP1.
0	PHYPD	PE1,WO	**PHY Power Down Control** 1 = Power down PHY 0 = Power up PHY Note: If this bit is updated from '1' to '0', the whole MAC and PHY Registers can not be accessed within 1ms.

6.20 TX Memory Read Pointer Address Register (22H~23H)

Bit	Bit Name	Default	Description
7:0	TRPAH	PS0,RO	TX Memory Read Pointer Address High Byte (23H)
7:0	TRPAL	PS0,RO	TX Memory Read Pointer Address Low Byte (22H)

6.21 RX Memory Write Pointer Address Register (24H~25H)

Bit	Bit Name	Default	Description
7:0	RWPAH	PS,0CH,RO	RX Memory Write Pointer Address High Byte (25H)
7:0	RWPAL	PS,00H,RO	RX Memory Write Pointer Address Low Byte (24H)

6.22 Vendor ID Register (28H~29H)

Bit	Bit Name	Default	Description
7:0	VIDH	PE,0AH,RO	Vendor ID High Byte (29H)
7:0	VIDL	PE,46H,RO	Vendor ID Low Byte (28H)

6.23 Product ID Register (2AH~2BH)

Bit	Bit Name	Default	Description
7:0	PIDH	PE,90H,RO	Product ID High Byte (2BH)
7:0	PIDL	PE,51H,RO	Product ID Low Byte (2AH)

6.24 CHIP Revision (2CH)

Bit	Bit Name	Default	Description
7:0	CHIPR	P,01H,RO	CHIP Revision

6.25 Transmit Control Register 2 (2DH)

Bit	Bit Name	Default	Description
7	LED	PE0,RW	**LED Mode** See the LED pin description for detailed. 1 = LED mode 1 0 = LED mode 0
6	RLCP	P0,RW	**Retry Late Collision Packet** Re-transmit the packet with late-collision. 1 = Enable 0 = Disable
5	RESERVED	P0,RW	Reserved
4	ONEPM	P0,RW	**One Packet Mode** 1 = Only one packet transmit command can be issued before transmit completed 0 = At most two packet transmit command can be issued before transmit completed
3:0	IFGS	P00,RW	**Inter-Frame Gap Setting** 0XXX = 96-bit 1000 = 64-bit 1001 = 72-bit 1010 = 80-bit 1011 = 88-bit 1100 = 96-bit 1101 = 104-bit 1110 = 112-bit 1111 = 120-bit

6.26 Auto-Transmit Control Register (30H)

Bit	Bit Name	Default	Description
7	AUTO_TX	PS0,RW	**Auto-Transmit Control** 1 = Auto-Transmit enabled. Packet transmitted automatically when end of write TX buffer 0 = Auto-Transmit disabled. When transmit packet, need to set MAC register 2H bit 0 to "1"
6:2	RESERVED	P00,RO	Reserved
1:0	RESERVED	PS0,RW	Reserved

6.27 Transmit Check Sum Control Register (31H)

Bit	Bit Name	Default	Description
7:3	RESERVED	0,RO	Reserved
2	UDPCSE	PS0,RW	**UDP CheckSum Generation** 1 = Enable 0 = Disable
1	TCPCSE	PS0,RW	**TCP CheckSum Generation** 1 = Enable 0 = Disable
0	IPCSE	PS0,RW	**IPv4 CheckSum Generation** 1 = Enable 0 = Disable

6.28 Receive Check Sum Status Register (32H)

Bit	Bit Name	Default	Description
7	UDPS	PS0,RO	**UDP CheckSum Status** 1 = Checksum fail, if UDP packet 0 = No UDP checksum error
6	TCPS	PS0,RO	**TCP CheckSum Status** 1 = Checksum fail, if TCP packet 0 = No TCP checksum error
5	IPS	PS0,RO	**IPv4 CheckSum Status** 1 = Checksum fail, if IP packet 0 = No IP checksum error
4	UDPP	PS0,RO	**UDP Packet of Current Received Packet** 1 = UDP packet 0 = Non UDP packet
3	TCPP	PS0,RO	**TCP Packet of Current Received Packet** 1 = TCP Packet 0 = Non TCP Packet
2	IPP	PS0,RO	**IPv4 Packet of Current Received Packet** 1 = IP Packet 0 = Non IP Packet
1	RCSEN	PS0,RW	**Receive CheckSum Checking Enable** When set, the checksum status (bit 7~2) will be stored in bit 7:2 of packet's first byte of RX packets status header respectively. 1 = Enable 0 = Disable
0	DCSE	PS0,RW	**Discard CheckSum Error Packet** When set, if IPv4/TCP/UDP checksum field is error, this packet will be discarded. 1 = Enable 0 = Disable

6.29 SPI Bus Control Register (38H)

Bit	Bit Name	Default	Description
7	RESERVED	P0,RW	Reserved
6:5	CURR	PE10,RW	**SPI_MISO Current Driving/Sinking Capability** 00 = 2mA 01 = 4mA 10 = 6mA (default) 11 = 8mA
4:3	RESERVED	P00,RW	Reserved
2	CSB_SPIKE	PE1,RW	**Eliminate SPI_CSB Spike** 1 = Eliminate about 2ns SPI_CSB spike
1:0	RESERVED	P00,RW	Reserved

6.30 INT Pin Control Register (39H)

Bit	Bit Name	Default	Description
7:2	RESERVED	PS0,RO	Reserved
1	INT_TYPE	PET0,RW	**INT Pin Output Type Control** 1 = INT Open-Collector output 0 = INT push-pull output
0	INT_POL	PET0,RW	**INT Pin Polarity Control** 1 = INT active low 0 = INT active high

6.31 Pause Packet Control/Status Register (3DH)

Bit	Bit Name	Default	Description
7:4	PAUSE_CTR	P00,RO	**Pause Packet Counter** The Pause packet counter before RX SRAM flow control low threshold reached.
3:0	PAUSE_MAX	PS1,RW	**Max. Pause Packet Count** The maximum count of to generate pause packet with timer field FFFFH, when the RX memory is reached to high threshold. If the value of these bits are zero, the pause packet with timer field FFFFH is generated whenever the RX memory is reached to the high threshold.

6.32 IEEE 802.3az Enter Counter Register (3EH)

Bit	Bit Name	Default	Description
7	RESERVED	P0,RO	Reserved
6:0	ENTER	P5,RW	**Timer to Enter EEE State (unit 2us)** The DM9051(I) will enter EEE state after TX idle timer timeout.

6.33 IEEE 802.3az Leave Counter Register (3FH)

Bit	Bit Name	Default	Description
7	EEE_EN	PE0,RW	EEE Enable
6:0	LEAVE	P0Fh,RW	**Timer to Leave EEE State (unit 2us)** The DM9051(I) will leave EEE state after TX leave timer timeout when transmit command issued by set MAC register 2H bit 0 or Auto-Transmit.

6.34 SPI Byte Align Error Counter Register (4AH)

Bit	Bit Name	Default	Description
7:0	ALN_ERR	P00,RO	**SPI Clock Byte Align Error Counter** The counter to count the byte align error of SPI_CK at end of SPI_CSN. The maximum value is 255. Cleared by write this register with any value.

6.35 RX Packet Length Control Register (52H)

Bit	Bit Name	Default	Description
7	RXLEN	PS0,RW	**RX Packet Length Filter** 1 = Enable check RX packet length 0 = Not to check RX packet length
6:5	RESERVED	P00,RO	Reserved
4:0	MAXRXLEN	PS0,RW	**Maximum RX Packet Length Allowed (unit 64-byte)** The RX packet will be discarded if the data length is more than this count. Note: all bits 0 means no length limitation

6.36 RX Broadcast Control Register (53H)

Bit	Bit Name	Default	Description
7:6	BC_EN	PS0,RW	**New RX Broadcast Packet Control Mode** 0X = Broadcast packet control by bit 7 of MAC register 1DH 10 = Not to accept broadcast packet 11 = Enable packet length filter of broadcast packet
5	RESERVED	P0,RO	Reserved
4:0	MAXBCLEN	PS0,RW	**Maximum RX Broadcast Packet Length Allowed** (unit 64-byte) The RX packet will be discarded if the data length is more than this count. Note: all bits 0 means no length limitation

6.37 INT Pin Clock Output Control Register (54H)

Bit	Bit Name	Default	Description
7	INT_CTL	PS0,RW	**INT Pin in Clock Output Control** 1 = Enable INT pin in clock output 0 = INT pin output controlled by MAC register 39H
6	CK_UNIT	PS0,RW	**Clock Output Duty Cycle Width Unit** 1 = 1.3ms 0 = 40.96us
5	RESERVED	P0,RO	Reserved
4:0	DUTY_LEN	PS0,RW	**Clock Output Duty Cycle Width** Note: all bits 0 means INT pin is controlled by register 39H

6.38 Memory Pointer Control Register (55H)

Bit	Bit Name	Default	Description
7:2	RESERVED	P00,RO	Reserved
1	RST_TX	PS0,RW	**Reset TX Memory Pointer** 1 = Reset TX write/read memory address, Auto-Cleared after 1us
0	RST_RX	PS0,RW	**Reset RX Memory Pointer** 1 = Reset RX write/read memory address, Auto-Cleared after 1us

6.39 More LED Control Register (57H)

Bit	Bit Name	Default	Description
7	LED_MOD3	P0,RW	**New LED Mode** 1 = LED types in bit 2:0 0 = The old LED mode 0 or 1 function
6:3	RESERVED	P00,RO	Reserved
2	LED_POL	P0,RW	**The Reverse Polarity of LED Type** 1 = LED in high active 0 = LED in low active
1:0	LED_TYPE	P00,RW	**LED Type** Note: see following table

LED_Type	LNKLED (pin 25)	SPDLED (pin 26)	FDXLED (pin 16)
00	Link	Traffic	Full-Duplex
01	Link & Traffic	Speed100M	Full-Duplex
10	Traffic	Speed100M	Speed10M
11	Link	Traffic100M	Traffic10M

6.40 Memory Control Register (59H)

Bit	Bit Name	Default	Description
7:1	RESERVED	P00,RO	Reserved
0	MSIZE_EN	P0,RW	**TX/RX Memory Size Configurable** 1 = Enable to configure TX/RX memory size by MAC register 5AH 0 = 3K-byte for TX and 13K-byte for RX

6.41 Transmit Memory Size Register (5AH)

Bit	Bit Name	Default	Description
7:5	RESERVED	P00,RO	Reserved
4:0	TRAM_SIZE	P3,RW	**TX Memory Size (unit K-byte)** The RX memory size is 16 – TRAM_SIZE.

6.42 Memory BIST Status Register (5DH)

Bit	Bit Name	Default	Description
7	BIST_END	P0,RO	**Memory BIST Completion** 1 = Completed 0 = In progress
6	BIST_DIS	P0,RO	**Memory BIST Control** This bit is the inverse of strap pin EECS. 1 = BIST disabled 0 = BIST enabled
5	RESERVED	P0,RO	Reserved
4	PAT_00	P0,RO	**BIST 00H Pattern Status** 1 = OK 0 = Fail
3	PAT_DEC	P0,RO	**BIST Decrement Pattern Status** 1 = OK 0 = Fail
2	PAT_INC	P0,RO	**BIST Increment Pattern Status** 1 = OK 0 = Fail
1	PAT_AA	P0,RO	**BIST AAH Pattern Status** 1 = OK 0 = Fail
0	PAT_55	P0,RO	**BIST 55H Pattern Status** 1 = OK 0 = Fail

6.43 Memory Data Pre-Fetch Read Command without Address Increment Register (70H)

Bit	Bit Name	Default	Description
7:0	MRCMDX	X,RO	**Memory Read Command** Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. And the DM9051(I) starts to pre-fetch the SRAM data to internal data buffers.

6.44 Memory Read Command without Data Pre-Fetch and Address Increment Register (71H)

Bit	Bit Name	Default	Description
7:0	MRCMDX1	X,RO	**Memory Read Command** Read data from RX Memory. After the read of this command, the read pointer of RX memory is unchanged. And the DM9051(I) do not pre-fetch the memory data.

6.45 Memory Data Read Command with Address Increment Register (72H)

Bit	Bit Name	Default	Description
7:0	MRCMD	X,RO	**Memory Read Command** Read data from RX SRAM. After the read of this command, the read pointer is increased by 1.

6.46 SPI Data Read Delay Counter Register (73H)

Bit	Bit Name	Default	Description
7:0	RD_DLY	0,WO	**Read Data Delay Counter** The byte delay counter that first data is valid after command byte.

6.47 Memory Data Read Address Register (74H~75H)

Bit	Bit Name	Default	Description
7:0	MDRAH	PS0,RW	**Memory Data Read Addresses High Byte** It will be set to 0CH, when IMR bit7 =1 (75H)
7:0	MDRAL	PS0,RW	**Memory Data Read Address Low Byte** (74H)

6.48 Memory Data Write Command without Address Increment Register (76H)

Bit	Bit Name	Default	Description
7:0	MWCMDX	X,WO	**Write Data to TX Memory** After the write of this command, the write pointer is unchanged

6.49 Memory Data Write Command with Address Increment Register (78H)

Bit	Bit Name	Default	Description
7:0	MWCMD	X,WO	**Write Data to TX SRAM** After the write of this command, the write pointer is increased by 1.

6.50 Memory Data Write Address Register (7AH~7BH)

Bit	Bit Name	Default	Description
7:0	MDWAH	PS0,RW	Memory Data Write Address High Byte (7BH)
7:0	MDWAL	PS0,RW	Memory Data Write Address Low Byte (7AH)

6.51 TX Packet Length Register (7CH~7DH)

Bit	Bit Name	Default	Description
7:0	TXPLH	X,R/W	TX Packet Length High Byte (7DH)
7:0	TXPLL	X,R/W	TX Packet Length Low Byte (7CH)

6.52 Interrupt Status Register (7EH)

Bit	Bit Name	Default	Description
7	RESERVED	P1,RO	Reserved
6	RESERVED	RO	Reserved
5	LNKCHG	PS0,RW/C1	**Link Status Change** 1 = Affirmative 0 = Negative
4	RESERVED	RO	Reserved
3	ROO	PS0,RW/C1	**Receive Overflow Counter Overflow** 1 = Affirmative 0 = Negative
2	ROS	PS0,RW/C1	**Receive Overflow** 1 = Affirmative 0 = Negative
1	PT	PS0,RW/C1	**Packet Transmitted** 1 = Affirmative 0 = Negative
0	PR	PS0,RW/C1	**Packet Received** 1 = Affirmative 0 = Negative

6.53 Interrupt Mask Register (7FH)

Bit	Bit Name	Default	Description
7	PAR	PS0,RW	**Pointer Auto-Return Mode** Enable the TX/RX memory read/write pointer to automatically return to the start address when pointers are over the TX/RX memory size. When this bit is set, the MAC register 75H will be set to 0CH automatically if RX memory size is 13K-byte. 1 = Enable 0 = Disable
6	RESERVED	RO	Reserved
5	LNKCHGI	PS0,RW	**Enable Link Status Change Interrupt** 1 = Enable 0 = Disable
4	RESERVED	RO	Reserved
3	ROOI	PS0,RW	**Enable Receive Overflow Counter Overflow Interrupt** 1 = Enable 0 = Disable
2	ROI	PS0,RW	**Enable Receive Overflow Interrupt** 1 = Enable 0 = Disable
1	PTI	PS0,RW	**Enable Packet Transmitted Interrupt** 1 = Enable 0 = Disable
0	PRI	PS0,RW	**Enable Packet Received Interrupt** 1 = Enable 0 = Disable

7 EEPROM and SPI Command Format

7.1 EEPROM Format

Name	Word	Offset	Description
MAC Address	0	0~5	6 Byte Ethernet Address
Auto Load Control	3	6~7	Bit 1:0 = 01: Update vendor ID and product ID from WORD4 and 5. Bit 3:2 = 01: Accept setting of WORD6 [15,4:3] Bit 5:4 = 01: Reserved, set to 00 in application Bit 7:6 = 01: Accept setting of WORD7 [3:0] Bit 9:8 = 01: Accept setting of WORD8[3:0] Bit 11:10 = 01: Accept setting of WORD7 [7] Bit 13:12 = 01: Accept setting of WORD7 [9:8] Bit 15:14 = 01: Accept setting of WORD7 [15:12]
Vendor ID	4	8~9	2 byte vendor ID (Default: 0A46H)
Product ID	5	10~11	2 byte product ID (Default: 9051H)
Pin Control / Control 1	6	12~13	When word 3 bit [3:2]=01, these bits can control the INT pins polarity. Bit 2:0: Reserved; set to 0 in application Bit 3: INT pin is active low when set (default: active high) Bit 4: INT pin is open-collected (default: push-pull output) Bit 14:5: Reserved; set to 0 in application Bit 15: Enable 802.3az, to MAC register 3FH bit [7]
Wake-up Mode Control / Control 2	7	14~15	Bit 0: The WOL pin is active low when set (default: active high) Bit 1: The WOL pin is in pulse mode when set (default: push-pull mode) Bit 2: Magic wakeup event is enabled when set. (default: disable) Bit 3: Link change wakeup event is enabled when set (default disable) Bit 6:4: Reserved; set to 0 in application Bit 7:0 = LED mode 0, 1=LED mode 1 (default: mode 0) Bit 8:1 = Internal PHY is enabled after power-on (default: disable) Bit 9: Fiber Mode Control; 1= Fiber mode, 0 = TP mode Bit 13:10: Reserved; set to 0 in application Bit 14: Reserved; set to 1 in application Bit 15: Reserved; set to 0 in application
Control 3	8	16~17	Bit 0: Reserved; set to 1 in application. Bit 1: Eliminate SPI_CSB high spike control This bit will be load into MAC register 38H bit 2 Bit 3:2: SPI_MISO driving capability This bit will be load into MAC register 38H bit [6:5]

7.2 SPI Command Format

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1
	Opcode	Register Address	Register Data
Register Write	1	A6~A0	D7~D0

SPI	Command Phase (MOSI pin)		Data Phase (MISO pin)
	Byte 0 [7:0]		Byte 1
	Opcode	Register Address	Register Data
Register Read	0	A6~A0	D7~D0
Memory Dummy Read	0	1110000	D7~D0

SPI	Command Phase (MOSI pin)		Data Phase (MISO pin)
	Byte 0 [7:0]		Byte 1~N
	Opcode	Register Address	Memory Data
Memory Dummy Read Without Pre-fetch	0	1110001	(D7~D0)*N

Note 1: N can be 1~4

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1~N
	Opcode	Register Address	Memory Data
Memory Write	1	1111000	(D7~D0)*N

SPI	Command Phase (MOSI pin)		Data Phase (MISO pin)
	Byte 0 [7:0]		Byte 1~N
	Opcode	Register Address	Memory Data
Memory Read	0	1110010	(D7~D0)*N

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0		Byte 1~N
	Opcode	Register Address	Transmit Length and Packet Data
Auto-Transmit	1	1111100	(D7~D0)*N (see Note1)

Note 2:
Byte 1: Transmit Length bit 7~0 of n-byte
Byte 2: FDH
Byte 3: Transmit Length bit 15~8 of n-byte
Byte 4: F8H
Byte 5~n+4: 5~n+4: n-byte transmit data

Note 3: This command burst is used only when register 30H bit 7 is set

8 PHY Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	CONTROL	Reset	Loop Back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01H	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02H	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03H	PHYID2	1	0	1	1	1	0	Model No.					Version No.				
								001010					0000				
04H	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05H	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06H	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
10H	Specified Config	BP 4B5B	BP SCR	BP ALIGN	BP_ ADPOK	Reserved	TX	Reserved	Reserved	Force 100LNK	Reserved	Reserved	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Reserved
11H	Specified Conf/Sta	100 FDX	100 HDX	10 FDX	10 HDX	Reserved	Reserved	Reserved	PHY ADDR [4:0]				Auto-N. Monitor Bit [3:0]				
12H	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Reserved	Reserved									Polarity Reverse
13H	PWDOR	Reserved							PD10DRV	PD100I	PDchip	PDcrm	PDaeq	PDdrv	PDecli	PDeclo	PD10
14H	Specified Config	TSTSE1	TSTSE2	FORCE_ TXSD	FORCE_ FEF	PREAM BLEX	TX10M_ PWR	NWAY_ PWR	Reserved	MDIX_ CNTL	AutoNeg_ dlpbk	Mdix_fix Value	Mdix_ down	MonSel1	MonSel0	Reserved	PD_ value
1BH	DSP_CTRL	Reserved															
1DH	PSCR	Reserved				preamblex	AMPLITUDE	TX_PWR	Reserved								

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>:
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- (PIN#) Value latched in from pin # at reset

<Access Type>:
- RO = Read Only
- RW = Read/Write

<Attribute(s)>:
SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

8.1 Basic Mode Control Register (BMCR) – 00H

Bit	Bit Name	Default	Description
15	Reset	0, RW/SC	**Reset** 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed.
14	Loopback	0, RW	**Loopback** Loopback control register 1 = Loopback enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 1300ms "dead time" before any valid data appear at the MII receive outputs.
13	Speed Selection	1, RW	**Speed select** 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by Auto-Negotiation. When Auto-Negotiation is enabled and bit 12 is set, this bit will return Auto-Negotiation selected media type.
12	Auto-Negotiation Enable	1, RW	**Auto-Negotiation enable** 1 = Auto-Negotiation is enabled, bit 8 and 13 will be in Auto-Negotiation status
11	Power Down	0, RW	**Power Down** While in the power down state, the PHY should respond to management transactions. During the transition to power down state and while in the power down state, the PHY should not generate spurious signals on the MII. 1 = Power down 0 = Normal operation
10	Isolate	0,RW	**Isolate** 1 = Isolates the PHY from the MII with the exception of the serial management. (When this bit is asserted, the PHY does not respond to the TXD[0:3], TX_EN, and TX_ER inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RX[0:3], COL and CRS outputs. When PHY is isolated from the MII it shall respond to the management transactions) 0 = Normal operation
9	Restart Auto-Negotiation	0,RW/SC	**Restart Auto-Negotiation** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. When Auto-Negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until Auto-Negotiation is initiated by the PHY. The operation of the Auto-Negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation

8	Duplex Mode	1,RW	**Duplex Mode** 1 = Full-Duplex operation. Duplex selection is allowed when Auto-Negotiation is disabled (bit 12 of this register is cleared). With Auto-Negotiation enabled, this bit reflects the duplex capability selected by Auto-Negotiation 0 = Normal operation
7	Collision Test	0,RW	**Collision Test** 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN 0 = Normal operation
6:0	RESERVED	0,RO	**Reserved** Write as 0, ignore on read

8.2 Basic Mode Status Register (BMSR) – 01H

Bit	Bit Name	Default	Description
15	100BASE-T4	0,RO/P	**100BASE-T4 Capable** 1 = Able to perform in 100BASE-T4 mode 0 = Not able to perform in 100BASE-T4 mode
14	100BASE-TX Full-Duplex	1,RO/P	**100BASE-TX Full-Duplex Capable** 1 = Able to perform 100BASE-TX in Full-Duplex mode 0 = Not able to perform 100BASE-TX in Full-Duplex mode
13	100BASE-TX Half-Duplex	1,RO/P	**100BASE-TX Half-Duplex Capable** 1 = Able to perform 100BASE-TX in Half-Duplex mode 0 = Not able to perform 100BASE-TX in Half-Duplex mode
12	10BASE-T Full-Duplex	1,RO/P	**10BASE-T Full-Duplex Capable** 1 = Able to perform 10BASE-T in Full-Duplex mode 0 = Not able to perform 10BASE-TX in Full-Duplex mode
11	10BASE-T Half-Duplex	1,RO/P	**10BASE-T Half-Duplex Capable** 1 = Able to perform 10BASE-T in Half-Duplex mode 0 = Not able to perform 10BASE-T in Half-Duplex mode
10:7	RESERVED	0,RO	**Reserved** Write as 0, ignore on read
6	MF Preamble Suppression	0,RO	**MII Frame Preamble Suppression** 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-Negotiation Complete	0,RO	**Auto-Negotiation Complete** 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed
4	Remote Fault	0,RO/LH	**Remote Fault** 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is PHY implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05H) is set 0 = No remote fault condition detected

3	Auto-Negotiation Ability	1,RO/P	**Auto Configuration Ability** 1 = Able to perform Auto-Negotiation 0 = Not able to perform Auto-Negotiation
2	Link Status	0,RO/LL	**Link Status** 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface.
1	Jabber Detect	0,RO/LH	**Jabber Detect** 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a PHY reset. This bit works only in 10Mbps mode.
0	Extended Capability	1,RO/P	**Extended Capability:** 1 = Extended register capable 0 = Basic register capable only

8.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9051(I). The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15.0	OUI_MSB	0181h	**OUI Most Significant Bits** This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2).

8.4 PHY ID Identifier Register #2 (PHYID2) – 03H

Bit	Bit Name	Default	Description
15:10	OUI_LSB	101110, RO/P	**OUI Least Significant Bits:** Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively.
9:4	VNDR_MDL	001010, RO/P	**Vendor Model Number** Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	0000, RO/P	**Model Revision Number** Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3).

8.5 Auto-Negotiation Advertisement Register (ANAR) – 04H

This register contains the advertised abilities of this DM905(I) device as they will be transmitted to its link partner during Auto-Negotiation.

Bit	Bit Name	Default	Description
15	NP	0,RO/P	**Next Page Indication** 1 = Next page available 0 = No next page available The PHY has no next page, so this bit is permanently set to 0.
14	ACK	0,RO	**Acknowledge** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The PHY's Auto-Negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-Negotiation process. Software should not attempt to write to this bit.
13	RF	0,RW	**Remote Fault** 1 = Local device senses a fault condition 0 = No fault detected
12:11	RESERVED	X,RW	**Reserved** Write as 0, ignore on read
10	FCS	0,RW	**Flow Control Support** 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	0,RO/P	**100BASE-T4 Support** 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The PHY does not support 100BASE-T4 so this bit is permanently set to 0
8	TX_FDX	1,RW	**100BASE-TX Full-Duplex Support** 1 = 100BASE-TX Full-Duplex is supported by the local device 0 = 100BASE-TX Full-Duplex is not supported
7	TX_HDX	1,RW	**100BASE-TX Support** 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX is not supported
6	10_FDX	1,RW	**10BASE-T Full-Duplex support** 1 = 10BASE-T Full-Duplex is supported by the local device 0 = 10BASE-T Full-Duplex is not supported
5	10_HDX	1,RW	**10BASE-T Support** 1 = 10BASE-T is supported by the local device 0 = 10BASE-T is not supported
4:0	Selector	00001,RW	**Protocol Selection Bits** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

8.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) – 05H

This register contains the advertised abilities of the link partner when received during Auto-Negotiation.

Bit	Bit Name	Default	Description
15	NP	0,RO	**Next Page Indication** 1 = Link partner, next page available 0 = Link partner, no next page available
14	ACK	0,RO	**Acknowledge** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The PHY's Auto-Negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
13	RF	0,RO	**Remote Fault** 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12:11	RESERVED	X,RO	**Reserved** Write as 0, ignore on read
10	FCS	0,RW	**Flow Control Support** 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	0,RO	**100BASE-T4 Support** 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	0,RO	**100BASE-TX Full-Duplex Support** 1 = 100BASE-TX Full-Duplex is supported by the link partner 0 = 100BASE-TX Full-Duplex is not supported by the link partner
7	TX_HDX	0,RO	**100BASE-TX Support** 1 = 100BASE-TX Half-Duplex is supported by the link partner 0 = 100BASE-TX Half-Duplex is not supported by the link partner
6	10_FDX	0,RO	**10BASE-T Full-Duplex Support** 1 = 10BASE-T Full-Duplex is supported by the link partner 0 = 10BASE-T Full-Duplex is not supported by the link partner
5	10_HDX	0,RO	**10BASE-T Support** 1 = 10BASE-T Half-Duplex is supported by the link partner 0 = 10BASE-T Half-Duplex is not supported by the link partner
4:0	Selector	00000,RO	**Protocol Selection Bits** Link partner's binary encoded protocol selector.

8.7 Auto-Negotiation Expansion Register (ANER) – 06H

Bit	Bit Name	Default	Description
15:5	RESERVED	X,RO	**Reserved** Write as 0, ignore on read
4	PDF	0,RO/LH	**Local Device Parallel Detection Fault** 1 = A fault detected via parallel detection function 0 = No fault detected via parallel detection function
3	LP_NP_ABLE	0,RO	**Link Partner Next Page Able** 1 = Link partner, next page available 0 = Link partner, no next page
2	NP_ABLE	0,RO/P	**Local Device Next Page Able** 1 = Next page available 0 = No next page
1	PAGE_RX	0,RO/LH	**New Page Received** A new link code word page received. This bit will be automatically cleared when the register (register 6H) is read by management.
0	LP_AN_ABLE	0,RO	**Link Partner Auto-Negotiation Able** A "1" in this bit indicates that the link partner supports Auto-Negotiation.

8.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Bit Name	Default	Description
15	BP_4B5B	0,RW	**Bypass 4B5B Encoding and 5B4B Decoding** 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
14	BP_SCR	0,RW	**Bypass Scrambler/Descrambler Function** 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
13	BP_ALIGN	0,RW	**Bypass Symbol Alignment Function** 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
12	BP_ADPOK	0,RW	**BYPASS ADPOK** Force signal detector (SD) active. This register is for debug only, not release to customer. 1 = Force SD is OK 0 = Normal operation
11	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
10	TX	1,RW	**100BASE-TX or FX Mode Control** 1 = 100BASE-TX operation 0 = 100BASE-FX operation
9	RESERVED	0,RO	**Reserved**
8	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
7	F_LINK_100	0,RW	**Force Good Link in 100Mbps** 1 = Force 100Mbps good link status 0 = Normal 100Mbps operation This bit is useful for diagnostic purposes.
6	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
5	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.

4	RPDCTR-EN	1,RW	**Reduced Power Down Control Enable** This bit is used to enable automatic reduced power down. 1 = Enable automatic reduced power down 0 = Disable automatic reduced power down
3	SMRST	0,RW	**Reset state machine** When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
2	MFPSC	1,RW	**MF Preamble Suppression Control** MII frame preamble suppression control bit. 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
1	SLEEP	0,RW	**Sleep Mode** Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset.
0	RESERVED	0,RW	**Reserved** Force to 0 in application.

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

Bit	Bit Name	Default	Description
15	100FDX	1,RO	**100M Full-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Full-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
14	100HDX	1,RO	**100M Half-Duplex Operation Mode** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Half-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
13	10FDX	1,RO	**10M Full-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
12	10HDX	1,RO	**10M Half-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Half-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
11:9	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
8:4	PHYADR[4:0]	00001,RW	**PHY Address Bit 4:0** The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY.

3:0	ANMB[3:0]	0,RO	**Auto-Negotiation Monitor Bits** These bits are for debug only. The Auto-Negotiation status will be written to these bits.

b3	b2	b1	b0	
0	0	0	0	In IDLE state
0	0	0	1	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detects signal_link_ready
0	1	1	1	Parallel detects signal_link_ready fail
1	0	0	0	Auto-Negotiation completed successfully

8.10 10BASE-T Configuration/Status (10BTCSR) – 12H

Bit	Bit Name	Default	Description
15	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
14	LP_EN	1,RW	**Link Pulse Enable** 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
13	HBE	1,RW	**Heartbeat Enable** 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the PHY is configured for Full-Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full-Duplex mode).
12	SQUELCH	1,RW	**Squelch Enable** 1 = Normal squelch 0 = Low squelch
11	JABEN	1,RW	**Jabber Enable** Enables or disables the Jabber function when the PHY is in 10BASE-T Full-Duplex or 10BASE-T transceiver loopback mode. 1 = Jabber function enabled 0 = Jabber function disabled
10:1	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
0	POLR	0,RO	**Polarity Reversed** When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is set and cleared by 10BASE-T module automatically.

8.11 Power Down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
15:9	RESERVED	0,RO	Reserved Read as 0, ignore on write
8	PD10DRV	0,RW	Vendor power down control test
7	PD100DL	0,RW	Vendor power down control test
6	PDCHIP	0,RW	Vendor power down control test
5	PDCOM	0,RW	Vendor power down control test
4	PDAEQ	0,RW	Vendor power down control test
3	PDDRV	0,RW	Vendor power down control test
2	PDEDI	0,RW	Vendor power down control test
1	PDEDO	0,RW	Vendor power down control test
0	PD10	0,RW	Vendor power down control test

Note: When selected, the power down value is control by register 14H bit0.

8.12 Specified Config Register – 14H

Bit	Bit Name	Default	Description
15	TSTSE1	0,RW	Vendor test select control
14	TSTSE2	0,RW	Vendor test select control
13	FORCE_TXSD	0,RW	**Force Signal Detect** 1 = Force SD signal OK in 100M 0 = Normal SD signal
12	FORCE_FEF	0,RW	Vendor test select control
11	PREAMBLEX	1,RW	**Preamble Saving Control** 1 = Transmit preamble bit count is normal in 10BASE-T mode 0 = When bit 10 is set, the 10BASE-T transmit preamble count is reduced. When bit 11 of register 1DH is set, 12-bit preamble is reduced; otherwise 22-bit preamble is reduced
10	TX10M_PWR	1,RW	**10BASE-T Mode Transmit Power Saving Control** 1 = Enable transmit power saving in 10BASE-T mode 0 = Disable transmit power saving in 10BASE-T mode
9	NWAY_PWR	0,RW	**Auto-Negotiation Power Saving Control** 1 = Disable power saving during Auto-Negotiation period 0 = Enable power saving during Auto-Negotiation period
8	RESERVED	0,RW	Reserved
7	MDIX_CNTL	MDI/MDIX,RO	**The Polarity of MDI/MDIX Value** 1 = MDIX mode 0 = MDI mode
6	AutoNeg_LPBK	0,RW	**Auto-Negotiation Loopback** 1 = Test internal digital Auto-Negotiation Loopback 0 = Normal
5	MDIX_FIX Value	0,RW	**MDIX_CNTL Force Value** When Mdix_down = 1, MDIX_CNTL value depend on the register value.

4	MDIX_Down	0,RW	**HP Auto-MDIX Down** Manual force MDI/MDIX. 1 = Disable HP Auto-MDIX , MDIX_CNTL value depend on Bit5 0 = Enable HP Auto-MDIX
3	MonSel1	0,RW	Vendor monitor select
2	MonSel0	0,RW	Vendor monitor select
1	RESERVED	0,RW	**Reserved** Force to 0, in application.
0	PD_Value	0,RW	**Power Down Control Value** Decision the value of each field register 19H. 1 = Power down 0 = Normal

8.13 Power Saving Control Register (PSCR) – 1DH

Bit	Bit Name	Default	Description
15:13	RESERVED	0,RO	Reserved
12	LPI	0,RO	**Low Power Idle Status** 1 = In Low power idle mode 0 = In normal mode
11	PREAMBLEX	0,RW	**Preamble Saving Control** When both bit 10and 11 of PHY register 14H are set, the 10BASE-T transmit preamble count is reduced. 1 = 12-bit preamble is reduced 0 = 22-bit preamble is reduced
10	AMPLITUDE	0,RW	**Transmit Amplitude Control Disabled** 1 = When cable is unconnected with link partner, the TX amplitude is reduced for power saving 0 = Disable Transmit amplitude reduce function
9	TX_PWR	0,RW	**Transmit Power Saving Control Disabled** 1 = When cable is unconnected with link partner, the driving current of transmit is reduced for power saving 0 = Disable transmit driving power saving function
8:0	RESERVED	0,RO	Reserved

9 Functional Description

9.1 SPI Processor Interface

The DM9051(I) supports a slave mode SPI interface. In this mode, an external SPI master device (from micro-controller or CPU) supplies the operating serial clock (SPI_CK), chip select (SPI_CSN), and serial input data (SPI_MOSI). A Serial output data (SPI_MISO) is driven from DM9051(I). SPI_MOSI is the output on SPI_CK falling edge of SPI master device, sampled by DM9051(I) on SPI_CK rising edge. SPI_MISO is driven from DM9051(I) on SPI_CK falling edge and sampled on SPI_CK rising edge by SPI master device. The falling edge of SPI_CSN starts the SPI burst operation and the rising edge of SPI_CSN stops the SPI burst operation. The SPI_CK stays in low state at SPI mode 0 or stays in high state at SPI mode 3 when SPI burst operation is idle (the SPI_CSN in high state).

9.2 Direct Memory Access Control

The DM9051(I) provides DMA capability to simplify the access of the internal memory. After the programming of the starting address of the internal memory and then issuing a dummy read/write command to load the current data to internal data buffer, the desired location of the internal memory can be accessed by the read/write command registers. The memory's address will be increased with one byte and the data of the next location will be loaded into internal data buffer automatically. It is noted that the data of the first access (the dummy read/write command) in a sequential burst should be ignored because that the data was the contents of the last read/write command.

The internal memory size is 16K bytes. The first location of 3K bytes is used for the data buffer of the packet transmission. The other 13K bytes are used for the buffer of the receiving packets. So in the write memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0 if the end of address (i.e. 3K) is reached. In a similar way, in the read memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0C00H if the end of address (i.e. 16K) is reached.

9.3 Packet Transmission

There are two packets, sequentially named as index I and index II, can be stored in the TX SRAM at the same time. The index MAC register 02H controls the insertion of CRC and pads. Their statuses are recorded at index MAC registers 03H and 04H respectively.

The start address of transmission is 00h and the current packet is index I after software or power-on reset. Firstly write data to the TX memory using the DMA port MAC register 78H and then write the byte count to TX packet length register at MAC register 7CH and 7DH. Set the bit 1 of transmit control register MAC 02H or by Auto-Transmit command burst, the DM9051(I) starts to transmit the index I packet. Before the transmission of the index I packet ends, the data of the next (index II) packet can be write into TX memory and transmit it. After the index I/II packet ends the transmission, the status MAC register 01H bit 3 and 4 will be set to indicate the next index I or II packet can be transmitted.

9.4 Packet Reception

The RX memory is a ring data structure. The start address of RX memory is default 0C00H after software or power-on reset or by set MAC register 55H bit 0. Each packet content format is a 4-byte status header followed with the data of the reception packet which CRC field is included. The format of the 4-byte status header is flag byte, RX status, low byte of RX size, and high byte of RX size respectively. The flag byte is 01h or is RX checksum status if register 32H bit 1 is set.

9.5 100Base –TX Operation

The transmitter section contains the following functional blocks:
- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Encoder
- NRZI to MLT-3
- MLT-3 Driver

9.5.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC reconciliation layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC reconciliation layer, the 4B5B encoder injects the T/R code group pair (01101 00111) indicating end-of-frame. After the T/R code group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9051(I) includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters, which do not require 4B5B conversion.

9.5.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.5.3 Parallel to Serial Converter

The parallel to serial converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block.

9.5.4 NRZ to NRZI Encoder

Since the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

9.5.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one event.

9.5.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.5.7 4B5B Code Group

Table 1

Symbol	Meaning	4B Code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	Undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	Undefined	01101
R	ESD (2)	Undefined	00111
H	Error	Undefined	00100
V	Invalid	Undefined	00000
V	Invalid	Undefined	00001
V	Invalid	Undefined	00010
V	Invalid	Undefined	00011
V	Invalid	Undefined	00101
V	Invalid	Undefined	00110
V	Invalid	Undefined	01000
V	Invalid	Undefined	01100
V	Invalid	Undefined	10000
V	Invalid	Undefined	11001

9.6 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.

The receive section contains the following functional blocks:
- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.6.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.6.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.6.3 MLT-3 to NRZI Decoder

The DM9051(I) decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.6.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the
NRZI to NRZ decoder.

9.6.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to parallel conversion block.

9.6.6 Serial to Parallel

The serial to parallel converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.6.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the serial to parallel converter, and it descrambles the data streams, and presents the data streams to the code GGoup alignment block.

9.6.8 Code Group Alignment

The code group alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code group alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

9.6.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the reconciliation layer.

9.7 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9051(I) is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.8 Collision Detection

For Half-Duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in Full-Duplex operation.

9.9 Carrier Sense

Carrier Sense (CRS) in internal MII is asserted in Half-Duplex operation during transmission or reception of data. During Full-Duplex mode, CRS is asserted only during receive operations.

9.10 Auto-Negotiation

The objective of Auto-Negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-Negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-Negotiation also provides a parallel detection function for devices that do not support the Auto-Negotiation feature. During parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-Negotiation but support a common mode of operation to establish a link.

9.11 Power Reduced Mode

The signal detect circuit is always turned to monitor whether there is any signal on the media (cable disconnected).

The DM9051(I) automatically turns off the power and enters the Power Reduced mode, whether its operation mode is N-way or force mode. When enters the Power Reduced mode, the transmit circuit still sends out fast link pulse with minimum power consumption. If a valid signal is detected from the media, which might be N-ways fast link pulse, 10Base-T normal link pulse, or 100Base-TX MLT3 signals, the device will wake up and resume a normal operation mode.

That can be writing zero to PHY register 16 bit 4 to disable Power Reduced mode.

9.11.1 Power Down Mode

The PHY register 0 bit 11 can be set high to enter the power down mode, which disables all transmit and receive functions, except the access of PHY registers

10 DC Characteristics

10.1 Absolute Maximum Ratings (25°C) (DM9051I support -40°C~+85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD	Supply Voltage	-0.3	3.6	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	
Tstg	Storage Temperature Range	-65	+150	℃	
TA	Ambient Temperature	0	+70	℃	
TA	Ambient Temperature	-40	+85	℃	DM9051INP
LT	Lead Temperature (TL,soldering,10 sec.).	—	+260	℃	

10.1.1 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD	Supply Voltage	3.135	3.300	3.465	V	
PD (Power Dissipation)	100BASE-TX	---	142	---	mA	3.3V
	100BASE-TX (802.3az)	---	95	---	mA	3.3V
	10BASE-T TX	---	106	---	mA	3.3V
	Auto-Negotiation	---	49	---	mA	3.3V
	Power Down Mode	---	11	---	mA	3.3V

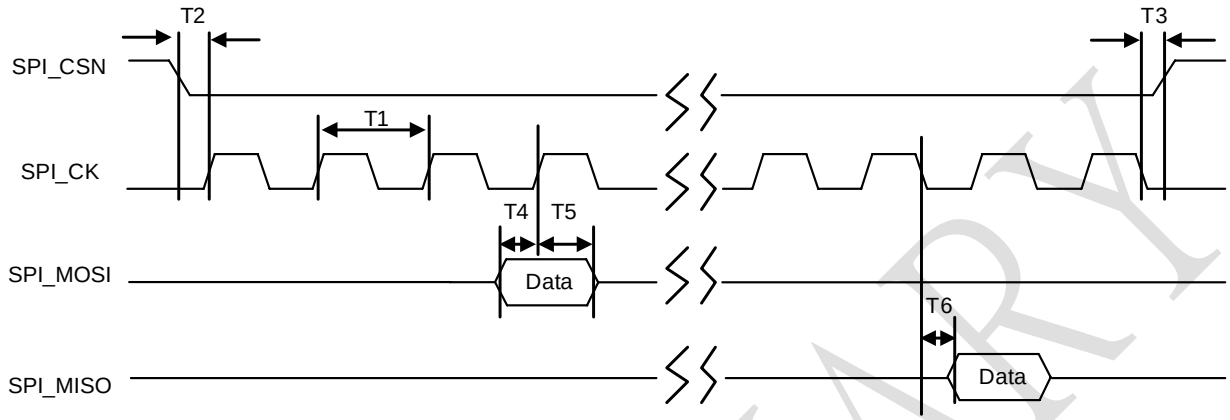
10.2 DC Electrical Characteristics (VDD = 3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	
VIH	Input High Voltage	2.0	-	-	V	
IIL	Input Low Leakage Current	-1	-	-	uA	Input Voltage = 0.0V
IIH	Input High Leakage Current	-	-	1	uA	Input Voltage = 3.3V
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

11 AC Electrical Characteristics & Timing Waveforms

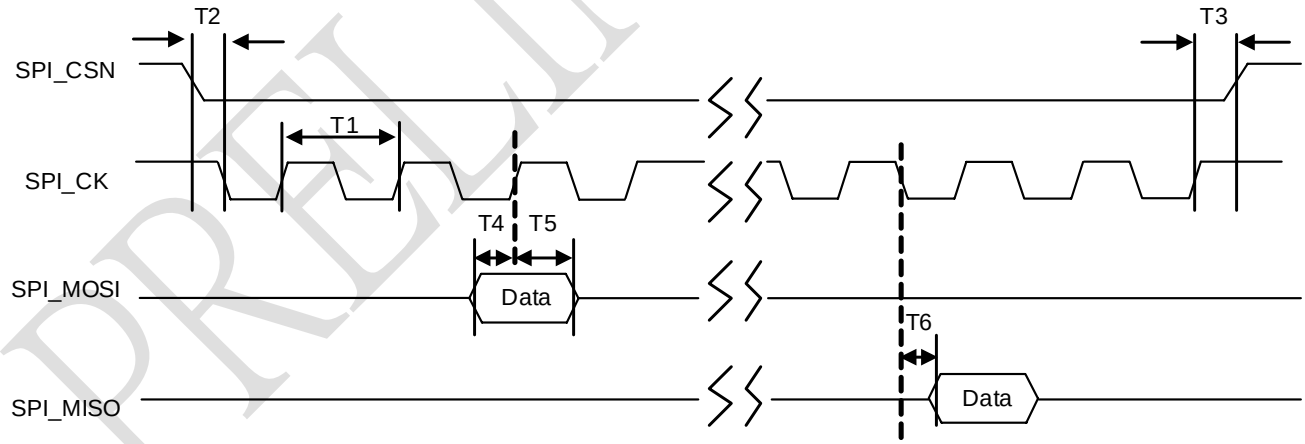
11.1 SPI Timing

M0 Mode



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SPI_CK Frequency	-	40	50	MHz
T2	SPI_CSN go low to SPI_CK go high	10	-	-	ns
T3	SPI_CK go low to SPI_CSN go high	10	-	-	ns
T4	SPI_MOSI setup time from SPI_CK go high	3	-	-	ns
T5	SPI_MOSI hold time after SPI_CK go high	3	-	-	ns
T6	SPI_MISO Output Delay after SPI_CK go low	5	6	7	ns

M3 Mode



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SPI_CK Frequency	-	40	50	MHz
T2	SPI_CSN go low to SPI_CK go low	0	-	-	ns
T3	SPI_CK go high to SPI_CSN go high	0	-	-	ns
T4	SPI_MOSI setup time from SPI_CK go high	3	-	-	ns
T5	SPI_MOSI hold time after SPI_CK go high	3	-	-	ns
T6	SPI_MISO output delay after SPI_CK go low	5	6	7	ns

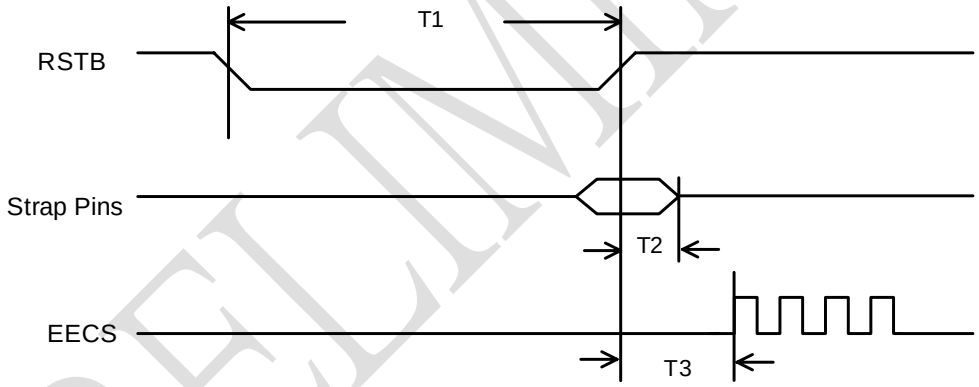
11.2 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	-
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	-
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	-
$T_{t/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	-
X_{OST}	100TX+/- Differential Voltage Overshoot	0	-	5	%	-

11.3 Oscillator/Crystal Timing

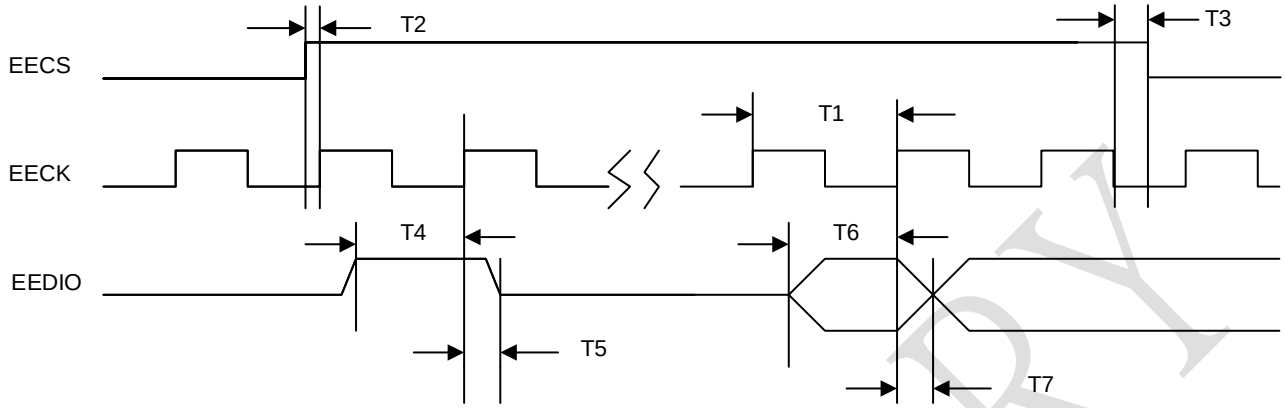
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_{CKC}	OSC Clock Cycle	39.9988	40	40.0012	ns	30ppm
T_{PWH}	OSC Pulse Width High	16	20	24	ns	-
T_{PWL}	OSC Pulse Width Low	16	20	24	ns	-

11.4 Power On Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	RSTB Low Period	1	-	-	ms	-
T2	Strap Pins hold time with RSTB	40	-		ns	-
T3	RSTB high to EECS high	-	9.5	-	us	-

11.5 EEPROM Interface Timing



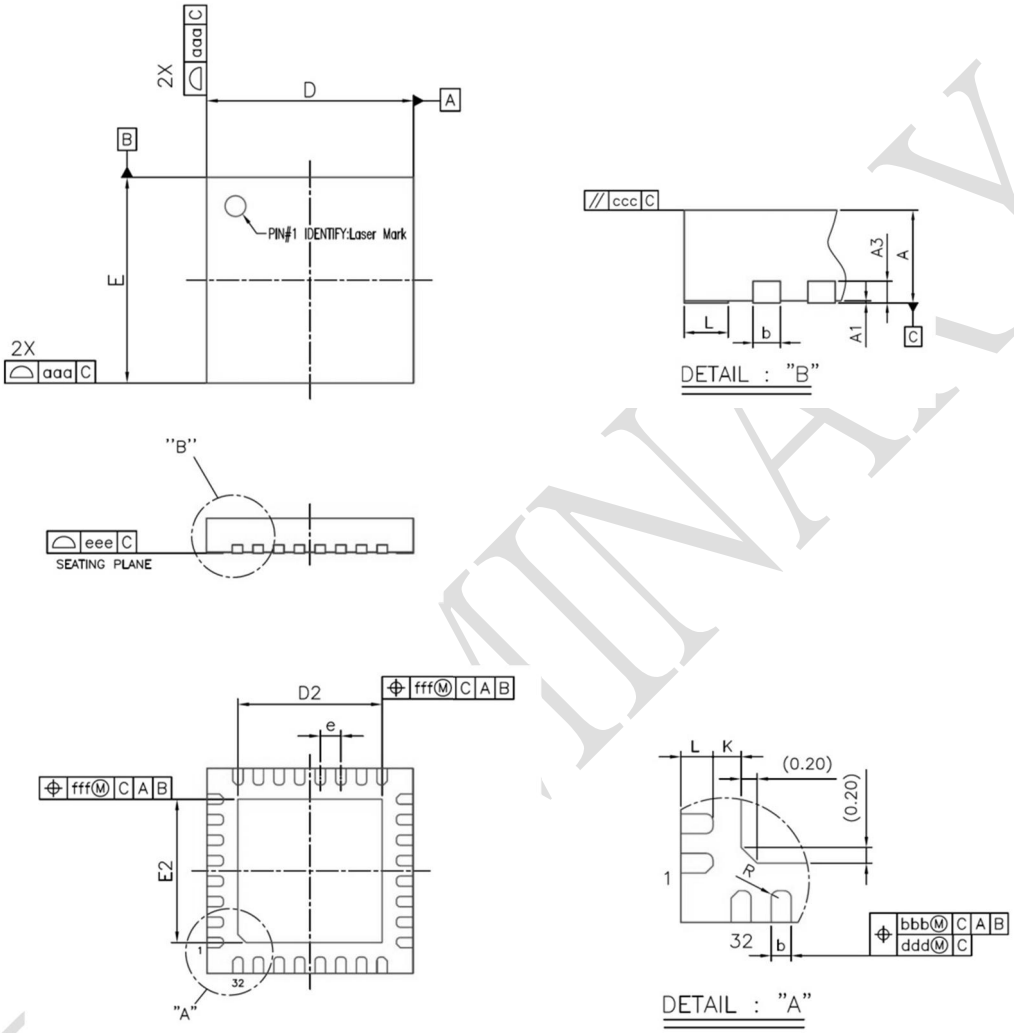
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECK Frequency	-	0.1953	-	MHz
T2	EECS setup time	-	960	-	ns
T3	EECS hold time	-	1600	-	ns
T4	EEDIO setup time when output	-	920	-	ns
T5	EEDIO hold time when output	-	4200	-	ns
T6	EEDIO setup time when input	15	-	-	ns
T7	EEDIO hold time when input	8	-	-	ns

11.6 LED (traffic ON/OFF timing) any LED as Traffic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	LED Traffic ON Time	-	16	-	ms
T2	LED Traffic OFF Time	64	-	-	ms

12 Package Information

32 Pins QFN Package Outline Information:



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.02 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2/E2	3.35	3.50	3.65	0.132	0.138	0.144
e	0.50 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20	---	---	0.008	---	---
R	0.09	---	---	0.004	---	---
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION: MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220

13 Ordering Information

Part Number	Pin Count	Package
DM9051NP	32	QFN(Pb-Free)
DM9051INP	32	QFN(Pb-Free)

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications.

Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6, Li-Hsin 6th Rd.,
Hsinchu Science Park,
Hsin-chu City 300, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.