

DMC-50448 (8 Characters × 2 lines) ● Display Fonts 5 × 8 Dots ● 1/16 Duty Drive

■ ABSOLUTE MAXIMUM RATINGS

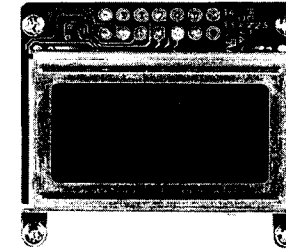
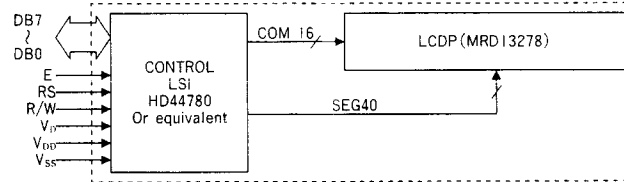
Item	Symbol	Test Condition	Standard Value		Unit
			min.	max.	
Supply Voltage for Logic	$V_{CC}-V_{SS}$	Ta=25°C	-0.3	7	V
Supply Voltage for LCD Drive	$V_{CC}-V_{EE}$	Ta=25°C	$V_{DD}-13.5$	$V_{DD}+0.3$	V
Input Voltage	V_I	Ta=25°C	-0.3	$V_{DD}+0.3$	V
Operating Temperature	Topr	—	0	+50	°C
Storage Temperature	Tstg	—	-20	+70	°C

■ ELECTRICAL CHARACTERISTICS

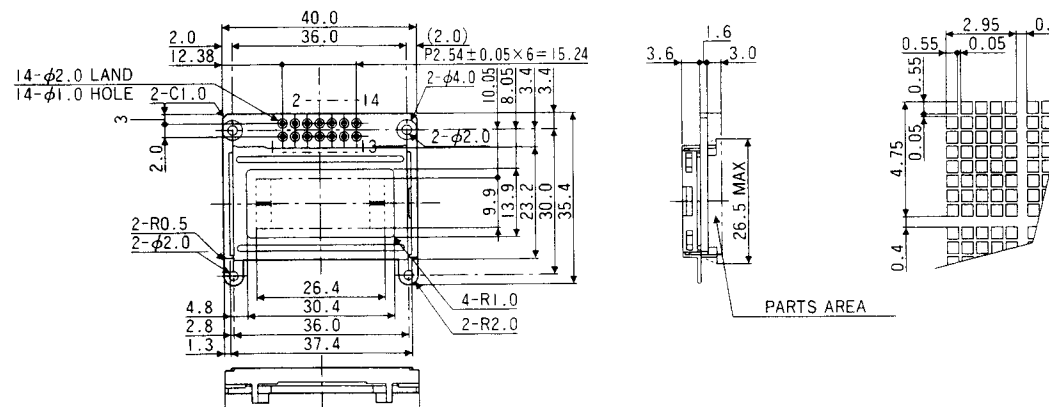
Item	Symbol	Test Condition	Standard Value			Unit
			min.	typ.	max.	
Input "High" Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input "Low" Voltage	V_{IL}	—	0	—	0.6	V
Output "High" Voltage	V_{OH}	$-I_{OH}=0.205mA$	—	—	—	V
Output "Low" Voltage	V_{OL}	$I_{OL}=1.2mA$	—	—	—	V
Supply Current	I_{CC}	$V_{CC}=5.0V$	—	2.0	8.5	mA

※ $V_{CC}=5.0V+5%$, Ta=25°C

■ BLOCK DIAGRAM



■ DIMENSION



DMC-16105 (16 Characters × 1 line) ● Display Fonts 5 × 8 Dots ● 1/16 Duty Drive

■ ABSOLUTE MAXIMUM RATINGS

■ ELECTRICAL CHARACTERISTICS

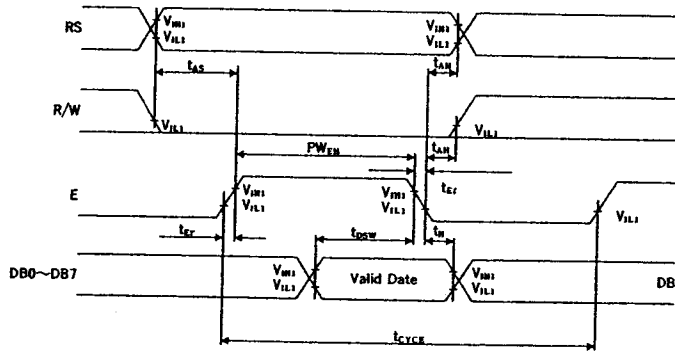
TIMING CHART (Except for DMC40401 series)

Enable Cycle Time	T_{CYCK}	Figs.1, 2	1000	—	—	ns
Enable Pulse Width, High Level	PW_{EH}	Figs.1, 2	450	—	—	ns
Enable Rise and Decay Time	t_{ER}, t_{EF}	Figs.1, 2	—	—	25	ns
Address Setup Time, RS, R/W-E	t_{AS}	Figs.1, 2	140	—	—	ns
Data Delay Time	t_{DDR}	Fig.2	—	—	320	ns
Data Setup Time	t_{DSW}	Fig.1	195	—	—	ns
Data Hold Time (Write Operation)	t_H	Fig.1	10	—	—	ns
Data Hold Time (Read Operation)	t_{DHR}	Fig.2	20	—	—	ns
Address Hold Time	t_{AH}	Figs.1, 2	10	—	—	ns

* $V_{CC}=5.0V \pm 10\%$, $GND=0V$, $T_a=-20 \sim +75^\circ C$

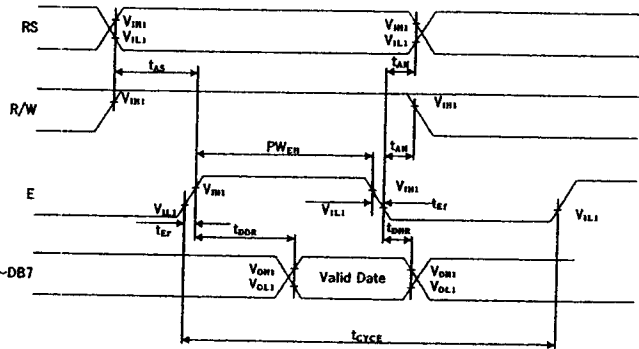
(In case controller LSI is HD44780)

FIG. 1 WRITE OPERATION



(Write Date from MPU to MODULE)

FIG. 2 READ OPERATION



(Read Date from MODULE TO MPU)

PIN ASSIGNMENT

1	V_{SS}	—	Power Supply	0V (GND)
2	V_{CC}	—		+5V
3	V_{EE}	—		for LGD Drive
4	RS	H/L	Register Select Signal Register H: Data Input Select L: Instruction Input	
5	R/W	H/L	H: Data Read (Module→MPU) L: Data Write (Module→MPU)	
6	E	H, H→L	Enable Signal (No pull-up Resistor)	
7	DB0	H/L	Data Bus Line	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

*Interface between Data Bus Line and 4-bit or 8-bit MPU is available. Data transfer are made in twice in case of 4-bit MPU, and once in case of 8-bit MPU.

■IF INTERFACE DATA IS 4-BIT LONG

Data transfer are made through 4 bus lines from DB4 to DB7, while the rest of 4 bus lines from DB0 to DB3 are not used. Data transfer with MPU are completed when 4-bit data are transferred in twice, first upper 4-bit data, then lower 4-bit data.

■IF INTERFACE DATA IS 8-BIT LONG

Data transfer are made through all of 8 bus lines from DB0 to DB7.

*Please refer to pp.80~81 for pin assignment of DMC 40457 series and DMC40401N series.

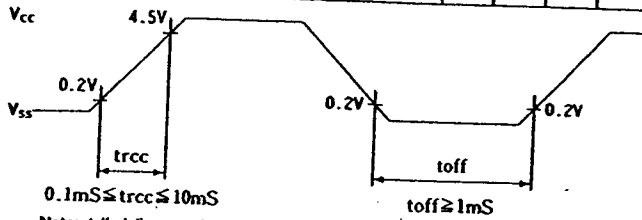
POWER SUPPLY RESET (Except for DMC40401 series)

※In case control LSI is HD44780

The internal reset circuit will be operated properly when the following power supply conditions are satisfied.

If it is not operated properly, please perform initial setting along with the instruction.

Item	Symbol	Measuring Condition	Standard Value			Unit
			min.	typ.	max.	
Power Supply Rise Time	trcc	—	0.1	—	10	mS
Power Supply OFF Time	toff	—	1	—	—	mS



Note: toff defines period that power supply is off when power supply shuts down momentarily or repeats on / off state.

RESET FUNCTION

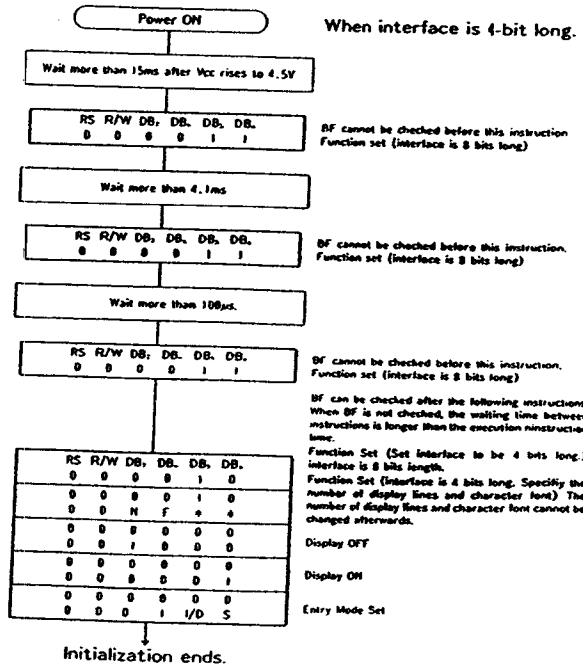
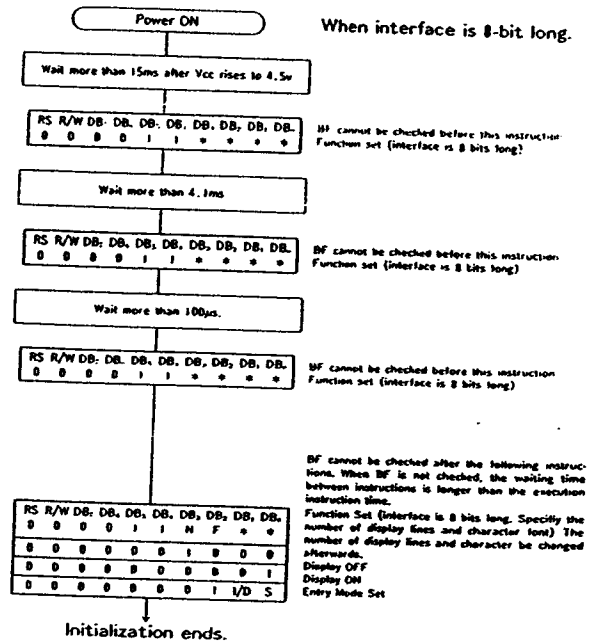
● Initialization made by Internal Reset Circuit
 HD44780 automatically initializes (resets) when power is supplied (built-in internal reset circuit). The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10ms after Vcc reach to 4.5V.

- (1) Display clear
- (2) Function set
 - DL=1: 8bit long interface data
 - DL=0: 4bit F=0: 5×7dot character font
 - N=1: 2lines
 - N=0: 1line
- (3) Display ON/OFF control
 - D=0: Display OFF C=0: Cursor OFF B=0: Blink OFF
- (4) Entry mode set
 - I/D=1: +(increment) S=0: No shift

Note: When conditions stated in "Power Supply Conditions Using Reset Circuit" are not satisfied, the internal reset circuit will not operate properly and initialization will not be performed. Please make initialization using MPU along with "Initialization along with Instruction"

● Initialization along with Instruction

If power supply conditions are not satisfied, which for proper operation of internal reset circuit, it is required to make initialization along with instruction. Please make following procedures:



DMC Series

INSTRUCTIONS (Except for DMC40401 series)

Instruction	R ₀	R ₁	R ₂	R ₃	R ₄	R ₅	R ₆	R ₇	R ₈	R ₉	Operation	Execution Time
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	
Cursor At Home	0	0	0	0	0	0	0	0	0	1	* Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position DDAM contents remain unchanged.	1.64mS
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	1.64mS
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D) cursor ON/OFF (C), and blink of cursor position character (B).	40μS
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DDRAM contents.	40μS
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length(DL), number of display lines(N) and character font(F).	40μS
CGRAM Address Set	0	0	0	1	ACG					Sets the CGRAM, data is sent and received after this setting.		40μS
DDRAM Address Set	0	0	1	ADD					Sets the CGRAM, data is sent and received after this setting.		40μS	
Busy Flag/ Address Read	0	1	BF	AC					Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.		40μS	
CGRAM/DDRAM Data Write	1	0	WRITE DATA					Writes data into DDRAM or CGRAM.		0μS		
CGRAM/DDRAM Data Read	1	1	READ DATA					Reads data into DDRAM or CGRAM.		40μS		

Note

I/D=1: Increment
 I/D=0: Decrement
 S=1: With display shift
 S/C=1: Display shift
 S/C=0: Cursor movement
 R/L=1: Shift to the right
 R/L=0: Shift to the left
 DL=1: 8-bit

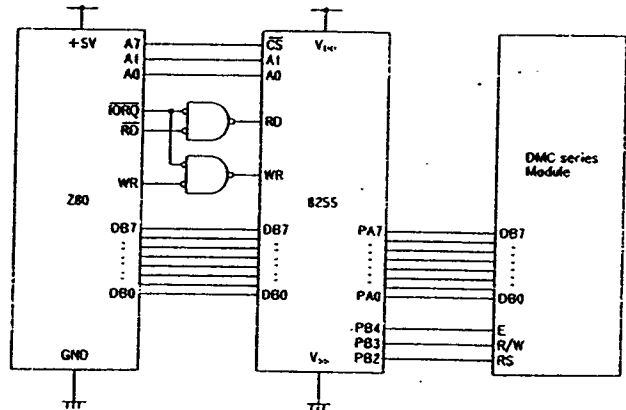
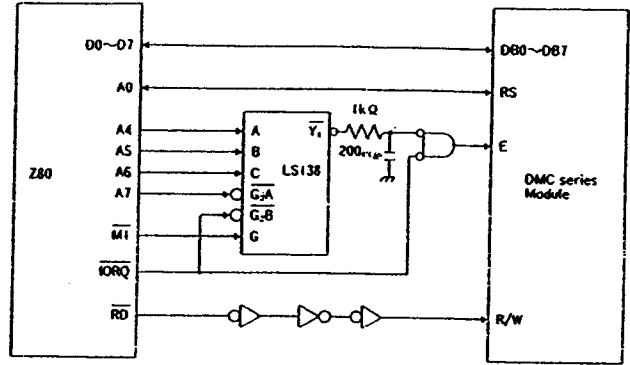
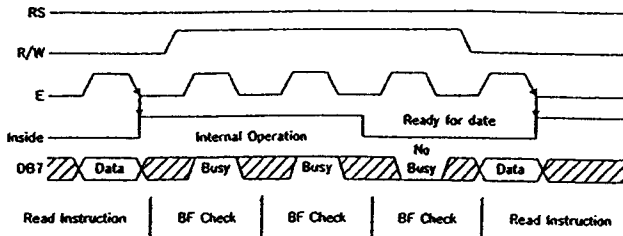
DL=0: 4-bit
 N=1: 2 Rows
 N=0: 1 Row
 F=1: 5×10dots
 F=0: 5×7dots
 BF=1: Internal operation is being performed
 BF=0: Instruction acceptable

DDRAM: Display Data RAM
 CGRAM: Character Generator RAM
 ACG: CGRAM Address
 ADD: DDRAM Address Corresponds to cursor address.
 AC: Address Counter, used for both DDRAM and CGRAM
 *: Invalid

f_{cp} or f_{osc}=250kHz
 However, when frequency changes, execution time also changes

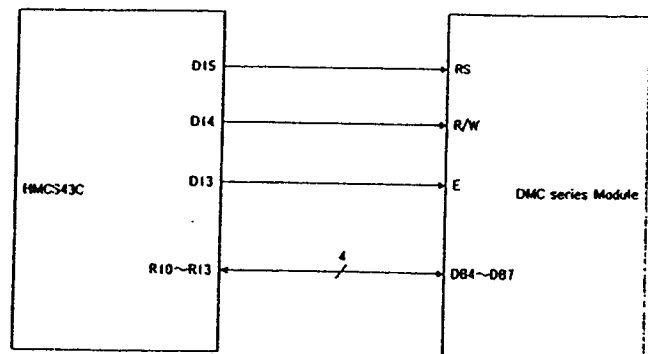
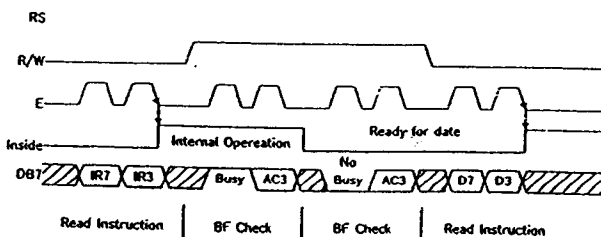
Ex
 If f_{cp} or f_{osc} is 250kHz,
 $37\mu S \times \frac{270}{250} = 40\mu S$

Example of Interface with 8-bit MPU (Z80)



Example of Interface with 4-bit MPU (HMCS43C)

Interface with 4-bit MPU can be made through I/O port of 4-bit MPU. If there are enough I/O ports, data can be transferred by 8-bit, however, if there isn't, data transfer can be done by 4-bit twice (select interface is 4-bit long), and timing sequence will be complicated in this case. Please take into account that 2 cycles of BF check is necessary, while 2 cycles of data transfer are also necessary.



Note: IR7, IR3: 7th bit, 3rd bit of instruction
AC3: 3th bit of Address Counter

DMC Series

Code	Description	Executed time (max)
I/D=1: Increment I/D=0: Decrement S=1: With display shift S/C=1: Display shift S/C=0: Cursor movement R/L=1: Shift to the right R/L=0: Shift to the left DL=1: 8-bit	DL=0: 4-bit N=1: 2 Rows N=0: 1 Row F=1: 5x10dots F=0: 5x7dots BF=1: Internal operation is being performed BF=0: Instruction acceptable	fcp or fosc=250kHz However, when frequency changes, execution time also changes Ex If fcp or fosc is 250kHz, $37\mu S \times \frac{270}{250} = 40\mu S$
	DDRAM: Display Data RAM CGRAM: Character Generator RAM ACG: CGRAM Address ADD: DDRAM Address Corresponds to cursor address. AC: Address Counter, used for both DDRAM and CGRAM *: Invalid	

FONT TABLE (5x11 Dots)

Code	CG RAM	Font
x x x x 0000	111	0 1 2 3 4 5 6 7 8 9
x x x x 0001	(12)	! " # \$ % & ' () * + , - . /
x x x x 0010	(13)	: ; < = > ? @ A B C D E F G H
x x x x 0011	(14)	I J K L M N O P Q R S T U V W X Y Z
x x x x 0100	(15)	[\] ^ _ ` { } ~
x x x x 0101	(16)	! " # \$ % & ' () * + , - . /
x x x x 0110	(17)	: ; < = > ? @ A B C D E F G H
x x x x 0111	(18)	I J K L M N O P Q R S T U V W X Y Z
x x x x 1000	(11)	0 1 2 3 4 5 6 7 8 9
x x x x 1001	(12)	! " # \$ % & ' () * + , - . /
x x x x 1010	(13)	: ; < = > ? @ A B C D E F G H
x x x x 1011	(14)	I J K L M N O P Q R S T U V W X Y Z
x x x x 1100	(15)	[\] ^ _ ` { } ~
x x x x 1101	(16)	! " # \$ % & ' () * + , - . /
x x x x 1110	(17)	: ; < = > ? @ A B C D E F G H
x x x x 1111	(18)	I J K L M N O P Q R S T U V W X Y Z

(5x8Dots)

0 1
2 3
4 5
6 7
8 9
: ;
< =
> ?
@ A
B C
D E
F G
H I
J K
L M
N O
P Q
R S
T U
V W
X Y
Z
[\
] ^
_ `
{
} ~
! " #
\$ % &
' ()
* + ,
- . /
: ; <
= > ?
@ A B
C D E
F G H
I J K
L M N
O P Q
R S T
U V W
X Y Z
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^ _ `
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~
! " #
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= > ?
@ A B
C D E
F G H
I J K
L M N
O P Q
R S T
U V W
X Y Z
[\]
^ _ `
{ }
~

*CGRAM is Character Generator RAM which memorize characters that you can freely input by program.
 *32 characters stated under upper 4-bit of 1110 and 1111 are 5x10 dots, and part of which is cut when you use in display which display fonts is 5x7 dots.
 Please note.

5x11 dots type product:
 DMC16106A, DMC32132, DMC40131