

**COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET**

**Product Summary**

Device	BV <sub>DSS</sub>	R <sub>DS(ON)</sub> max	I <sub>D</sub> max T <sub>A</sub> = +25°C
Q1 N-Channel	12V	25mΩ @ V <sub>GS</sub> = 4.5V	6.0A
		30mΩ @ V <sub>GS</sub> = 3.3V	5.5A
		32mΩ @ V <sub>GS</sub> = 2.5V	5.3A
Q2 P-Channel	-20V	80mΩ @ V <sub>GS</sub> = -4.5V	-3.4A
		90mΩ @ V <sub>GS</sub> = -3.3V	-3.2A
		100mΩ @ V <sub>GS</sub> = -2.5V	-3.0A

**Features**

- Low On-Resistance
- Low Input Capacitance
- Low Profile, 0.6mm Max Height
- **ESD HBM Protected up to 1.5KV, MM Protected up to 150V.**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

**Description**

This MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

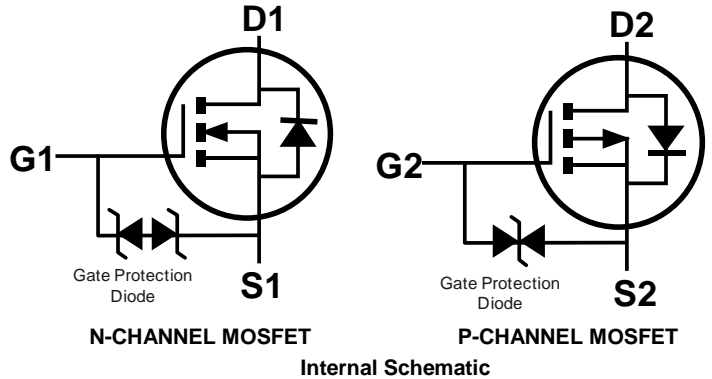
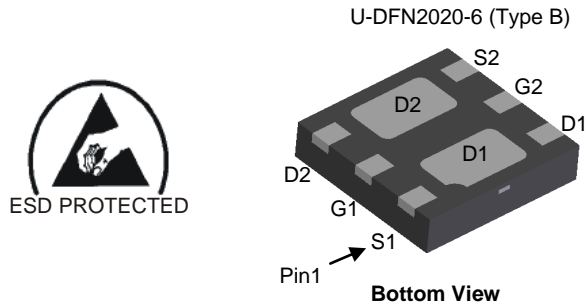
**Applications**

Optimized for Point of Load (POL) Synchronous Buck Converter that steps down from 3.3V to 1V for core voltage supply to ASICs. Target applications are Ethernet Network Controllers used in:

- Routers, Switchers, Network Interface Controllers (NICs)
- Digital Subscriber Line (DSL)
- Set-Top Boxes (STBs)

**Mechanical Data**

- Case: U-DFN2020-6 (Type B)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Terminals Connections: See Diagram Below
- Weight: 0.0065 grams (Approximate)

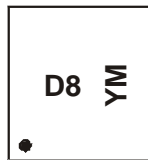


**Ordering Information** (Note 4)

Part Number	Case	Packaging
DMC1028UFDB-7	U-DFN2020-6 (Type B)	3,000/Tape & Reel
DMC1028UFDB-13	U-DFN2020-6 (Type B)	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**



D8 = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year (ex: C = 2015)  
 M = Month (ex: 9 = September)

Date Code Key

Year	2015	2016	2017	2018	2019	2020	2021
Code	C	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1 N-CHANNEL	Q2 P-CHANNEL	Units
Drain-Source Voltage			V <sub>DSS</sub>	12	-20	V
Gate-Source Voltage			V <sub>GSS</sub>	±8	±8	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	6.0 4.8	-3.4 -2.7	A
	t < 5s	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	7.1 5.7	-4.0 -3.2	A
Maximum Continuous Body Diode Forward Current (Note 5)			I <sub>S</sub>	1.4	-1.4	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)			I <sub>DM</sub>	40	-20	A
Avalanche Current L = 0.1mH			I <sub>AS</sub>	12	-12	A
Avalanche Energy L = 0.1mH			E <sub>AS</sub>	8.4	7.5	mJ

**Thermal Characteristics**

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	Steady State	P <sub>D</sub>	1.36	W
	t < 5s		1.89	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R <sub>θJA</sub>	92	°C/W
	t < 5s		66	
Thermal Resistance, Junction to Case (Note 5)		R <sub>θJC</sub>	19	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Note: 5. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.

**Electrical Characteristics Q1 N-CHANNEL** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 6)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	12	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	-	-	1.0	μA	V <sub>DS</sub> = 12V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 6)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.4	-	1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	17	25	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5.2A
		-	19	30		V <sub>GS</sub> = 3.3V, I <sub>D</sub> = 5.0A
		-	21	32		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 4.8A
		-	30	40		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 2.5A
Diode Forward Voltage	V <sub>SD</sub>	-	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 7)</b>						
Input Capacitance	C <sub>ISS</sub>	-	787	-	pF	V <sub>DS</sub> = 6V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>OSS</sub>	-	203	-	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	-	177	-	pF	
Gate Resistance	R <sub>g</sub>	-	4.8	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 3.3V)	Q <sub>g</sub>	-	7.9	-	nC	V <sub>DS</sub> = 6V, I <sub>D</sub> = 6.8A
Total Gate Charge (V <sub>GS</sub> = 4.5V)		-	10.5	-	nC	
Total Gate Charge (V <sub>GS</sub> = 8V)		-	18.5	-	nC	
Gate-Source Charge	Q <sub>gs</sub>	-	1.2	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	2.9	-	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	-	4.6	-	ns	
Turn-On Rise Time	t <sub>r</sub>	-	9.4	-	ns	V <sub>DD</sub> = 6V, V <sub>GS</sub> = 4.5V, R <sub>L</sub> = 1.1Ω, R <sub>G</sub> = 1Ω
Turn-Off Delay Time	t <sub>D(OFF)</sub>	-	15.7	-	ns	
Turn-Off Fall Time	t <sub>f</sub>	-	3.7	-	ns	
Body Diode Reverse Recovery Time	t <sub>RR</sub>	-	12.0	-	ns	I <sub>S</sub> = 5.4A, dI/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	-	1.8	-	nC	I <sub>S</sub> = 5.4A, dI/dt = 100A/μs

**Electrical Characteristics Q2 P-CHANNEL** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 6)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	-	-	-1.0	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 6)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.4	-	-1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	55	80	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3.8A
		-	63	90		V <sub>GS</sub> = -3.3V, I <sub>D</sub> = -3.5A
		-	70	100		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -3.3A
		-	88	140		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -1.0A
		-	110	210		V <sub>GS</sub> = -1.5V, I <sub>D</sub> = -0.5A
		-	-	-		-
Diode Forward Voltage	V <sub>SD</sub>	-	-0.7	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A
<b>DYNAMIC CHARACTERISTICS (Note 7)</b>						
Input Capacitance	C <sub>ISS</sub>	-	576	-	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>OSS</sub>	-	87	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	71	-	pF	
Gate Resistance	R <sub>g</sub>	-	15	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = -3.3V)	Q <sub>g</sub>	-	5.2	-	nC	V <sub>DS</sub> = -10V, I <sub>D</sub> = -4.9A
Total Gate Charge (V <sub>GS</sub> = -4.5V)		-	6.7	-	nC	
Total Gate Charge (V <sub>GS</sub> = -8V)		-	11.5	-	nC	
Gate-Source Charge	Q <sub>gs</sub>	-	1.0	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	2.0	-	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	-	3.5	-	ns	
Turn-On Rise Time	t <sub>r</sub>	-	3.6	-	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	-	20.8	-	ns	
Turn-Off Fall Time	t <sub>f</sub>	-	12.7	-	ns	
Body Diode Reverse Recovery Time	t <sub>RR</sub>	-	13.1	-	ns	
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	-	3.9	-	nC	I <sub>S</sub> = -3.9A, dI/dt = 100A/μs

Notes: 6. Short duration pulse test used to minimize self-heating effect.  
7. Guaranteed by design. Not subject to product testing.

**Typical Characteristics - N-CHANNEL**

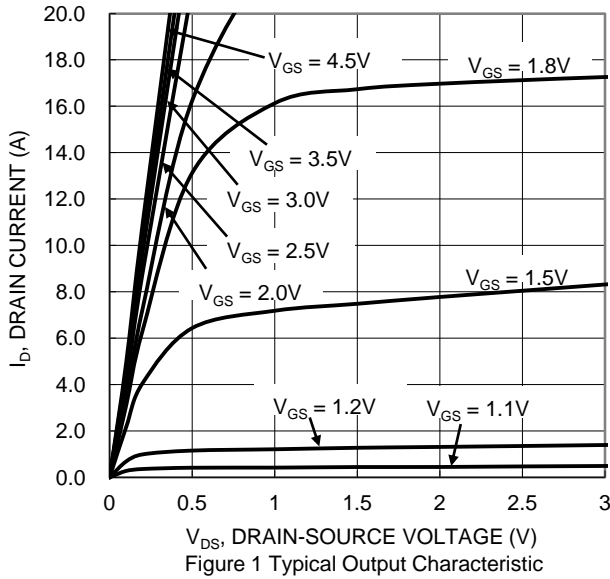


Figure 1 Typical Output Characteristic

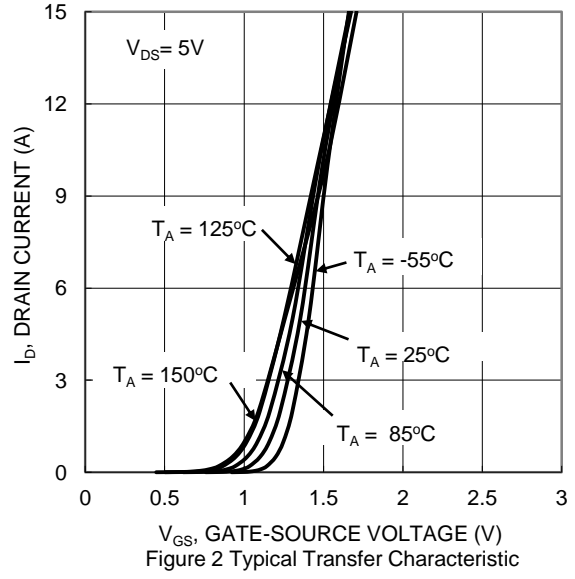


Figure 2 Typical Transfer Characteristic

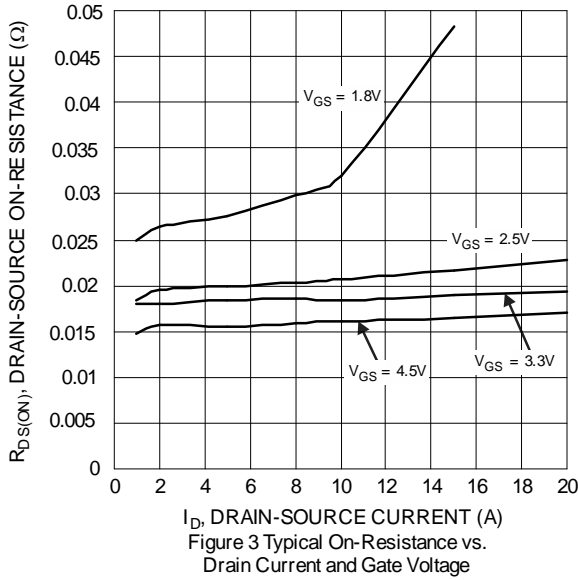


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

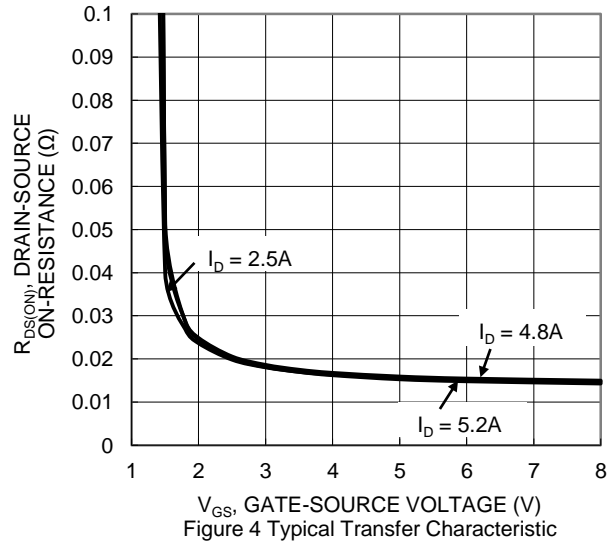


Figure 4 Typical Transfer Characteristic

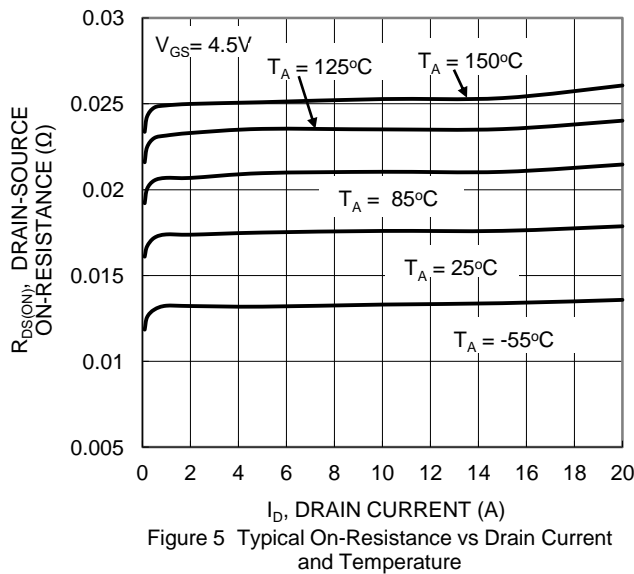


Figure 5 Typical On-Resistance vs Drain Current and Temperature

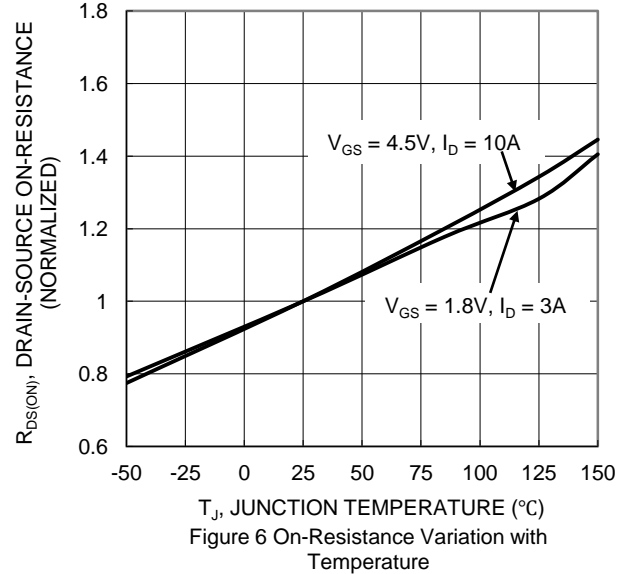


Figure 6 On-Resistance Variation with Temperature

**Typical Characteristics - N-CHANNEL** (continued)

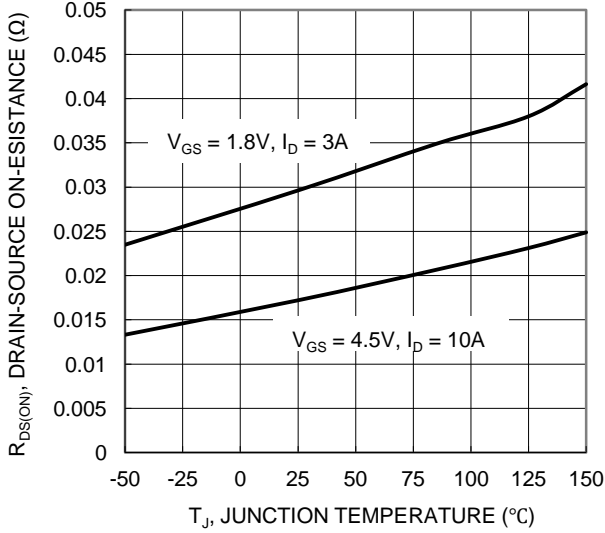


Figure 7 On-Resistance Variation with Temperature

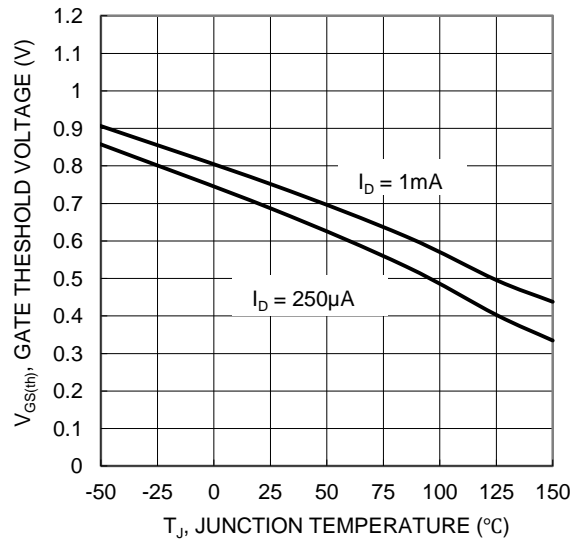


Figure 8 Gate Threshold Variation vs Junction Temperature

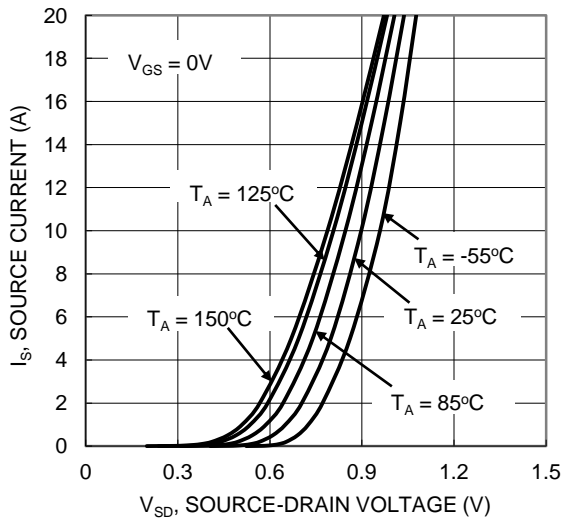


Figure 9 Diode Forward Voltage vs. Current

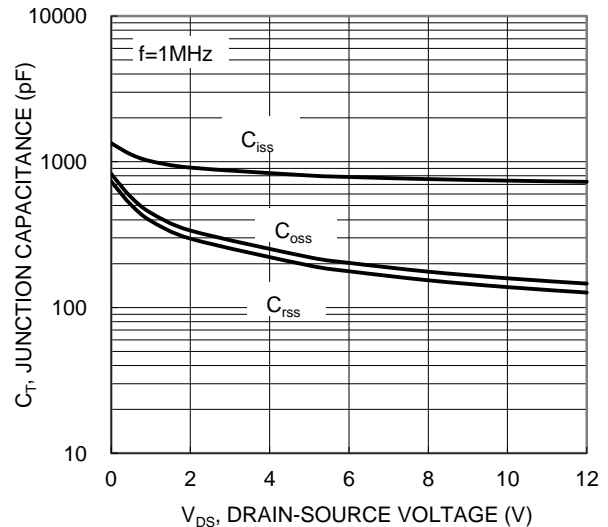


Figure 10 Typical Junction Capacitance

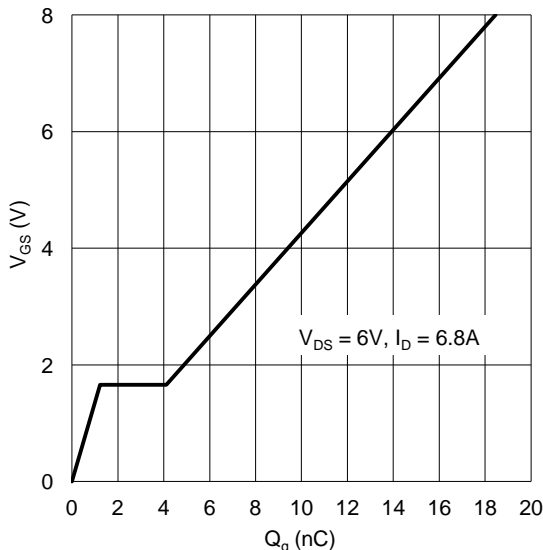


Figure 11 Gate Charge

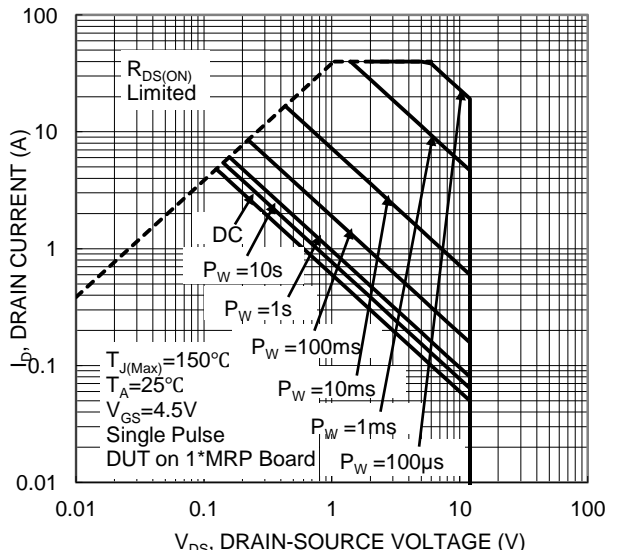


Figure 12 SOA, Safe Operation Area

**Typical Characteristics - P-CHANNEL**

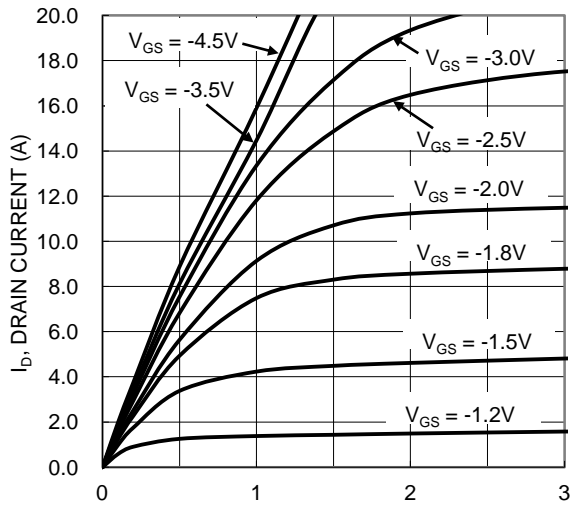


Figure 13 Typical Output Characteristic

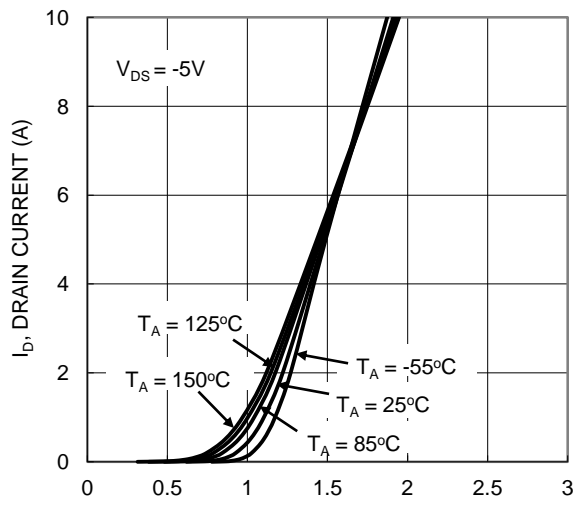


Figure 14 Typical Transfer Characteristic

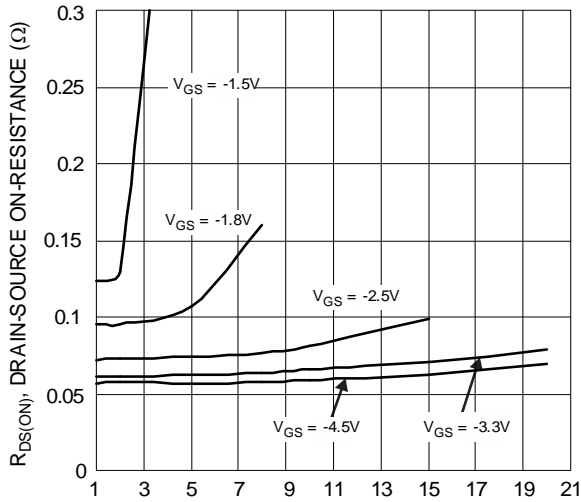


Figure 15 Typical On-Resistance vs. Drain Current and Gate Voltage

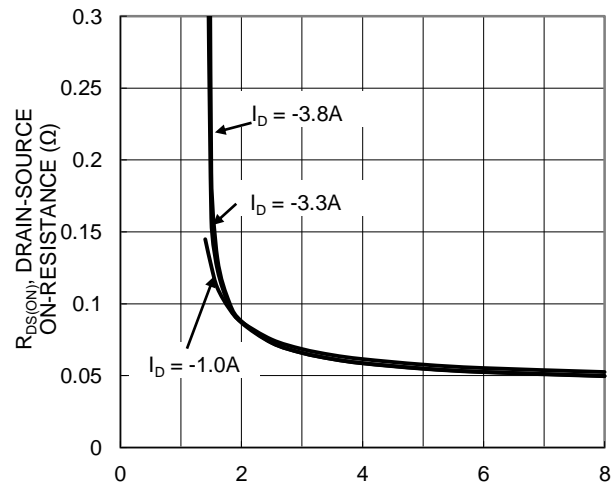


Figure 16 Typical Transfer Characteristic

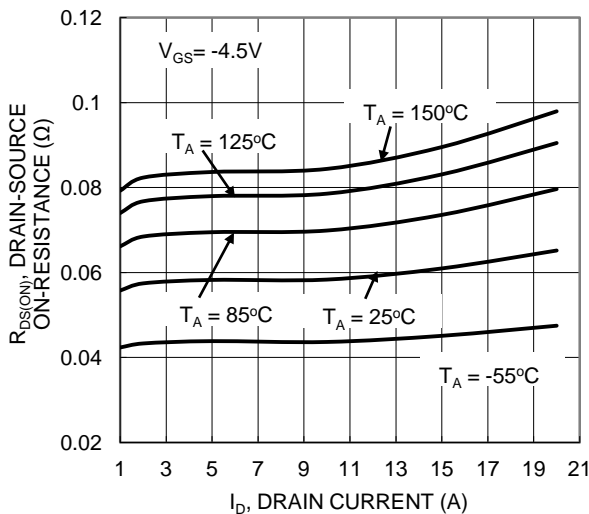


Figure 17 Typical On-Resistance vs Drain Current and Temperature

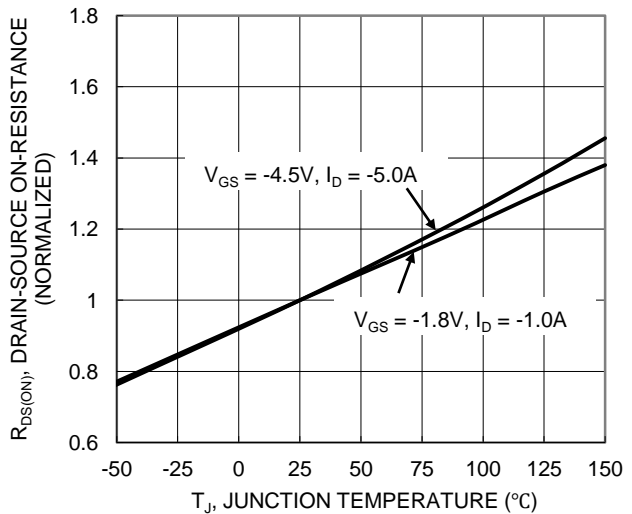
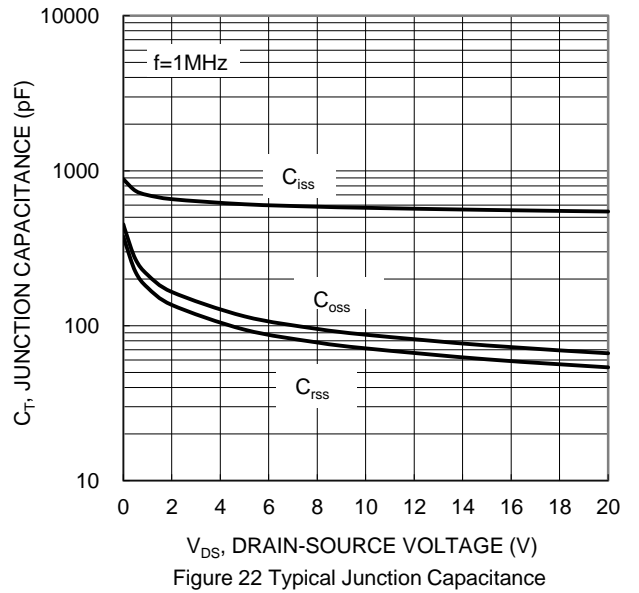
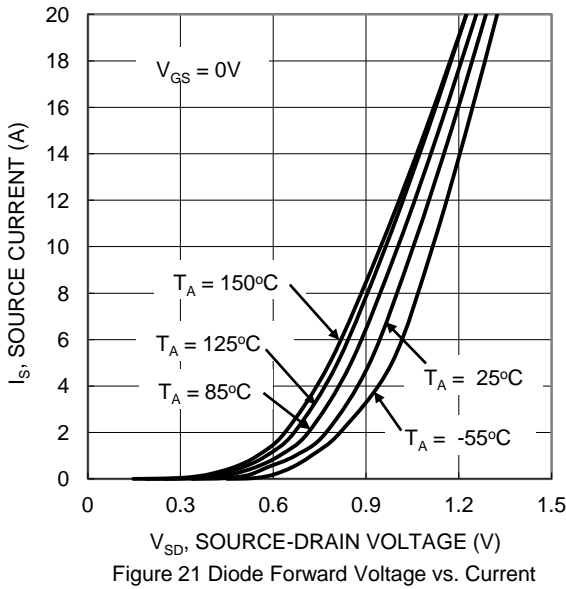
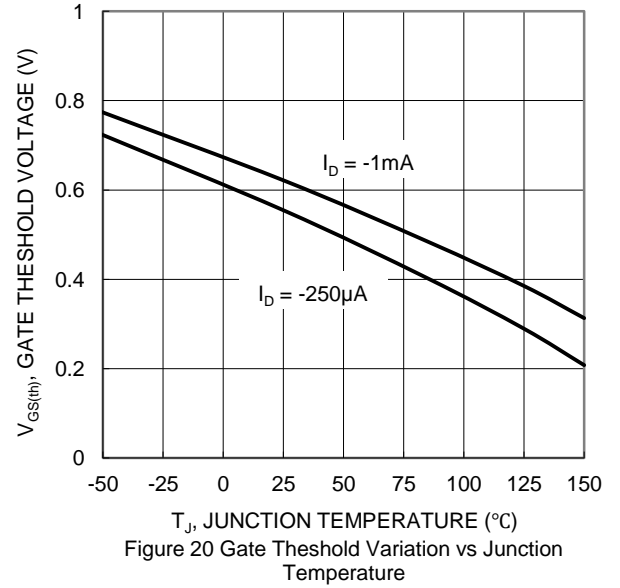
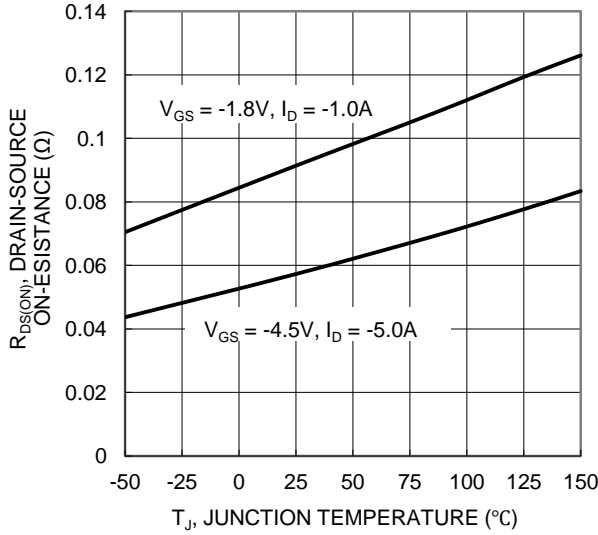
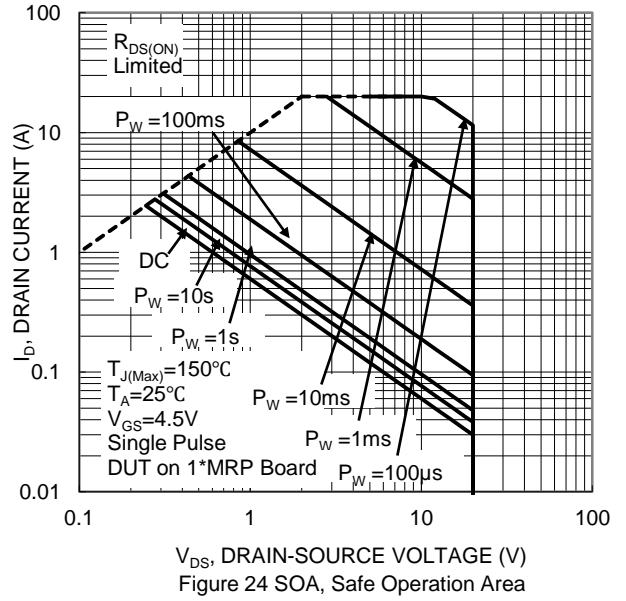
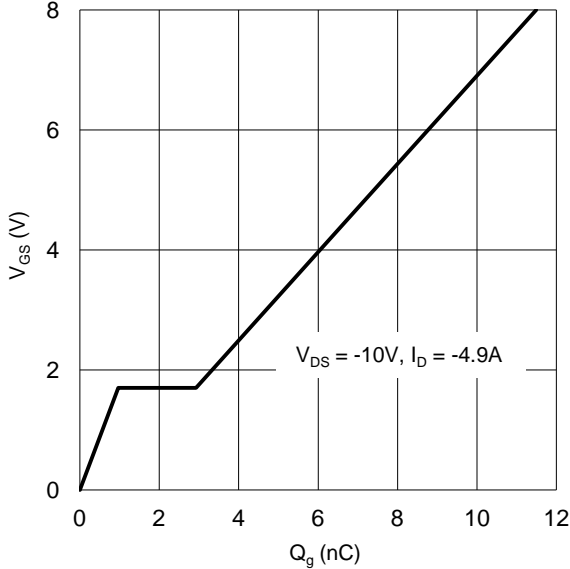


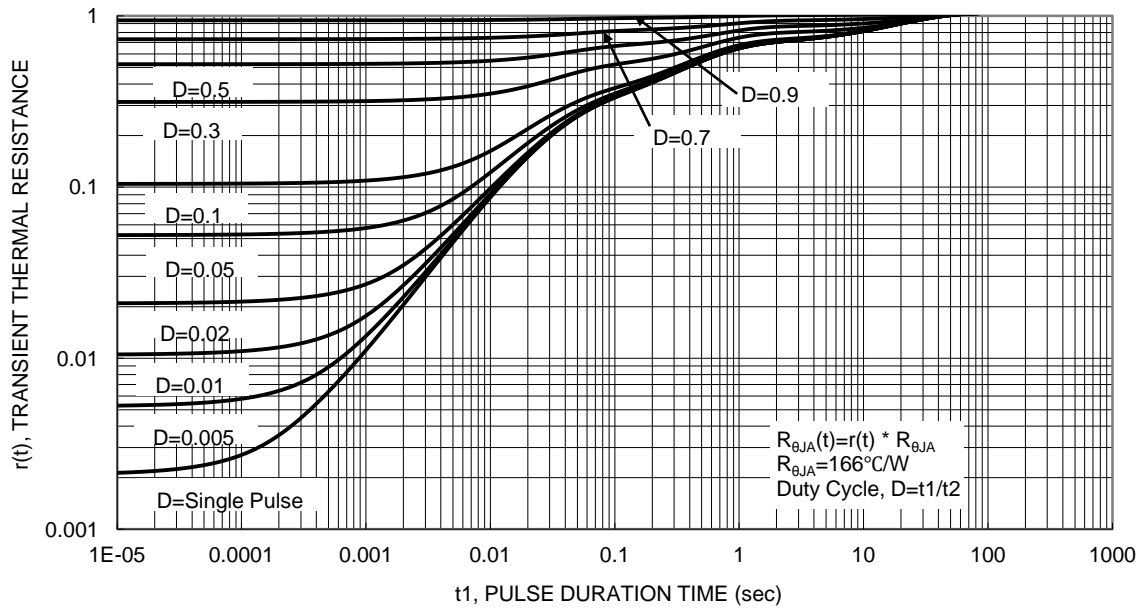
Figure 18 On-Resistance Variation with Temperature

**Typical Characteristics - P-CHANNEL** (continued)



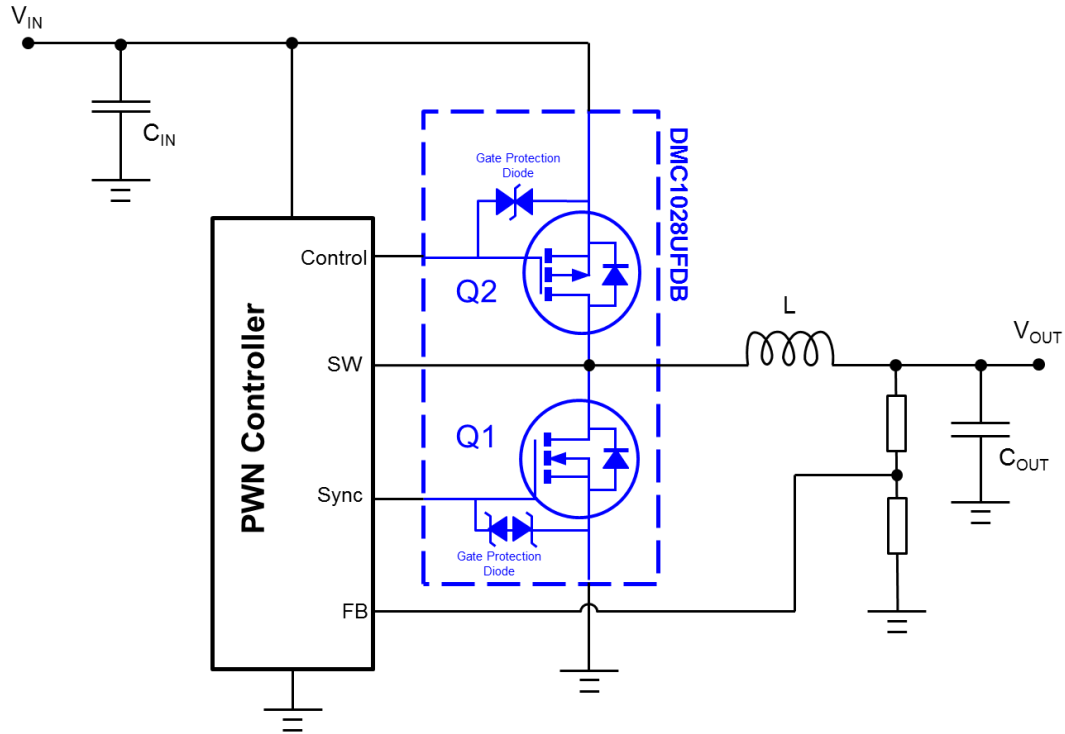


**Typical Characteristics - P-CHANNEL** (cont.)





**Typical Application Circuit**

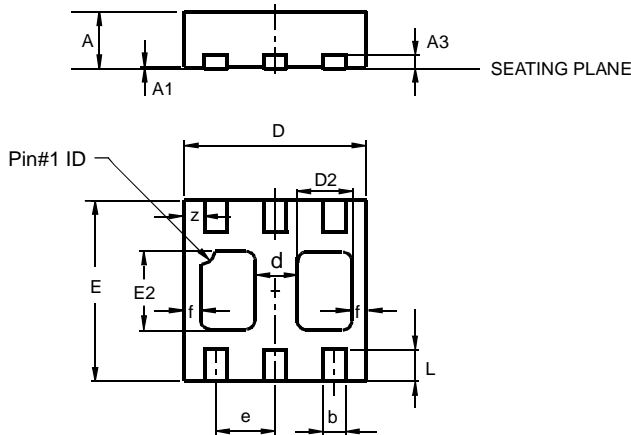


Example of a 3.3V to 1V POL Buck Converter using the DMC1028UFDB

DMC1028UFDB is designed for Point-of-Load (POL) converter that is stepping down from a nominal 3.3V to 1V with a load current up to 3A. This is implemented with a separate ASIC that is PWM signaling the complementary MOSFETs to act as a synchronous buck converter. The control switch (Q2) is implemented with P-channel MOSFETs to avoid needing a charge pump and with the 3.3V to 1V step down, which has a duty cycle of 33%. This means that for 67% of the cycle, the synchronous switch (Q1) is on and efficiency is dominated by the conduction losses; hence, the need for low  $R_{DS(on)}$  N-channel MOSFETs. Whereas for the control switch (Q2), the gate charge needs to be minimized as the switching losses become significant.

**Package Outline Dimensions**

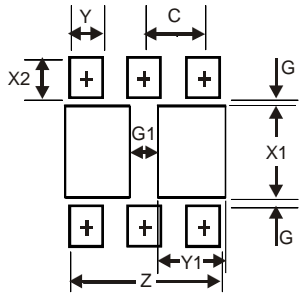
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



U-DFN2020-6 Type B			
Dim	Min	Max	Typ
A	0.545	0.605	0.575
A1	0	0.05	0.02
A3	—	—	0.13
b	0.20	0.30	0.25
D	1.95	2.075	2.00
d	—	—	0.45
D2	0.50	0.70	0.60
e	—	—	0.65
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
f	—	—	0.15
L	0.25	0.35	0.30
z	—	—	0.225
All Dimensions in mm			

## Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	1.67
G	0.20
G1	0.40
X1	1.0
X2	0.45
Y	0.37
Y1	0.70
C	0.65

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