



COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET POWERDI3333-8

Product Summary

Device	BVDSS	Rds(on) Max	I _D Max T _C = +25°C
01	201/	$35m\Omega$ @ V _{GS} = 10V	5.5A
Q1 20V	40mΩ @ V _{GS} = 4.5V	5.1A	
Q2	-20V	120mΩ @ V _G S = -4.5V	-3.0A
QZ	-20V	150mΩ @ V _{GS} = -2.5V	-2.6A

Description

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

Applications

- · Power-management functions
- Analog switches

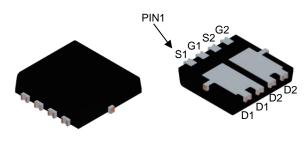
Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Wettable Flank for Improved Optical Inspection
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

Mechanical Data

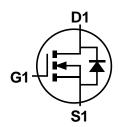
- Package: POWERDI[®]3333-8
- Package Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 ©3
- Weight: 0.072 grams (Approximate)

POWERDI® 3333-8/SWP (Type UXD)

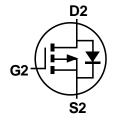


Top View Bottom View

Equivalent Circuit



N-Channel MOSFET



P-Channel MOSFET

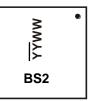
Ordering Information (Note 4)

Orderable Part Number	Dookogo	Packing		
Orderable Part Number	Package	Qty.	Carrier	
DMC2058UDVW-7	POWERDI®3333-8/SWP (Type UXD)	2,000	Tape & Reel	
DMC2058UDVW-13	POWERDI®3333-8/SWP (Type UXD)	3,000	Tape & Reel	

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



BS2 = Product Type Marking Code

YYWW = Date Code Marking

YY = Last Two Digits of Year (ex: 24 for 2024)

WW = Week Code (01 to 53)



Maximum Ratings Q1 - N-Channel (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	Vgss	±12	V
Continuous Drain Current, V _{GS} = 10V (Note 6)	I _D	5.5 4.4	А
Maximum Body Diode Forward Current (Note 6)	Is	1.8	Α
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)	I _{DM}	21	Α
Avalanche Current (L = 0.1mH) (Note 8)	las	10	Α
Avalanche Energy (L = 0.1mH) (Note 8)	E _{AS}	5	mJ

Maximum Ratings Q2 - P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage		VDSS	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Continuous Drain Current, Vgs = -4.5V (Note 6)	ID	-3.0 -2.3	Α	
Maximum Body Diode Forward Current (Note 6)		ls	-1.7	Α
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)	I _{DM}	-17	Α	
Avalanche Current (L = 0.1mH) (Note 8)	las	-11	Α	
Avalanche Energy (L = 0.1mH) (Note 8)	Eas	6.4	mJ	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	PD	0.87	W	
Thermal Resistance, Junction to Ambient (Note 5) Steady State		RθJA	143	°C/W
Total Power Dissipation (Note 6)		P_{D}	1.6	W
Thermal Resistance, Junction to Ambient (Note 6) Steady State		RθJA	78	°C/W
Thermal Resistance, Junction to Case (Note 7)	$R_{ heta JC}$	20	C/VV	
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
- 7. Thermal resistance from junction to soldering point (on the exposed drain pad).
- 8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25$ °C.



Electrical Characteristics Q1 - N-Channel (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	20	1	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current, T _J = +25°C	IDSS	1		1	μΑ	$V_{DS} = 20V$, $V_{GS} = 0V$
Gate-Source Leakage	Igss		1	±100	nA	$V_{GS} = \pm 12V$, $V_{DS} = 0V$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	VGS(TH)	0.4		1.2	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
			28	35		$V_{GS} = 10V, I_D = 6A$
Static Drain-Source On-Resistance	Descent		32	40	mΩ	$V_{GS} = 4.5V, I_{D} = 5A$
Static Dialit-Source Off-Resistance	RDS(ON)	_	43	60		$V_{GS} = 2.5V, I_{D} = 4A$
			65	91		$V_{GS} = 1.8V, I_D = 2A$
Diode Forward Voltage	VsD		0.7	1.2	V	$V_{GS} = 0V$, $I_{S} = 1A$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	Ciss	_	281			\/ 40\/\\ 0\/
Output Capacitance	Coss		50	_	pF	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	Crss		39	_		I = I.OIVII IZ
Total Gate Charge (V _{GS} = 4.5V)	Qg		3.6	_		\\ 45\\\\ 40\\
Gate-Source Charge	Qgs	_	0.5	_	nC	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_{D} = 6A$
Gate-Drain Charge	Qgd	_	0.9	_		ID = 6A
Turn-On Delay Time	td(ON)	_	2.0	_		
Turn-On Rise Time	t _R	_	4.9	_		$V_{DS} = 10V, V_{GS} = 4.5V,$
Turn-Off Delay Time	tD(OFF)	_	9.9	_	ns	$R_G = 6\Omega$, $I_D = 6A$
Turn-Off Fall Time	t _F	_	3.3	_		

Electrical Characteristics Q2 - P-Channel (@TA = +25°C, unless otherwise specified.)

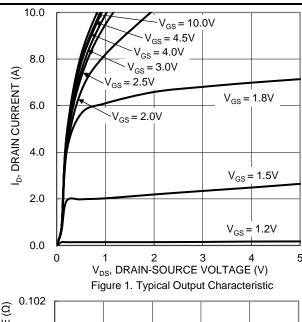
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)					•	•
Drain-Source Breakdown Voltage	BVDSS	-20	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$
Zero Gate Voltage Drain Current, T _J = +25°C	I _{DSS}	_	_	-1.0	μA	$V_{DS} = -20V, V_{GS} = 0V$
Gate-Source Leakage	Igss	_	_	±100	nA	$V_{GS} = \pm 8V$, $V_{DS} = 0V$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	Vgs(th)	-0.4	_	-1.2	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
Static Dunin Course On Benintanna	,		79	120	0	$V_{GS} = -4.5V$, $I_{D} = -2.8A$
Static Drain-Source On-Resistance	RDS(ON)	_	111	150	mΩ	$V_{GS} = -2.5V$, $I_{D} = -2.0A$
Diode Forward Voltage	VsD	_	-0.75	-1.2	V	$V_{GS} = 0V$, $I_{S} = -1A$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	Ciss	_	476	_		\/ 40\/ \/ 0\/
Output Capacitance	Coss	_	53	_	pF	$V_{DS} = -10V$, $V_{GS} = 0V$, $f = 1MHz$
Reverse Transfer Capacitance	Crss	_	45	_		1 – 11011 12
Total Gate Charge (VGS = -4.5V)	Qg	_	5.5	_		\\ 4 E\\ \\ 6\\
Gate-Source Charge	Qgs	_	0.9	_	nC	$V_{GS} = -4.5V, V_{DS} = -6V,$ $I_{D} = -2.8A$
Gate-Drain Charge	Qgd	_	1.8	_		ID = -2.6A
Turn-On Delay Time	t _{D(ON)}	_	5	_		
Turn-On Rise Time	tR	_	10	_	ns	$V_{GS} = -4.5V$, $V_{DS} = -6V$,
Turn-Off Delay Time	tD(OFF)	_	30	_	115	$R_G = 6\Omega$, $I_D = -1A$
Turn-Off Fall Time	tF	_	20	_		

Notes:

- 9. Short duration pulse test used to minimize self-heating effect.
- 10. Guaranteed by design. Not subject to product testing.



Q1 - N-Channel



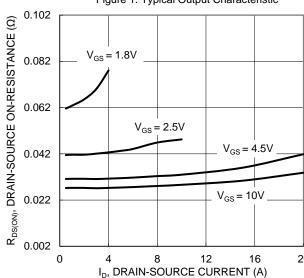


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

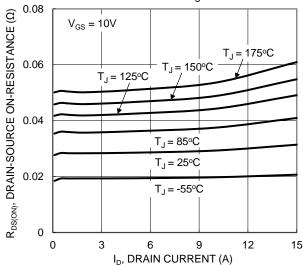
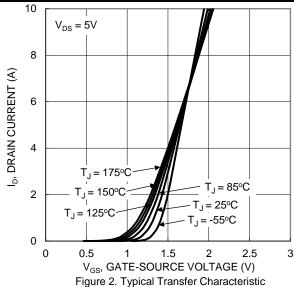
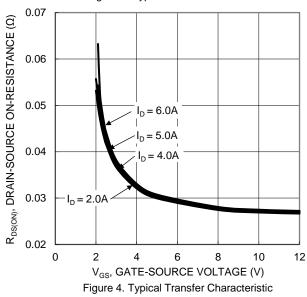


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature





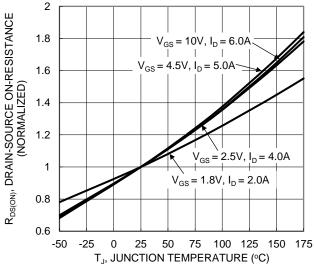


Figure 6. On-Resistance Variation with Junction Temperature



- N-Channel (continued)

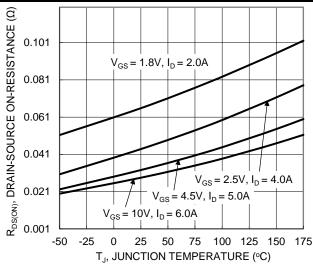
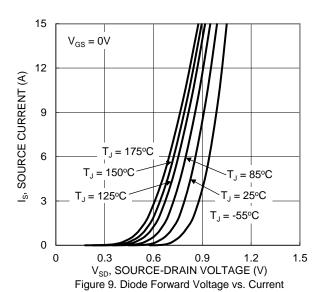
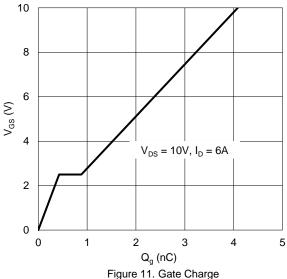


Figure 7. On-Resistance Variation with Junction Temperature





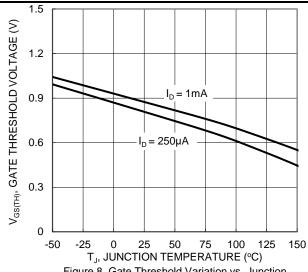
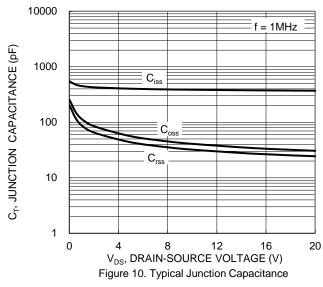


Figure 8. Gate Threshold Variation vs. Junction Temperature



100 R_{DS(ON)} Limited $P_W = 100 \mu s$ 1ms ID, DRAIN CURRENT (A) 10 $P_W = 10ms$ P_W = 100ms $T_A = 25^{\circ}C$ 0.1 Single Pulse DUT on 1*MRP Board $V_{GS} = 10V$ 0.01 0.1 1 10 100 V_{DS}, DRAIN-SOURCE VOLTAGE (V) Figure 12. SOA, Safe Operation Area



Q1 - N-Channel (continued)

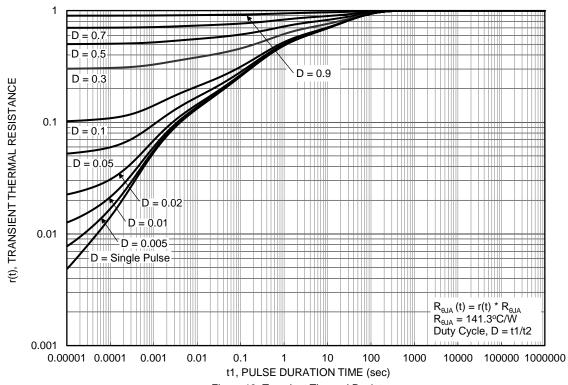
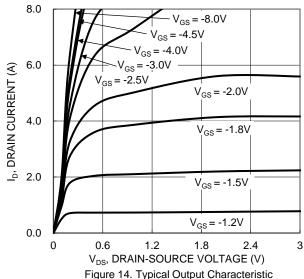


Figure 13. Transient Thermal Resistance



Q2 - P-Channel



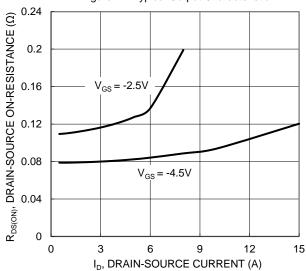


Figure 16. Typical On-Resistance vs. Drain Current and Gate Voltage

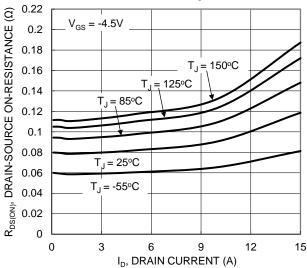


Figure 18. Typical On-Resistance vs. Drain Current and Junction Temperature

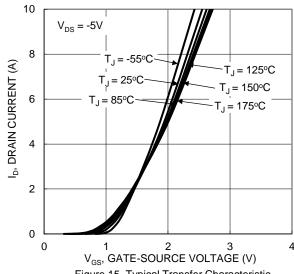


Figure 15. Typical Transfer Characteristic

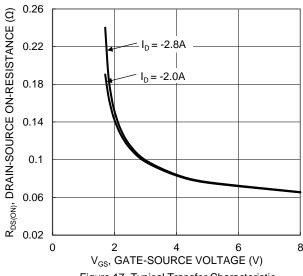


Figure 17. Typical Transfer Characteristic

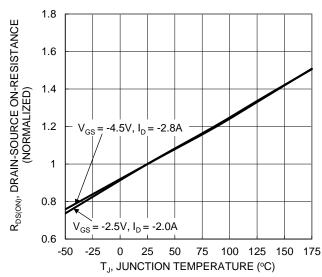


Figure 19. On-Resistance Variation with Junction Temperature



Q2 - P-Channel (continued)

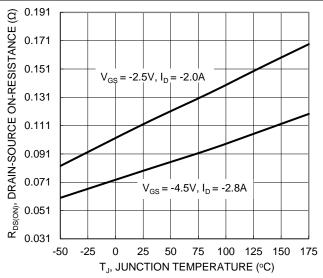


Figure 20. On-Resistance Variation with Junction Temperature

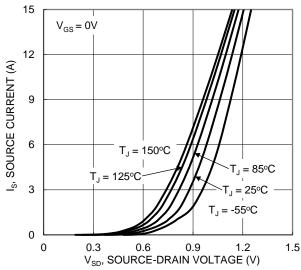


Figure 22. Diode Forward Voltage vs. Current

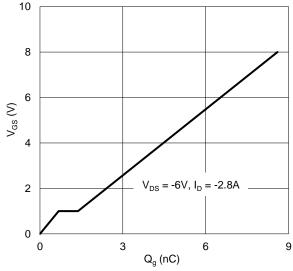


Figure 24. Gate Charge

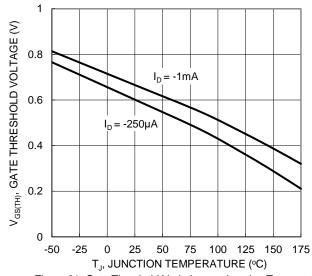
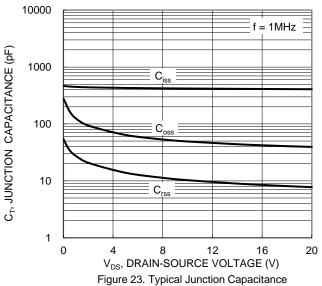
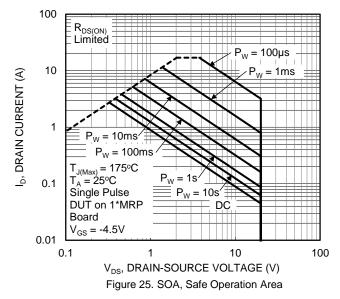


Figure 21. Gate Threshold Variation vs. Junction Temperature







Q2 - P-Channel (continued)

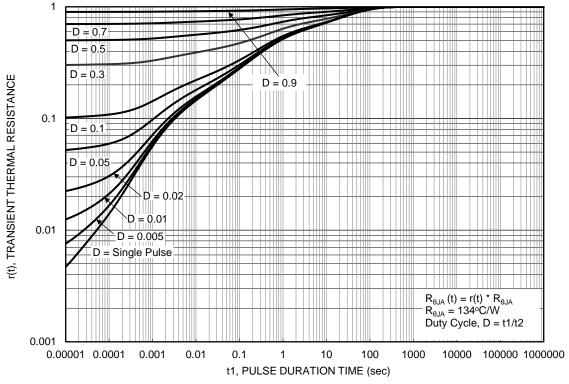


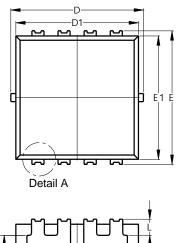
Figure 26. Transient Thermal Resistance

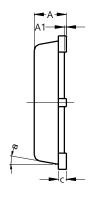


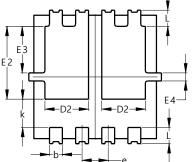
Package Outline Dimensions

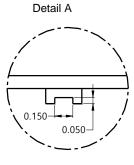
Please see http://www.diodes.com/package-outlines.html for the latest version.

POWERDI®3333-8/SWP (Type UXD)







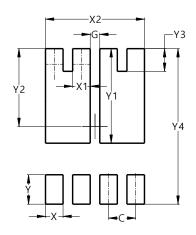


POWERDI®3333-8/SWP						
(Type UXD)						
Dim	Min	Max	Тур			
Α	0.75	0.85	0.80			
A1	0.00	0.05				
b	0.25	0.40	0.32			
С	0.10	0.25	0.15			
D	3.20	3.40	3.30			
D1	2.95	3.15	3.05			
D2	1.00	1.20	1.10			
Е	3.20	3.40	3.30			
E1	2.95	3.15	3.05			
E2	1.60	2.00	1.80			
E3	0.95	1.35	1.15			
E4	0.10	0.30	0.20			
е	_	_	0.65			
L	0.30	0.50	0.40			
k	0.50	0.90	0.70			
а	0°	12°	10°			
All Dimensions in mm						

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

POWERDI®3333-8/SWP (Type UXD)



Dimensions	Value (in mm)
С	0.650
G	0.230
X	0.420
X1	0.420
X2	2.370
Υ	0.700
Y1	2.250
Y2	1.850
Y3	0.540
Y4	3.700



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