60V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
Q1	60V	1.7Ω @ V_{GS} = 10V	510mA
		3Ω @ V_{GS} = 4.5V	393mA
Q2	-60V	8Ω @ V_{GS} = -5V	-244mA

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Ultra-Small Surface-Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.**
  https://www.diodes.com/quality/product-definitions/
- **An automotive-compliant part is available under a separate datasheet (DMC62D3SVQ)**

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

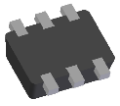
- General-purpose interfacing switches
- Power-management functions
- Analog switches

Mechanical Data

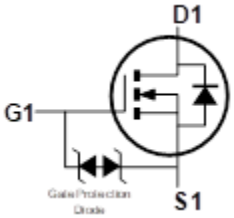
- Package: SOT563
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish—Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.027 grams (Approximate)

SOT563

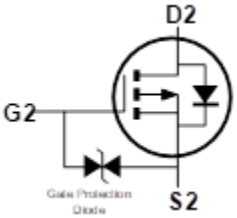
Top View



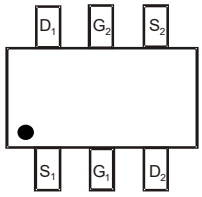
Bottom View



Q1 N-Channel



Q2 P-Channel



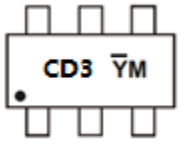
Top View
Internal Schematic

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMC62D3SV-7	SOT563	3,000	Tape & Reel
DMC62D3SV-13	SOT563	10,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



CD3 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: M = 2025)
M = Month (ex: 9 = September)

Date Code Key

Year	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Code	M	N	P	R	S	T	U	V	W	X	Y	Z

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings N-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	510 408	mA
Maximum Body Diode Forward Current (Note 5)			I_S	510	mA
Pulsed Drain Current (Note 5)			I_{DM}	1	A
Pulsed Source Current (Note 5)			I_{SM}	1	A

Maximum Ratings P-CHANNEL – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = -5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-244 -195	mA
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-244	mA
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-1	A
Pulsed Source Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	-1	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)		P_D	0.5	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	241	°C/W
Total Power Dissipation (Note 5)		P_D	0.8	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	140	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Electrical Characteristics N-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = 60V, V_{GS} = 0
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±20V, V_{DS} = 0
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	1.0	1.7	Ω	V_{GS} = 10V, I_D = 200mA
		—	1.2	3		V_{GS} = 4.5V, I_D = 200mA
Diode Forward Voltage	V_{SD}	—	0.85	1.4	V	V_{GS} = 0, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	41	—	pF	V_{DS} = 30V, V_{GS} = 0 f = 1.0MHz
Output Capacitance	C_{oss}	—	4.5	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	2.7	—	pF	
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	0.51	—	nC	V_{DS} = 15V, I_D = 200mA
Total Gate Charge (V_{GS} = 10V)	Q_g	—	1.04	—	nC	
Gate-Source Charge	Q_{gs}	—	0.16	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.18	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	6.9	—	ns	V_{DD} = 30V, V_{GS} = 10V R_g = 150Ω, I_D = 200mA
Turn-On Rise Time	t_R	—	5.8	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	37.8	—	ns	
Turn-Off Fall Time	t_F	—	14.3	—	ns	
Reverse-Recovery Time	t_{RR}	—	19	—	ns	I_F = 1A, di/dt = 100A/μs
Reverse-Recovery Charge	Q_{RR}	—	9	—	nC	I_F = 1A, di/dt = 100A/μs

Electrical Characteristics P-CHANNEL – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-60	—	—	V	V_{GS} = 0, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	μA	V_{DS} = -60V, V_{GS} = 0
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±20V, V_{DS} = 0
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.8	—	-2.1	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	2	8	Ω	V_{GS} = -5V, I_D = -100mA
Diode Forward Voltage	V_{SD}	—	-0.8	-1.5	V	V_{GS} = 0, I_S = -100mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	42	—	pF	V_{DS} = -30V, V_{GS} = 0 f = 1.0MHz
Output Capacitance	C_{oss}	—	10	—		
Reverse Transfer Capacitance	C_{rss}	—	6	—		
Gate Resistance	R_g	—	225	—	Ω	V_{DS} = 0, V_{GS} = 0, f = 1MHz
Total Gate Charge	Q_g	—	0.6	—	nC	V_{GS} = -5V, V_{DS} = -30V I_D = -100mA
Gate-Source Charge	Q_{gs}	—	0.1	—		
Gate-Drain Charge	Q_{gd}	—	0.2	—		
Turn-On Delay Time	$t_{D(ON)}$	—	11	—	ns	V_{GS} = -5V, V_{DS} = -30V R_g = 50Ω, I_D = -100mA
Turn-On Rise Time	t_R	—	16	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	30	—		
Turn-Off Fall Time	t_F	—	30	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

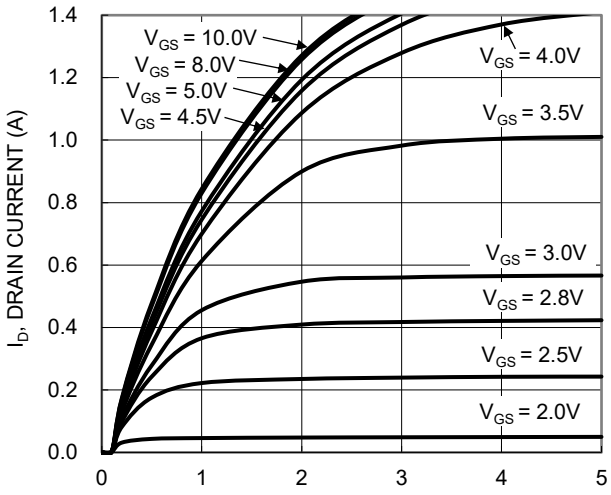


Figure 1. Typical Output Characteristic (Q1)

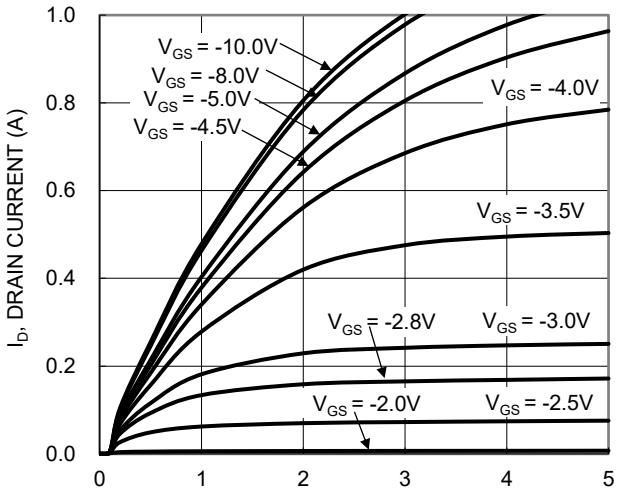


Figure 2. Typical Output Characteristic (Q2)

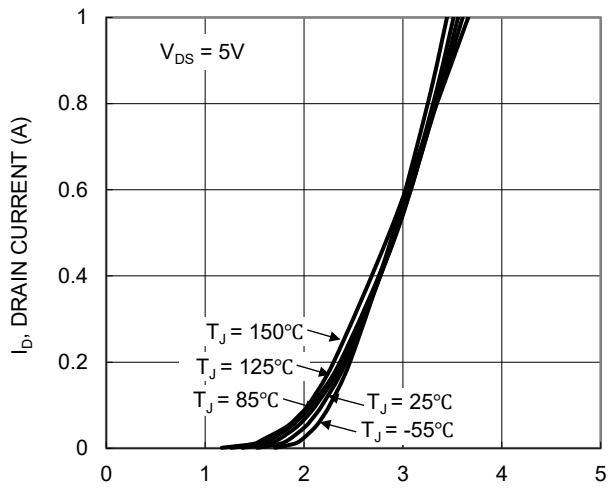


Figure 3. Typical Transfer Characteristic (Q1)

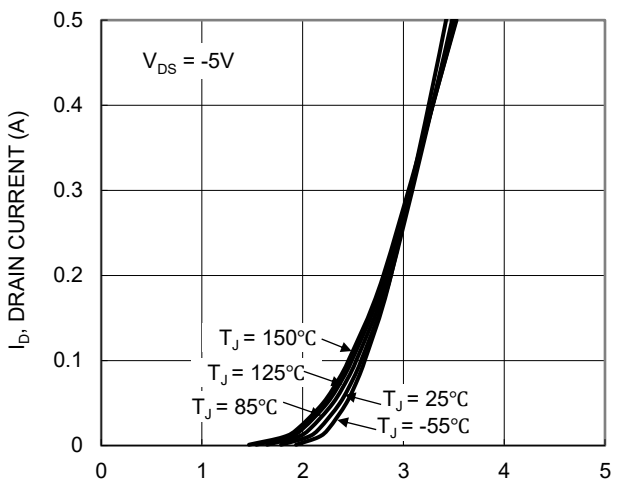


Figure 4. Typical Transfer Characteristic (Q2)

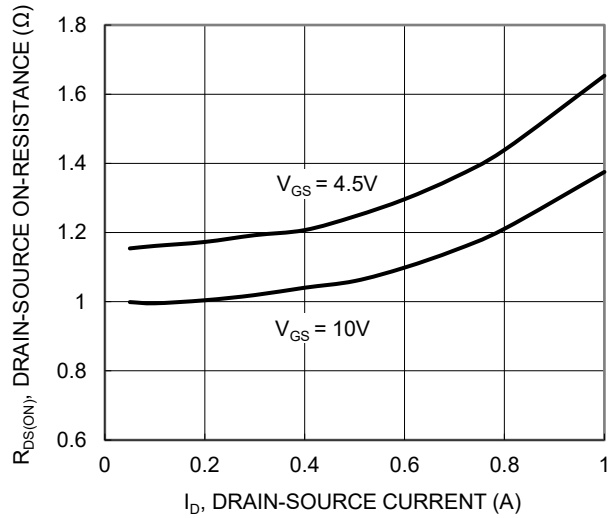


Figure 5. Typical On-Resistance vs. Drain Current and Gate Voltage (Q1)

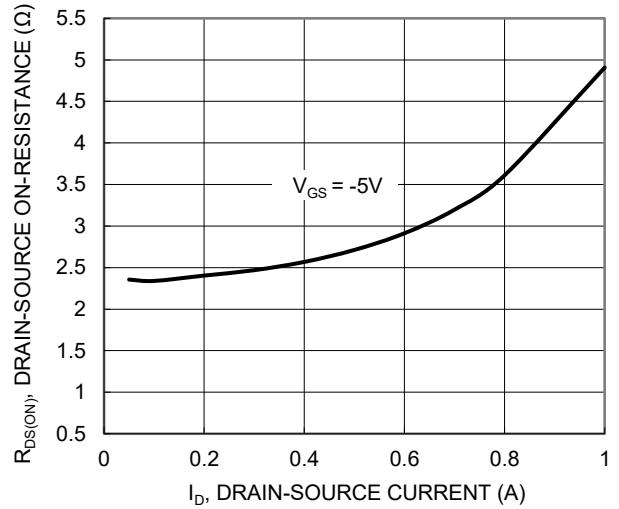


Figure 6. Typical On-Resistance vs. Drain Current and Gate Voltage (Q2)

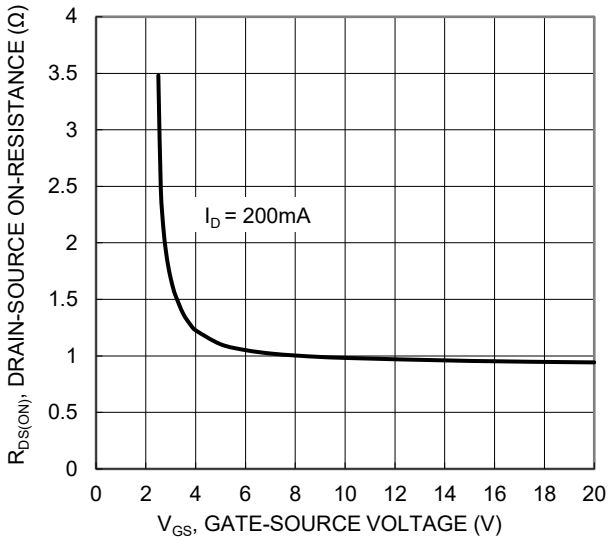


Figure 7. Typical Transfer Characteristic (Q1)

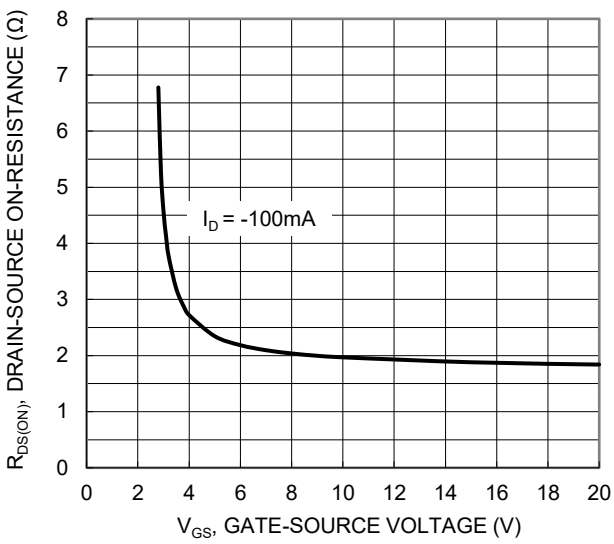


Figure 8. Typical Transfer Characteristic (Q2)

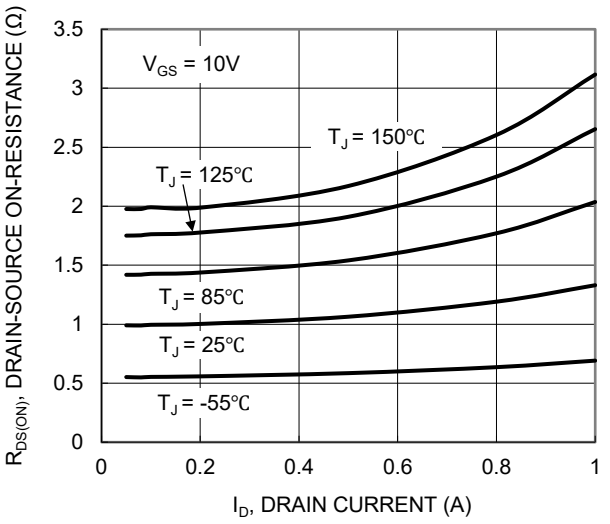


Figure 9. Typical On-Resistance vs. Drain Current and Junction Temperature (Q1)

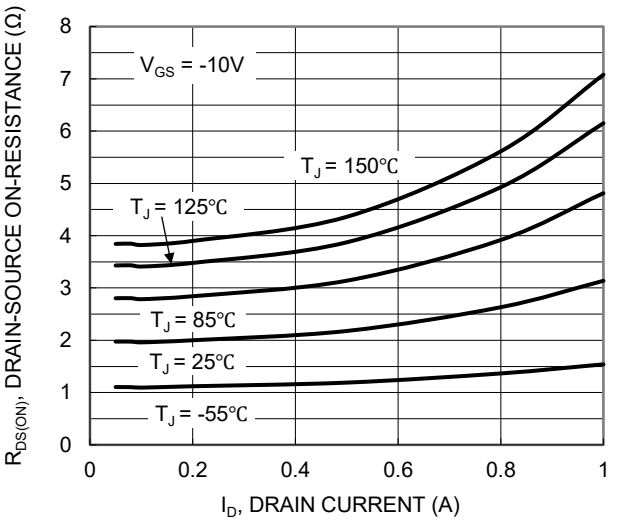


Figure 10. Typical On-Resistance vs. Drain Current and Junction Temperature (Q2)

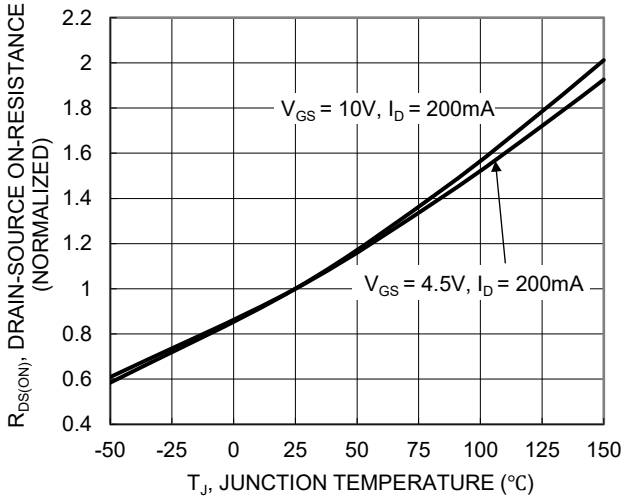


Figure 11. On-Resistance Variation with Junction Temperature (Q1)

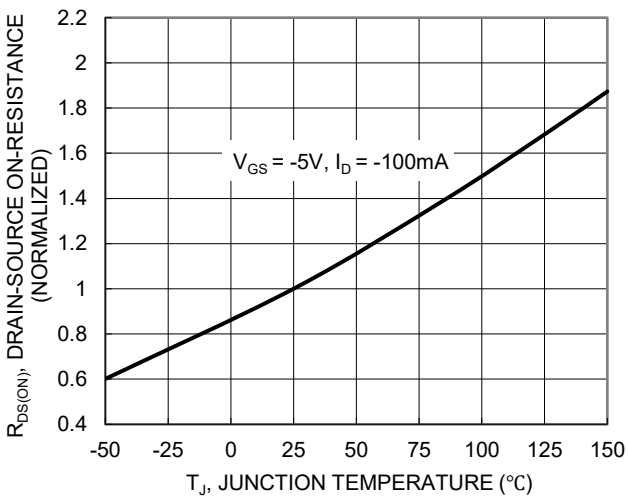


Figure 12. On-Resistance Variation with Junction Temperature (Q2)

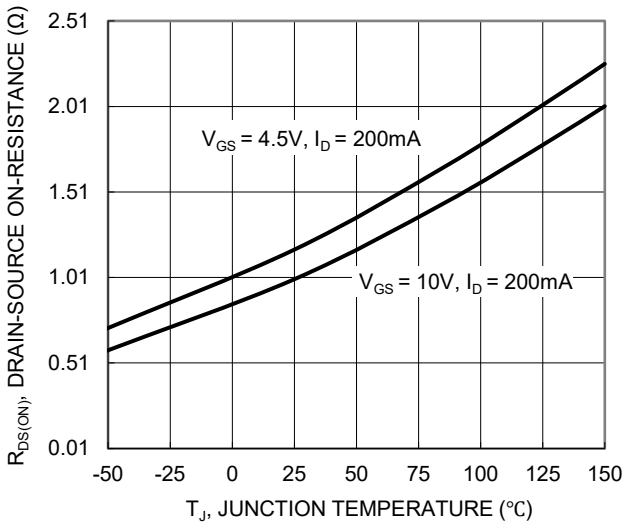


Figure 13. On-Resistance Variation with Junction Temperature (Q1)

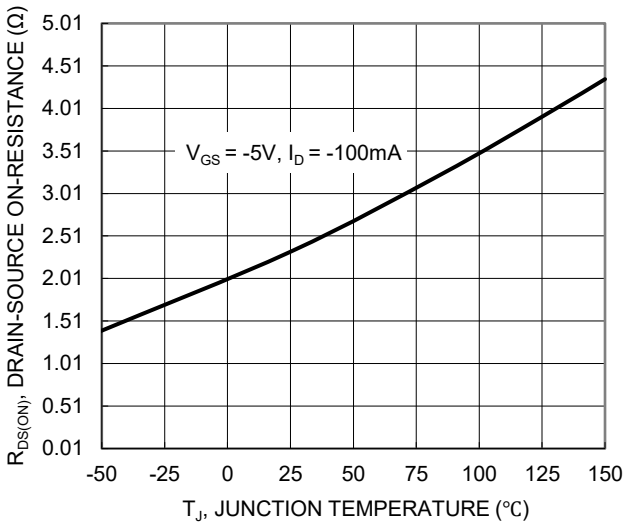


Figure 14. On-Resistance Variation with Junction Temperature (Q2)

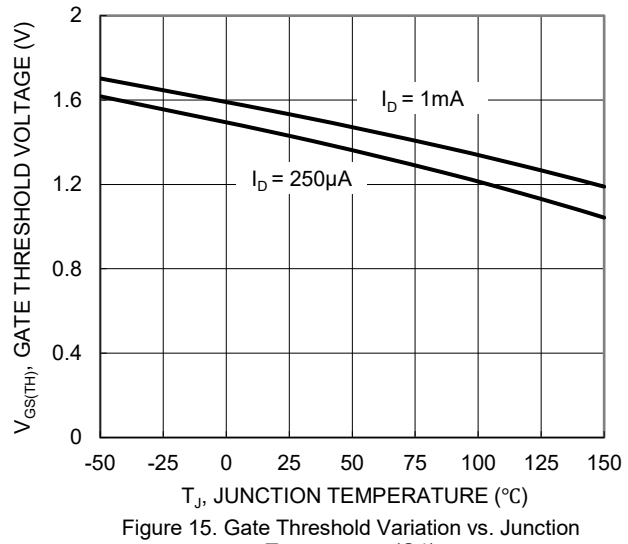


Figure 15. Gate Threshold Variation vs. Junction Temperature (Q1)

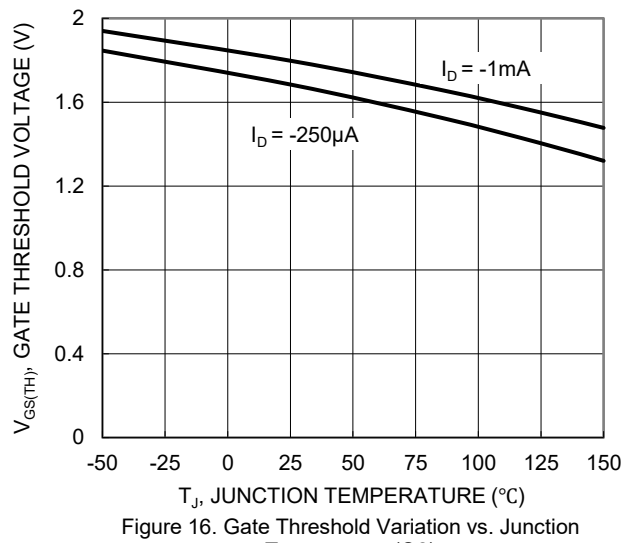


Figure 16. Gate Threshold Variation vs. Junction Temperature (Q2)

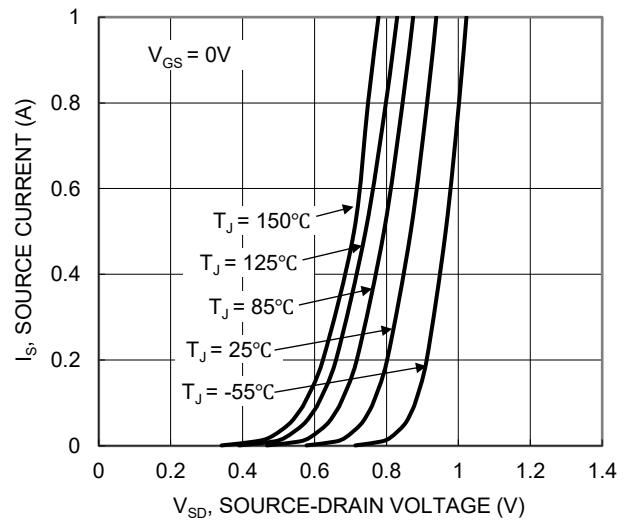


Figure 17. Diode Forward Voltage vs. Current (Q1)

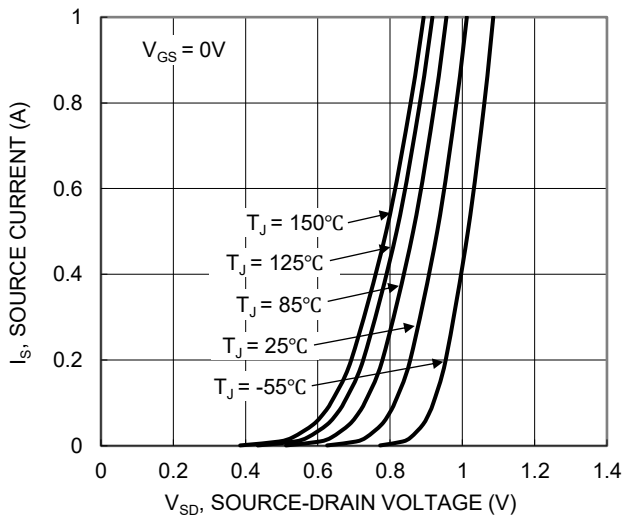


Figure 18. Diode Forward Voltage vs. Current (Q2)

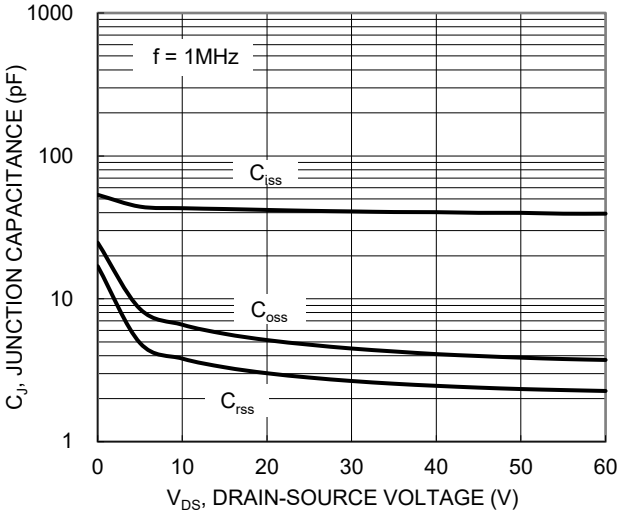


Figure 19. Typical Junction Capacitance (Q1)

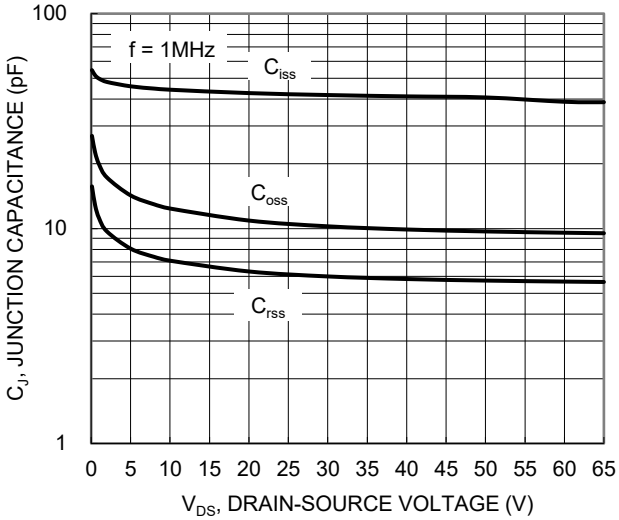


Figure 20. Typical Junction Capacitance (Q2)

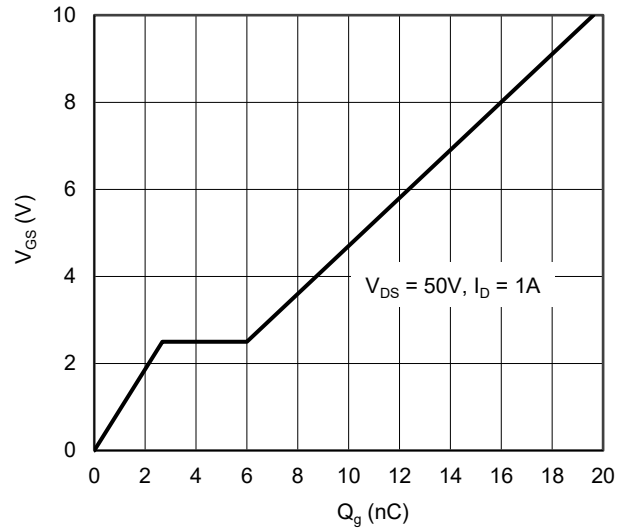


Figure 21. Gate Charge (Q1)

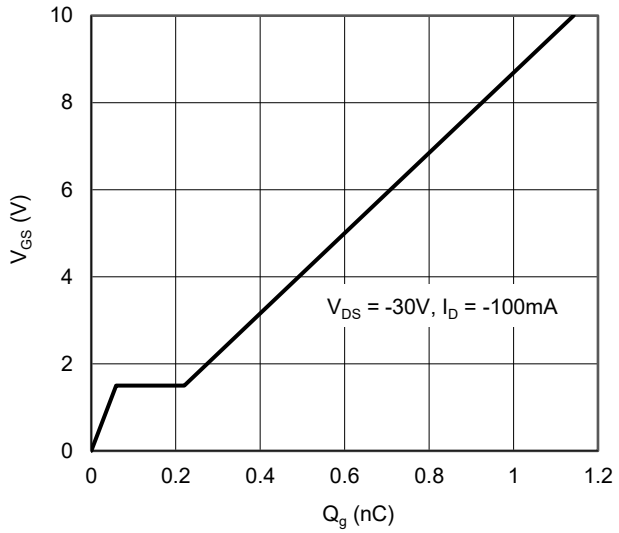


Figure 22. Gate Charge (Q2)

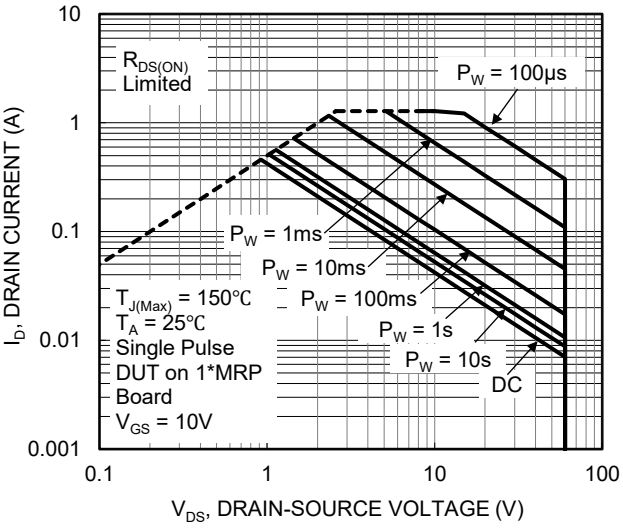


Figure 23. SOA, Safe Operation Area (Q1)

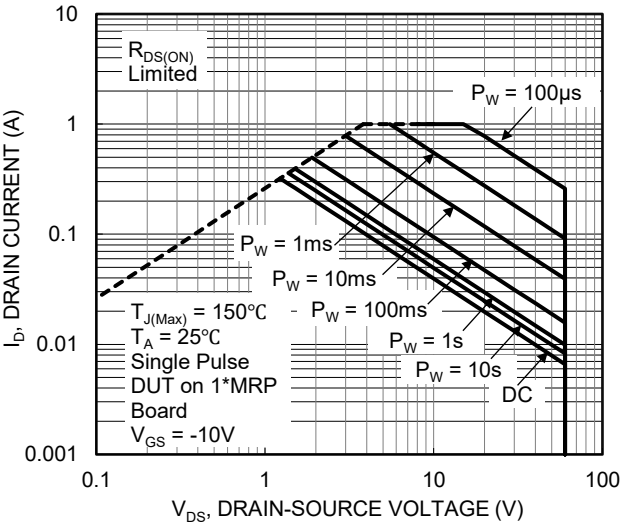


Figure 24. SOA, Safe Operation Area (Q2)

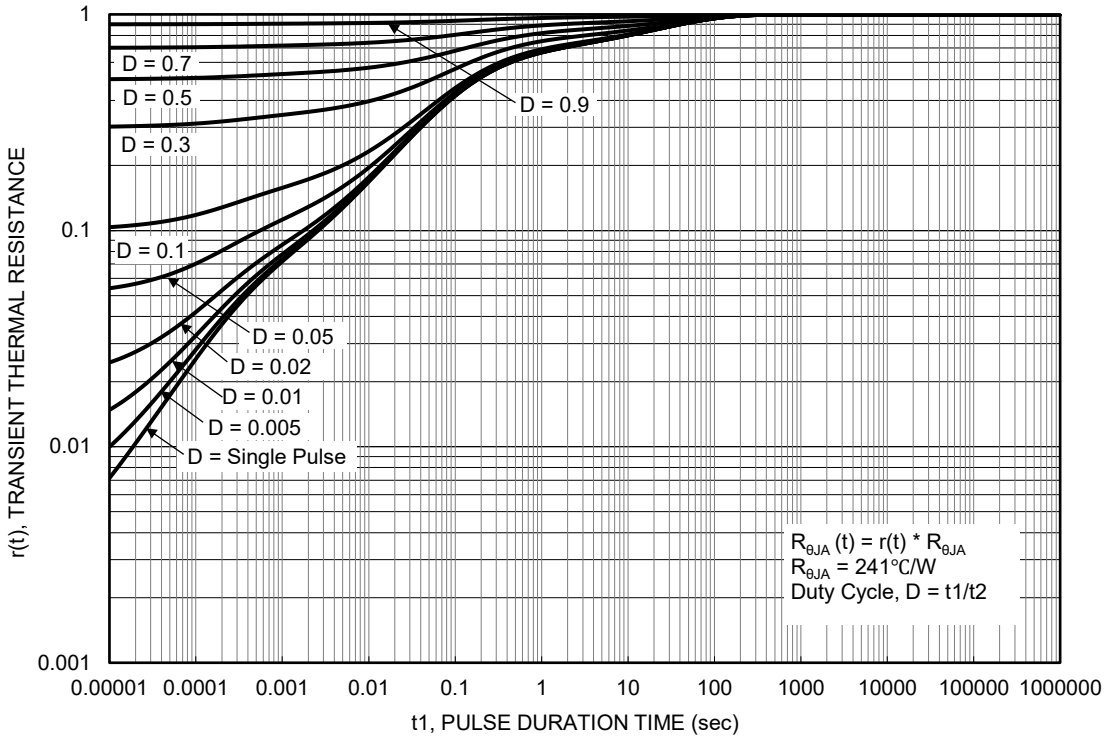
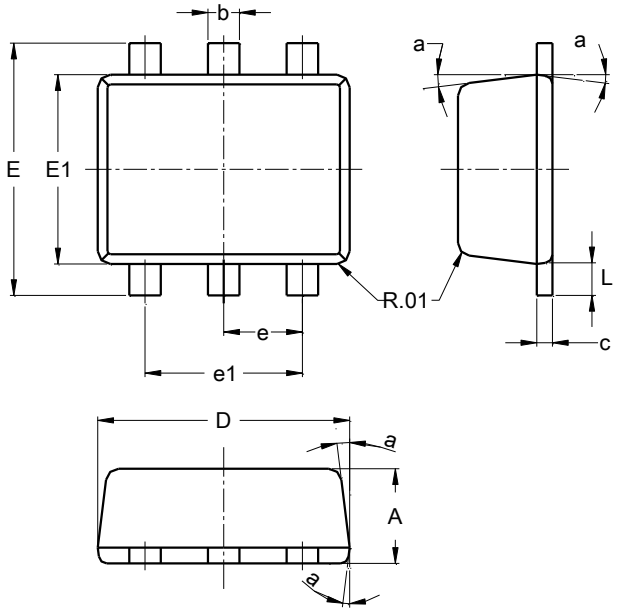


Figure 25. Transient Thermal Resistance (Q1/Q2)

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563

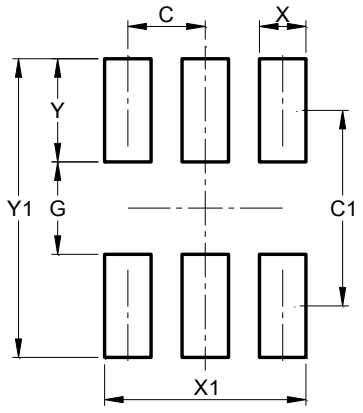


SOT563			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.60	--
b	0.15	0.30	0.20
c	0.10	0.18	0.11
D	1.50	1.70	1.60
E	1.55	1.70	1.60
E1	1.10	1.25	1.20
e	--	--	0.50
e1	0.90	1.10	1.00
L	0.10	0.30	0.20
a	8°	9°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563



Dimensions	Value (in mm)
C	0.500
C1	1.270
G	0.600
X	0.300
X1	1.300
Y	0.670
Y1	1.940

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