

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25^\circ C$
-30V	7.5m Ω @ $V_{GS} = -10V$	-12A
	10.2m Ω @ $V_{GS} = -4.5V$	-10A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

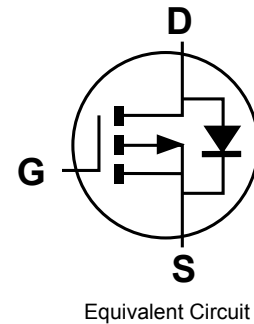
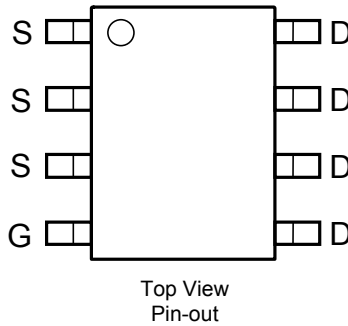
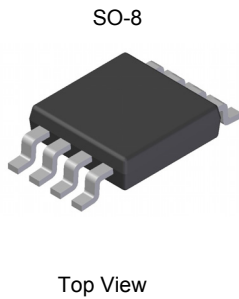
- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS compliant (Note 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram below
- Terminals: Finish — Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 $\text{\textcircled{3}}$
- Weight: 0.074 grams (approximate)

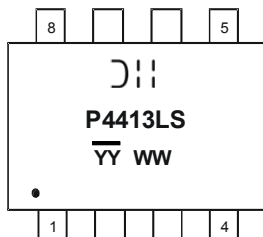


Ordering Information (Note 4)

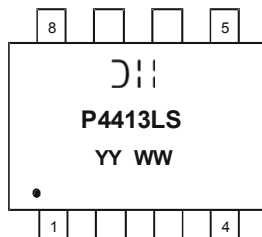
Part Number	Case	Packaging
DMG4413LSS-13	SO-8	2500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

- ⌋;⌋ = Manufacturer's Marking
- P4413LS = Product Type Marking Code
- YYWW = Date Code Marking
- YY or YY = Year (ex: 13 = 2013)
- WW = Week (01 - 53)
- YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
- YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = -10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-12 -10	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-22 -17	A
Continuous Drain Current (Note 6) $V_{GS} = -4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-10 -8	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-18 -14	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	-100	A
Maximum Body Diode continuous Current			I_S	-4	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	1.7	W
	$T_A = +70^\circ\text{C}$		1.1	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	74	$^\circ\text{C/W}$
	$t < 10\text{s}$		22	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	2.2	W
	$T_A = +70^\circ\text{C}$		1.4	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	56	$^\circ\text{C/W}$
	$t < 10\text{s}$		17	
Thermal Resistance, Junction to Case (Note 6)	Steady State	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 1	μA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-1.1	1.6	-2.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	6.3	7.5	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -13\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -10\text{A}$
		—	7.9	10.2		
Forward Transconductance	g_{fs}	—	26	—	S	$V_{DS} = -15\text{V}, I_D = -13\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.7	-1.0	V	$V_{GS} = 0\text{V}, I_S = -2.7\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	4965	—	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	1487	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	711	—	pF	
Gate Resistance	R_G	—	7.3	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
SWITCHING CHARACTERISTICS (Note 8)						
Total Gate Charge	Q_G	—	46	—	nC	$V_{DS} = -15\text{V}, V_{GS} = -5\text{V}$ $I_D = -13\text{A}$
Gate-Source Charge	Q_{GS}	—	17	—		
Gate-Drain Charge	Q_{GD}	—	16	—		
Turn-On Delay Time	$t_{d(on)}$	—	15	—	ns	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V},$ $I_D = -1\text{A}, R_G = 6.0\Omega$
Rise Time	t_r	—	9	—		
Turn-Off Delay Time	$t_{d(off)}$	—	160	—		
Fall Time	t_f	—	66	—		

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

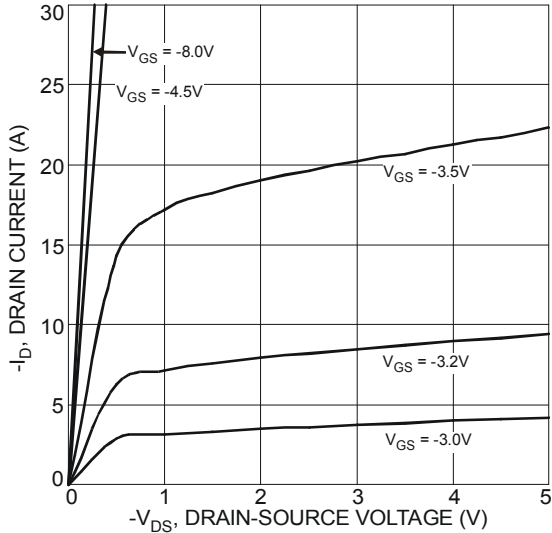


Fig. 1 Typical Output Characteristic

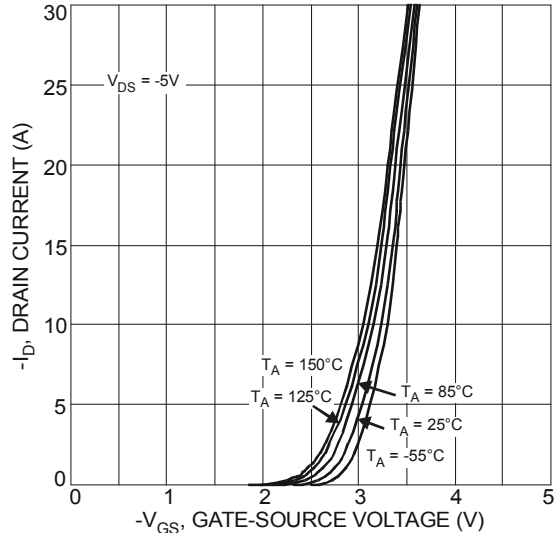


Fig. 2 Typical Transfer Characteristic

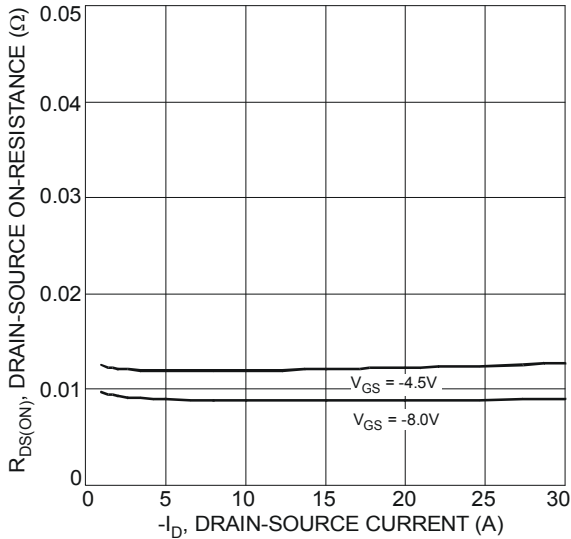


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

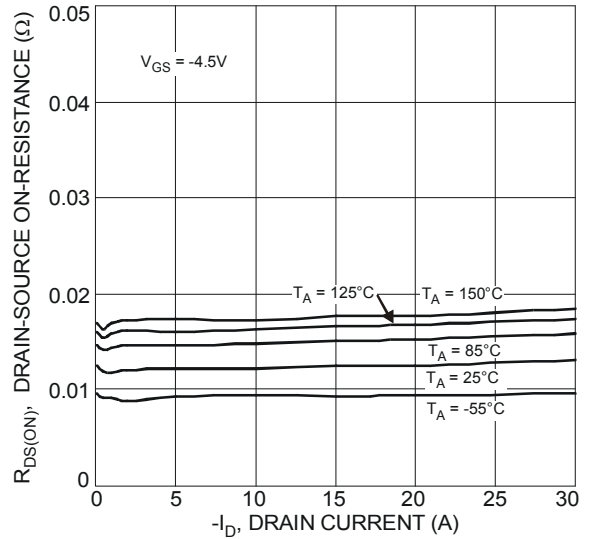


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

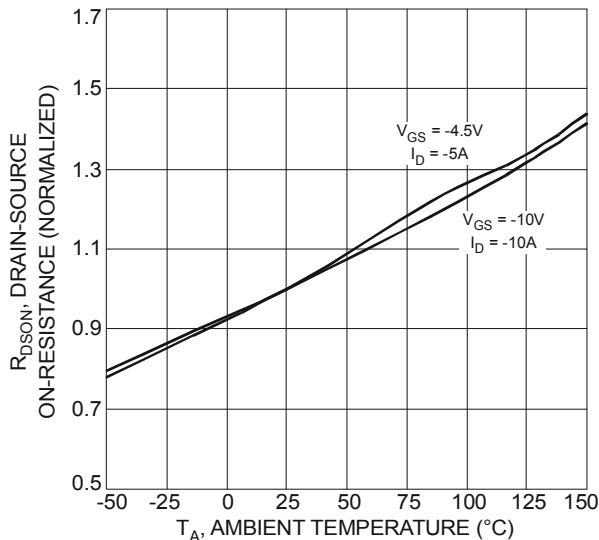


Fig. 5 On-Resistance Variation with Temperature

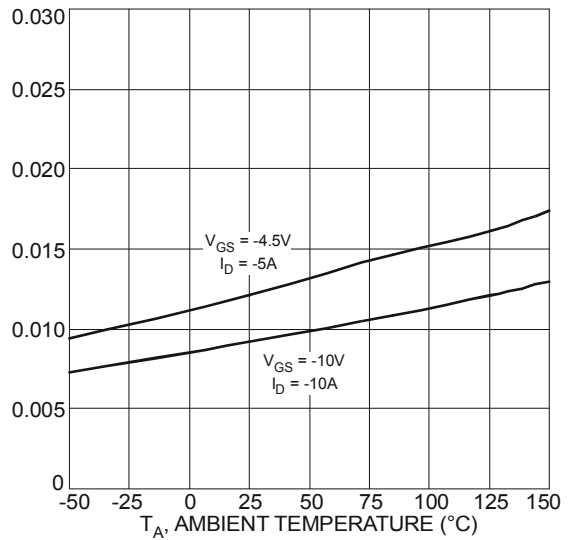


Fig. 6 On-Resistance Variation with Temperature

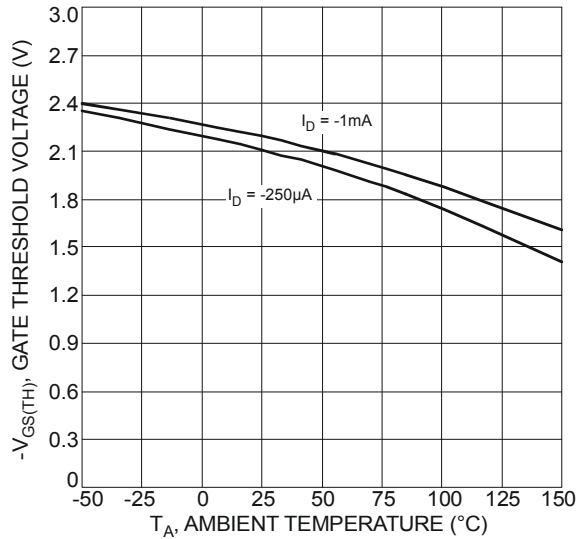


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

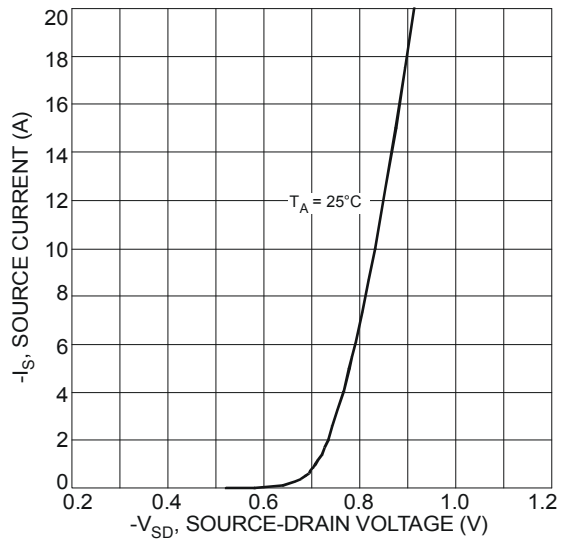


Fig. 8 Diode Forward Voltage vs. Current

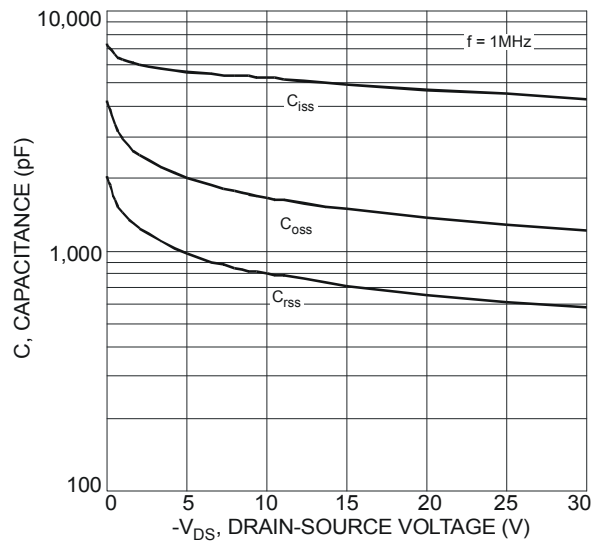
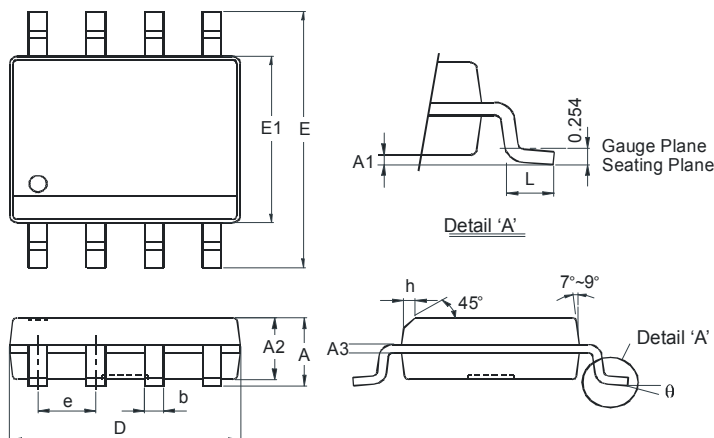


Fig. 9 Typical Total Capacitance

Package Outline Dimensions

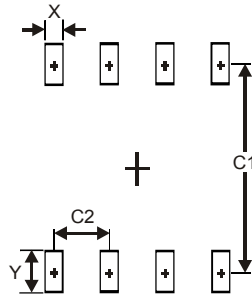
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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