NOT RECOMMENDED FOR NEW DESIGN
USE DMP2040USS

Lead-free Green

DMP2066LSD

DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ max	I_D T_A = +25°C
-20V	40mΩ @ V_{GS} = -4.5V	-5.8A
	70mΩ @ V_{GS} = -2.5V	-4.4A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

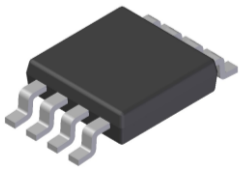
Features

- Dual P-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

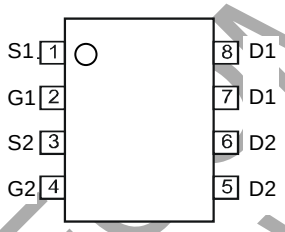
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections Indicator: See Diagram
- Terminals: Finish - Matte Tin Annealed over Copper Lead Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.072 grams (Approximate)

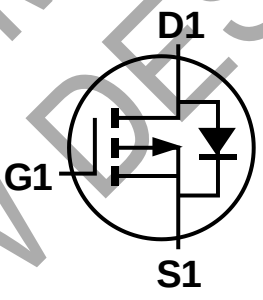
SO-8



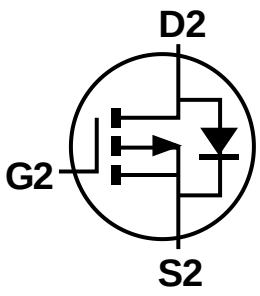
Top View



Top View
Internal Schematic



P-Channel MOSFET



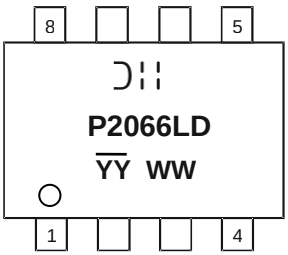
P-Channel MOSFET

Ordering Information (Note 4)

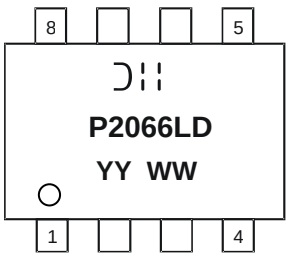
Part Number	Case	Packaging
DMP2066LSD-13	SO-8	2500/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

= Manufacturer's Marking
P2066LD = Product Type Marking Code
YYWW = Date Code Marking
YY or YY = Year (ex: 18 = 2018)
WW = Week (01 to 53)
YY = Date Code Marking for SAT (Shanghai Assembly/ Test Site)
YY = Date Code Marking for CAT (Chengdu Assembly/ Test Site)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±12	V
Drain Current (Note 5)	Steady State	T_A = +25°C T_A = +70°C	I_D	-5.8 -4.6	A
Pulsed Drain Current (Note 6)			I_{DM}	-20	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.0	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	62.5	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.6	-0.94	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	— —	29 55	40 70	mΩ	V_{GS} = -4.5V, I_D = -4.6A V_{GS} = -2.5V, I_D = -3.8A
Forward Transconductance	g_{fs}	—	9	—	S	V_{DS} = -10V, I_D = -4.6A
Diode Forward Voltage (Note 7)	V_{SD}	-0.5	-0.72	-1.4	V	V_{GS} = 0V, I_S = -2.1A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	820	—	pF	V_{DS} = -15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	200	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	160	—	pF	
Gate Resistance	R_G	—	2.5	—	Ω	V_{DS} = 0V, V_{GS} = 0V f = 1.0MHz
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	—	10.1	—	nC	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -5.9A
Gate-Source Charge	Q_{GS}	—	1.5	—		
Gate-Drain Charge	Q_{GD}	—	4.3	—		
Turn-On Delay Time	$t_{D(ON)}$	—	4.4	—	ns	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -1A, R_G = 6.0Ω
Rise Time	t_R	—	9.9	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	28.0	—		
Fall Time	t_F	—	23.4	—		

Notes: 5. Device mounted on 2 oz. 1" x 1" Copper pads on 2" x 2" FR-4 PCB.
6. Pulse width ≤10µS, Duty Cycle ≤1%.
7. Short duration pulse test used to minimize self-heating effect.

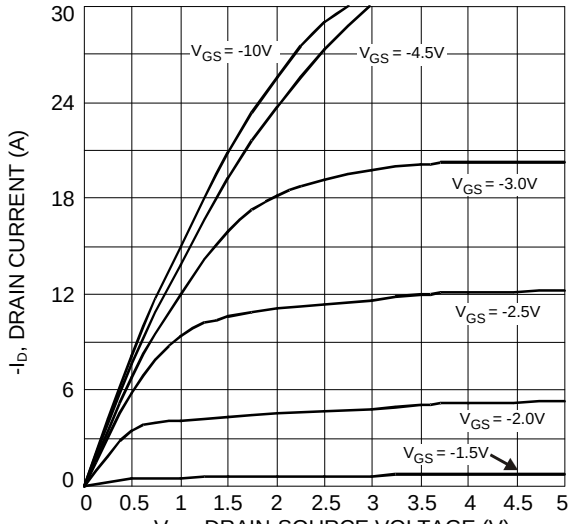


Fig. 1 Typical Output Characteristic

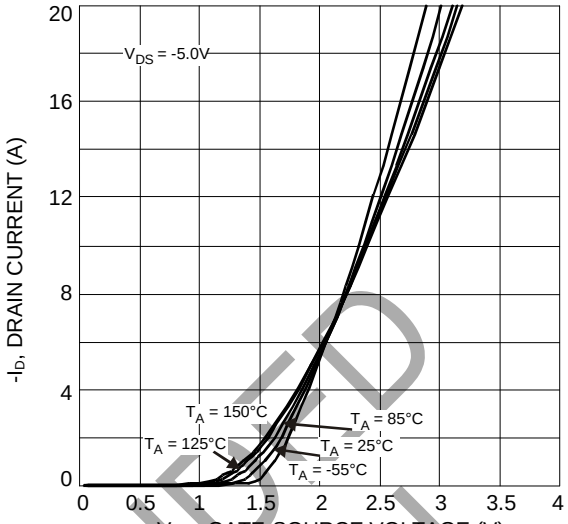


Fig. 2 Typical Transfer Characteristic

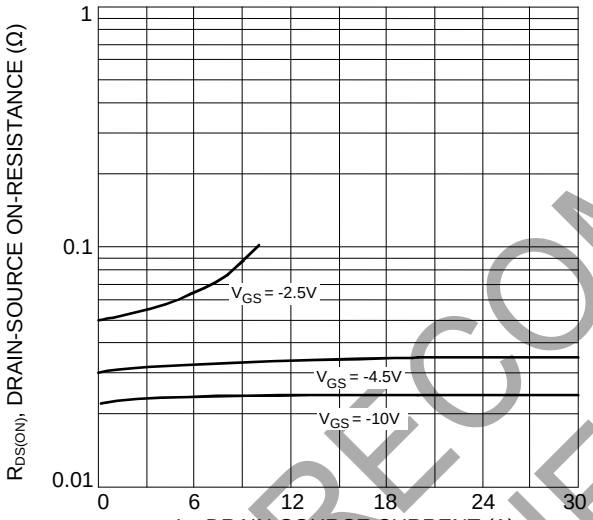


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

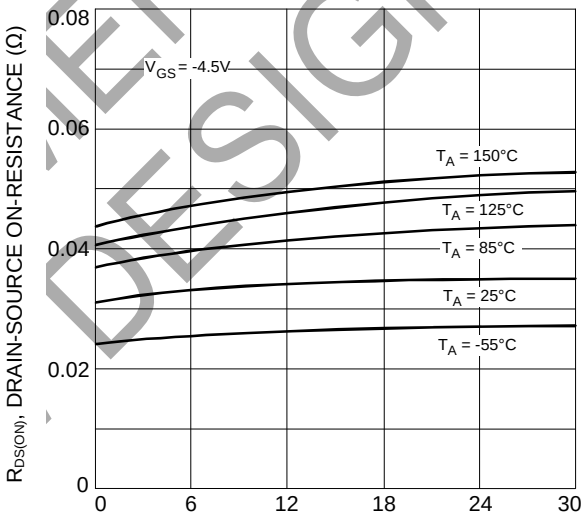


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

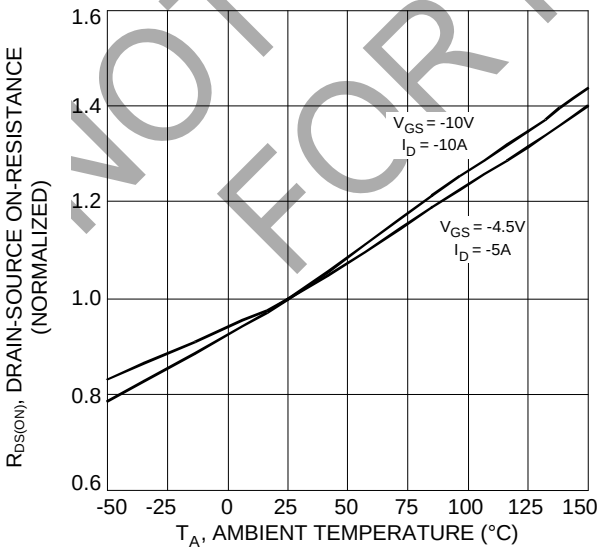


Fig. 5 Normalized On-Resistance vs. Ambient Temperature

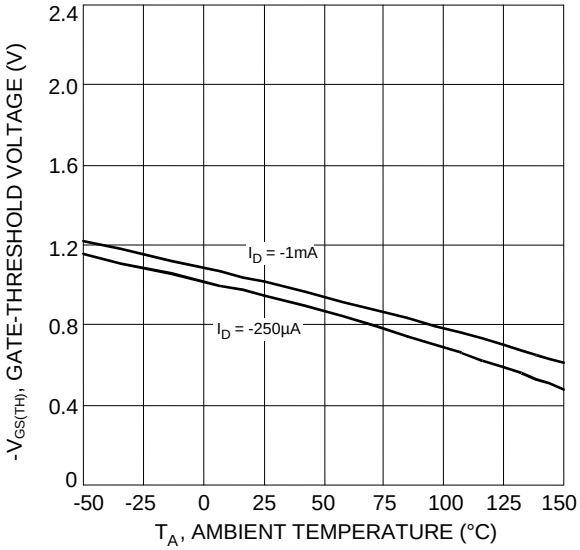


Fig. 6 Gate Threshold Variation vs. Ambient Temperature

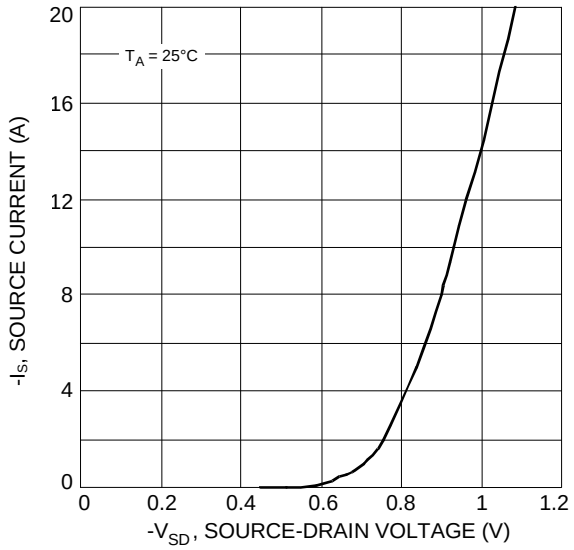


Fig. 7 Diode Forward Voltage vs. Current

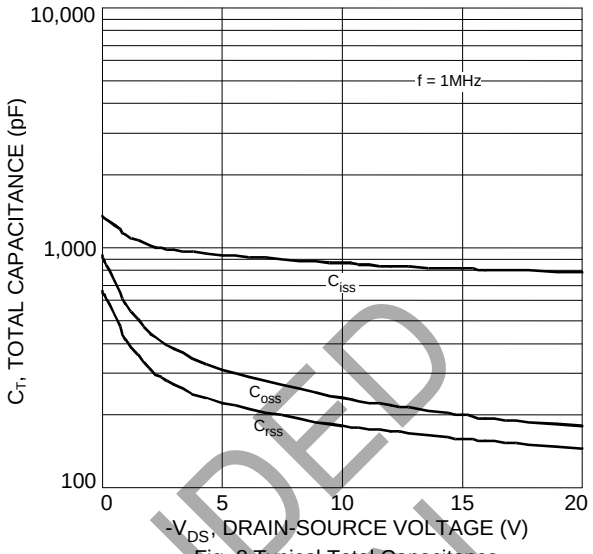


Fig. 8 Typical Total Capacitance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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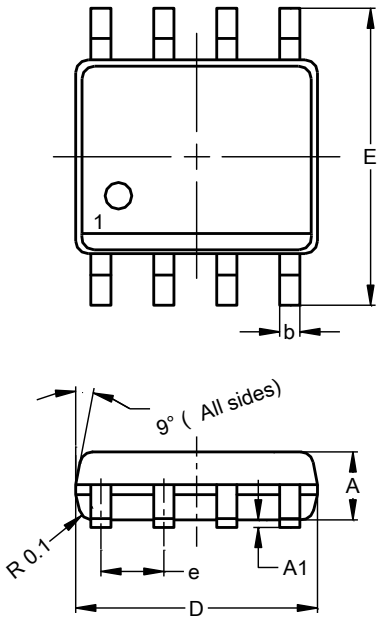

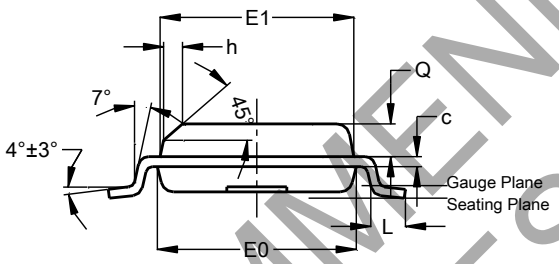

SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

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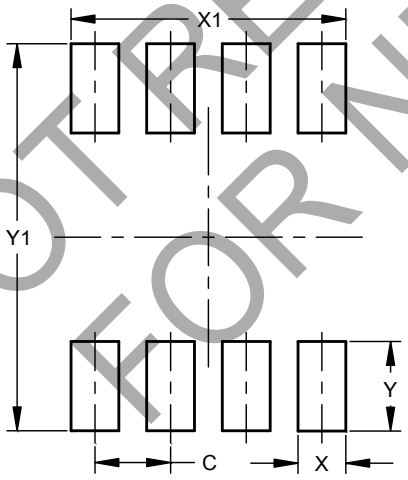

Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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