



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
-20V	$45m\Omega$ @ $V_{GS} = -4.5V$	-4.5A
-200	65mΩ @ V _{GS} = -2.5V	-3.8A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$), and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Power Management Functions

Features and Benefits

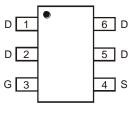
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

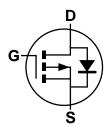
- Case: SOT26
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 (§3)
- Weight: 0.015 grams (Approximate)



Top View



Top View Pin-Out



Equivalent Circuit

Ordering Information (Note 4)

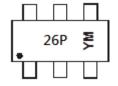
Part Number	Case	Packaging
DMP2066LVT-7	SOT26	3,000/Tape & Reel
DMP2066LVT-13	SOT26	10,000/Tape & Reel

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.

- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds4. For packaging details, go to our website at http://www.diodes.com.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

SOT26



26P = Product Type Marking Code YM = Date Code Marking for SAT (Shanghai Assembly/ Test site) Y or \overline{Y} = Year (ex: A = 2013) M = Month (ex: 9 = September)

Shanghai A/T Site

Date Code Kev

	Year	201	1	2012		2013	20	14	2015		2016	2	2017
	Code	Υ		Z		Α	I	3	С		D		Е
Ī	Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
	Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	-20	V	
Gate-Source Voltage	V_{GSS}	±8	V	
Drain Current (Note 5) Continuous $T_A = +25$ °C $T_A = +70$ °C		I _D	-4.5 -3.7	А
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I _{DM}	-20	A	
Body-Diode Continuous Current (Note 5)	Is	-2.0	Α	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

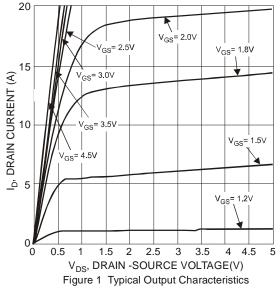
Characteristic	Symbol	Value	Units		
Total Power Dissipation (Note 5)	P_{D}	1.2	W		
Thermal Desistance Lunction to Ambient (Note 5)	Steady State	Б	100	°C/W	
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{\theta JA}$	74	C/VV	
Total Power Dissipation (Note 6)		P_{D}	1.8	W	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Б	70	°C/W	
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{\theta JA}$	46	C/VV	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C	

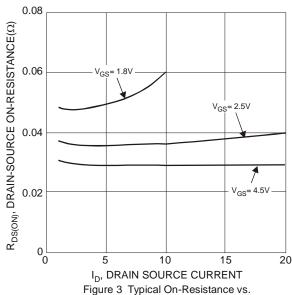
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

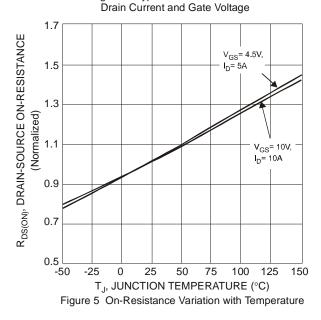
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
STATIC PARAMETERS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	-20		_	V	$I_D = -250\mu A, V_{GS} = 0V$	
Zero Gate Voltage Drain Current	I _{DSS}		_	-1	μA	V _{DS} = -16V, V _{GS} = 0V	
@ T _J = +55°C (Note 8)	.033			-10	μ., .	$V_{DS} = -16V, V_{GS} = 0V$	
Zero Gate Voltage Drain Current @T _J = +150°C (Note 8)	I _{DSS}	-	-	-100	μΑ	$V_{DS} = -16V, V_{GS} = 0V$	
Gate-Body Leakage Current	I _{GSS}			±100	nA	$V_{DS} = 0V$, $V_{GS} = \pm 8V$	
Gate Threshold Voltage	V _{GS(th)}	-0.4		-1.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	R _{DS (ON)}		25	45	mΩ	$V_{GS} = -4.5V$, $I_D = -4.5A$	
Statio Brain Source on Nosistance	TVDS (ON)		33	65	11132	$V_{GS} = -2.5V, I_D = -3.8A$	
Static Drain-Source On-Resistance @ T _J = +125°C (Note 8)	R _{DS} (ON)	_		72	mΩ	$V_{GS} = -4.5V$, $I_D = -4.5A$	
Diode Forward Voltage	V _{SD}	-0.5	-0.72	-1.4	V	I _S = -2.1A, V _{GS} = 0V	
On State Drain Current (Note 8)		10	_	_	Α	$V_{DS} \leq 5V$, $V_{GS} = 4.5V$	
DYNAMIC PARAMETERS (Note 8)				•			
Input Capacitance			1,496	2,990	pF		
Output Capacitance	Coss		130	260	ı n⊢ ı	$V_{DS} = -15V, V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}		116	230	pF	1 = 1.01/11/12	
Total Gate Charge	Q_{G}	_	14.4	25			
Gate-Source Charge	Q _{GS}	_	2.6	5	nC	$V_{DS} = -10V, V_{GS} = -4.5V,$ $I_{D} = -4.5A$	
Gate-Drain Charge	Q_{GD}	_	2.7	5.5		ID = -4.5A	
Turn-On Delay Time	t _{d(on)}	_	8.5	30			
Rise Time	t _r		11	60	ns	$V_{DS} = -5V$, $V_{GS} = -4.5V$, $I_{D} = -1A$, $R_{G} = 6.0\Omega$	
Turn-Off Delay Time	t _{d(off)}		61	130			
Fall Time	t _f		25	100			

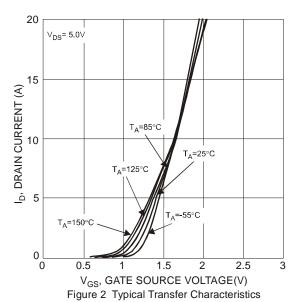
 Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing. Notes:











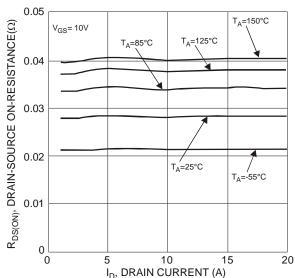
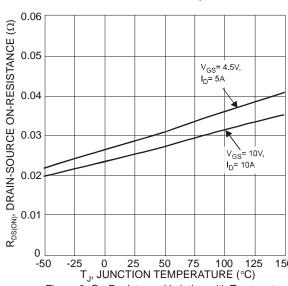


Figure 4 Typical On-Resistance vs.

Drain Current and Temperature



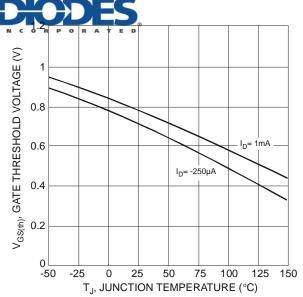


Figure 7 Gate Threshold Variation vs. Ambient Temperature

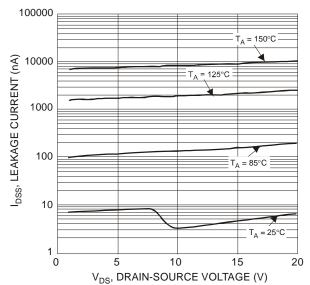
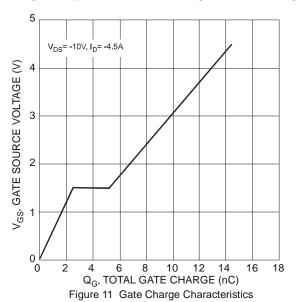


Figure 9 Typical Drain-Source Leakage Current vs. Voltage



DMP2066LVT

16

16

T_A=25°C

T_A=25°C

10

0.2

0.4

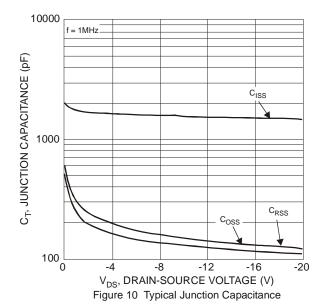
0.6

0.8

1.2

V_{SD}, SOURCE-DRAIN VOLTAGE (V)

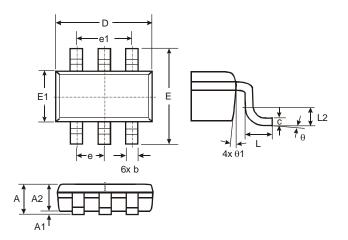
Figure 8 Diode Forward Voltage vs. Current





Package Outline Dimensions

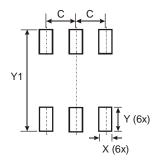
TSOT26



TSOT26							
Dim	Min	Max	Тур				
Α	-	1.00	ı				
A1	0.01	0.10	-				
A2	0.84	0.90	-				
D	_	_	2.90				
Е	-	-	2.80				
E1	_	_	1.60				
b	0.30	0.45	-				
С	0.12	0.20	ı				
е	_	_	0.95				
e1	_	_	1.90				
L	0.30	0.50					
L2	_	_	0.25				
θ	0°	8°	4°				
θ1	4°	12°	_				
All Dimensions in mm							

Suggested Pad Layout

TSOT26



Dimensions	Value (in mm)
С	0.950
Х	0.700
Y	1.000
Y1	3.199



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