# 60V P-CHANNEL ENHANCEMENT MODE MOSFET

## Product Summary

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ max | $I_D$ max $T_A$ = +25°C |
|---|---|---|
| -60V | 25mΩ @ $V_{GS}$ = -10V | -6.6A |
| | 33mΩ @ $V_{GS}$ = -4.5V | -5.8A |

## Features and Benefits

- Low On-Resistance
- Fast Switching Speed
- Low Threshold
- Low Gate Drive
- Low Input Capacitance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Description and Applications

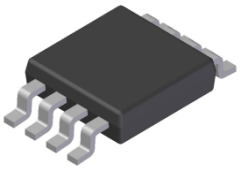
This MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- Power Management Functions
- DC-DC Converters

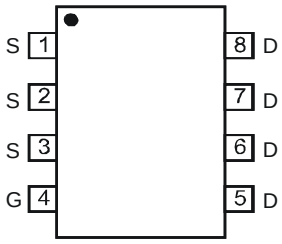
## Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram Below
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)

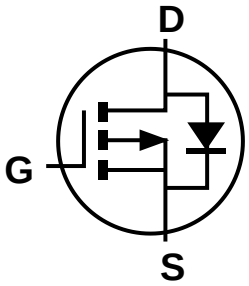
SO-8



Top View




TOP VIEW



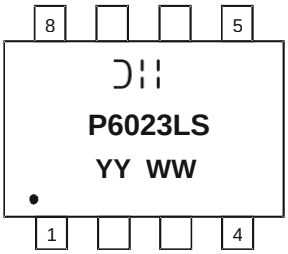

Equivalent Circuit

## Ordering Information (Note 4)

| Part Number | Case | Packaging |
|---|---|---|
| DMP6023LSS-13 | SO-8 | 2,500/Tape & Reel |

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http"//www.diodes.com/products/packages.html.

## Marking Information




= Manufacturer's Marking
P6023LS = Product Type Marking Code
YYWW = Date Code Marking
YY or YY = Last Digit of Year (ex: 14 = 2014)
WW = Week Code (01 - 53)

## Maximum Ratings (@$T_A$ = +25°C unless otherwise specified.)

| Characteristic | | Symbol | Value | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | -60 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current (Note 6) $V_{GS}$ = -10V | $T_A$ = +25°C<br>$T_A$ = +70°C | $I_D$ | -6.6<br>-5.3 | A |
| Pulsed Drain Current (10µs pulse, duty cycle = 1%) | | $I_{DM}$ | -50 | A |
| Maximum Continuous Body Diode Forward Current (Note 6) | | $I_S$ | -1.8 | A |
| Avalanche Current, L = 0.1mH | | $I_{AS}$ | -35.5 | A |
| Avalanche Energy, L = 0.1mH | | $E_{AS}$ | 62.9 | mJ |

## Thermal Characteristics (@$T_A$ = +25°C unless otherwise specified.)

| Characteristic | Symbol | Value | Units |
|---|---|---|---|
| Total Power Dissipation (Note 5) | $P_D$ | 1.2 | W |
| Thermal Resistance, Junction to Ambient (Note 5) | $R_{\theta JA}$ | 100 | °C/W |
| Total Power Dissipation (Note 6) | $P_D$ | 1.6 | W |
| Thermal Resistance, Junction to Ambient (Note 6) | $R_{\theta JA}$ | 75 | °C/W |
| Thermal Resistance, Junction to Case (Note 6) | $R_{\theta JC}$ | 12 | |
| Operating and Storage Temperature Range | $T_J$, $T_{STG}$ | -55 to +150 | °C |

## Electrical Characteristics ($T_A$ = +25°C unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS (Note 7)** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | -60 | — | — | V | $V_{GS}$ = 0V, $I_D$ = -250µA |
| Zero Gate Voltage Drain Current $T_J$ = +25°C | $I_{DSS}$ | — | — | -1 | µA | $V_{DS}$ = -60V, $V_{GS}$ = 0V |
| Gate-Source Leakage | $I_{GSS}$ | — | — | ±100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| **ON CHARACTERISTICS (Note 7)** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | -1 | — | -3 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = -250µA |
| Static Drain-Source On-Resistance | $R_{DS\ (ON)}$ | — | — | 25 | mΩ | $V_{GS}$ = -10V, $I_D$ = -5A |
| | | — | — | 33 | | $V_{GS}$ = -4.5V, $I_D$ = -4A |
| Diode Forward Voltage | $V_{SD}$ | — | -0.7 | -1.2 | V | $V_{GS}$ = 0V, $I_S$ = -1A |
| **DYNAMIC CHARACTERISTICS (Note 8)** | | | | | | |
| Input Capacitance | $C_{iss}$ | — | 2569 | — | pF | $V_{DS}$ = -30V, $V_{GS}$ = 0V, f = 1MHz |
| Output Capacitance | $C_{oss}$ | — | 179 | — | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 143 | — | pF | |
| Gate Resistance | $R_g$ | — | 8 | — | Ω | $V_{DS}$ = 0V, $V_{GS}$ = 0V, f = 1MHz |
| Total Gate Charge ($V_{GS}$ = -4.5V,) | $Q_g$ | — | 26.5 | — | nC | $V_{DS}$ = -30V, $I_D$ = -5A |
| Total Gate Charge ($V_{GS}$ = -10V), | $Q_g$ | — | 53.1 | — | nC | |
| Gate-Source Charge | $Q_{gs}$ | — | 7.1 | — | nC | |
| Gate-Drain Charge | $Q_{gd}$ | — | 12.6 | — | nC | |
| Turn-On Delay Time | $t_{D(on)}$ | — | 6 | — | ns | $V_{GS}$ = -10V, $V_{DS}$ = -30V, $R_G$ = 3Ω, $I_D$ = -5A |
| Turn-On Rise Time | $t_r$ | — | 7.1 | — | ns | |
| Turn-Off Delay Time | $t_{D(off)}$ | — | 110 | — | ns | |
| Turn-Off Fall Time | $t_f$ | — | 62 | — | ns | |
| Body Diode Reverse Recovery Time | $t_{rr}$ | — | 20 | — | nS | $I_F$ = -5A, di/dt = 100A/µs |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | — | 14 | — | nC | |

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

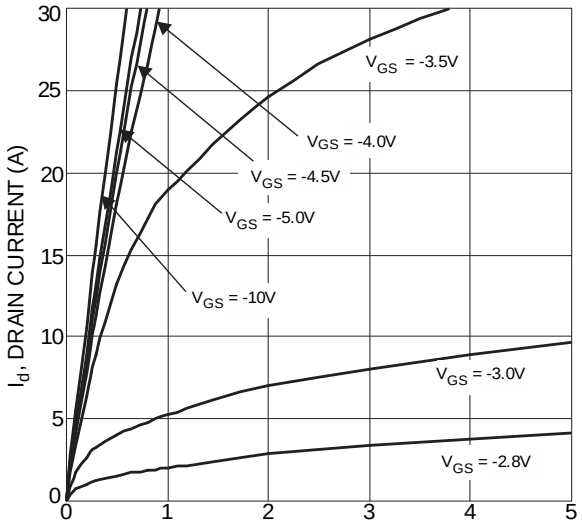


Figure 1 Typical Output Characteristics

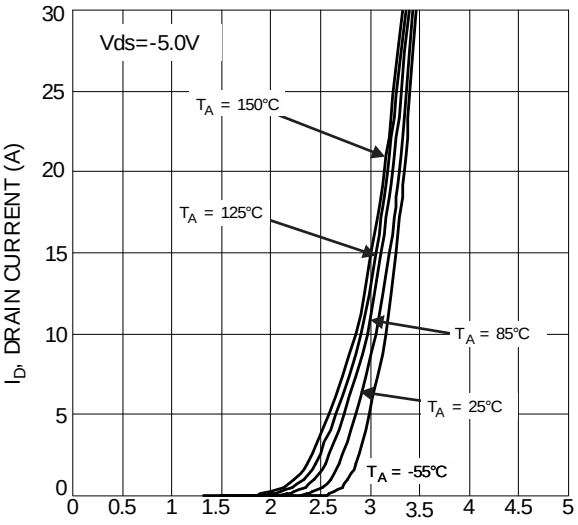


Figure 2 Typical Transfer Characteristics

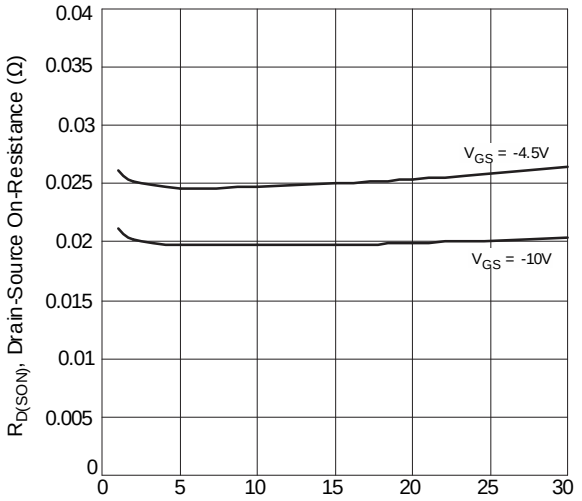


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

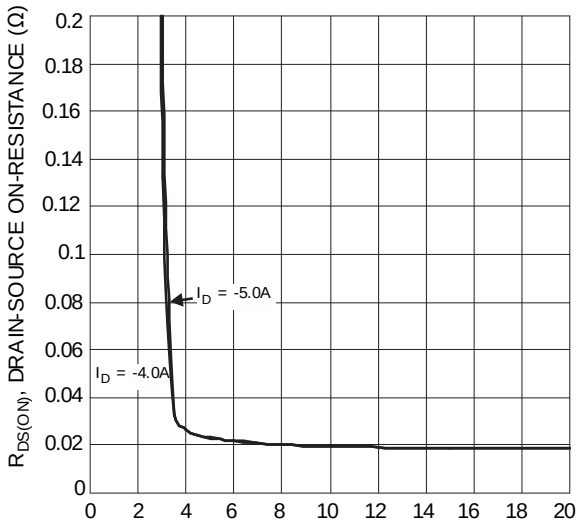


Figure 4 Typical Transfer Characteristics

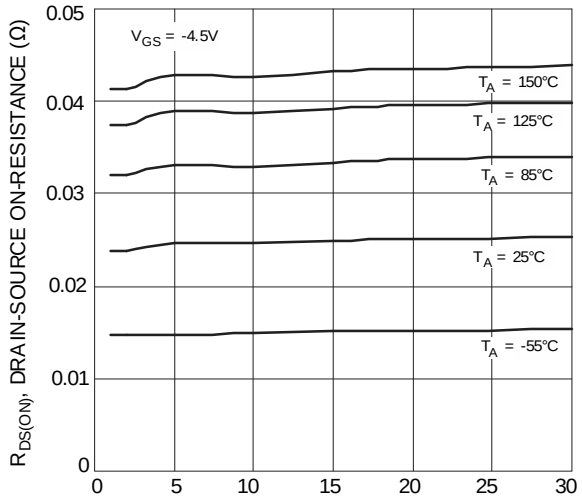


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

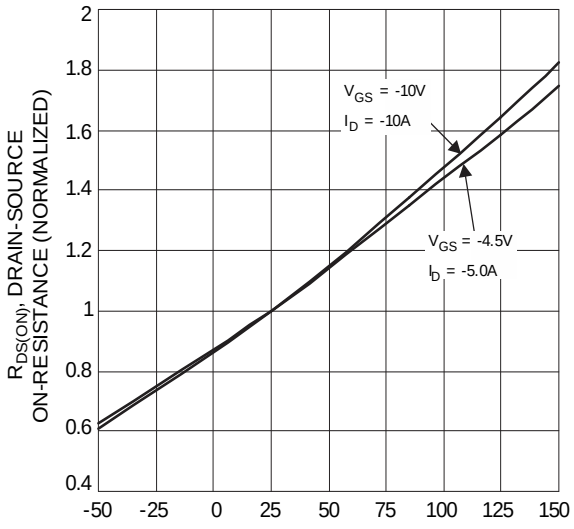


Figure 6 On-Resistance Variation with Temperature

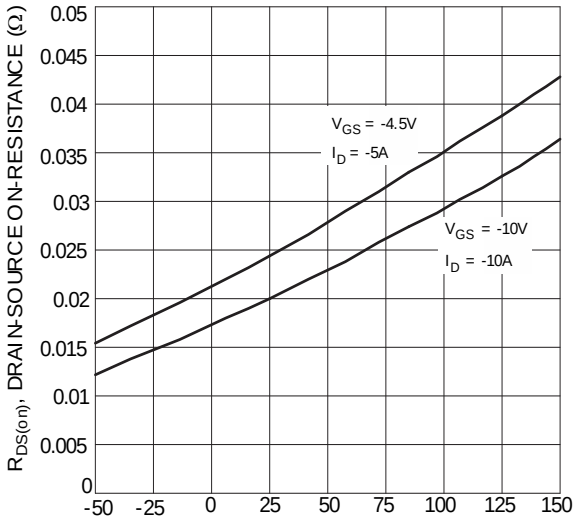


Figure 7 On-Resistance Variation with Temperature

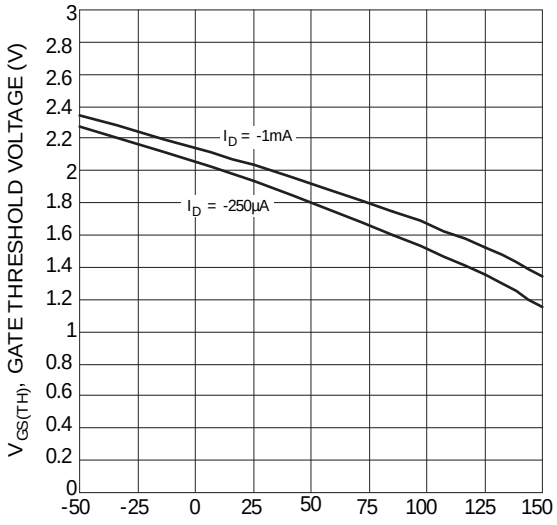


Figure 8 Gate Threshold Variation vs. Ambient Temperature

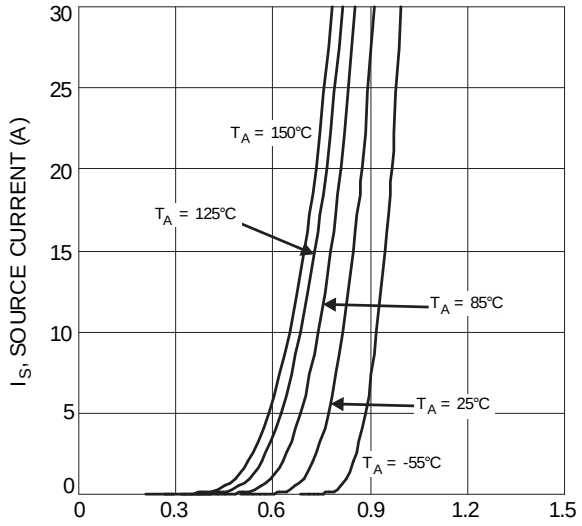


Figure 9 Diode Forward Voltage vs. Current

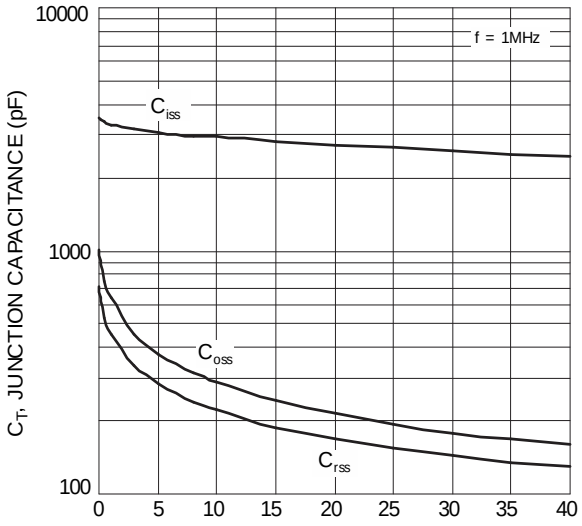


Figure 10 Typical Junction Capacitance

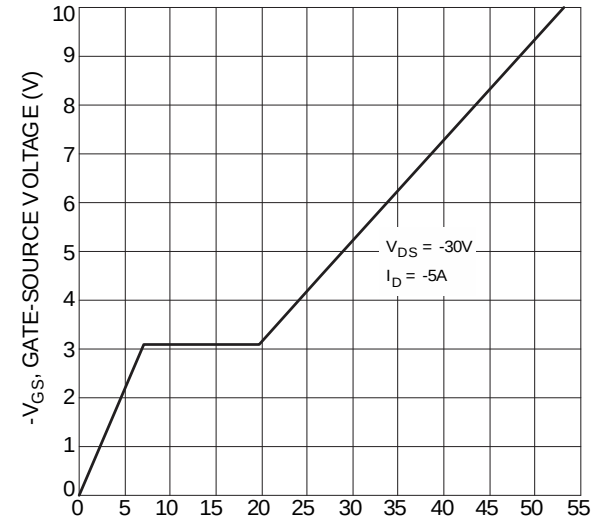


Figure 11 Gate-Charge Characteristics

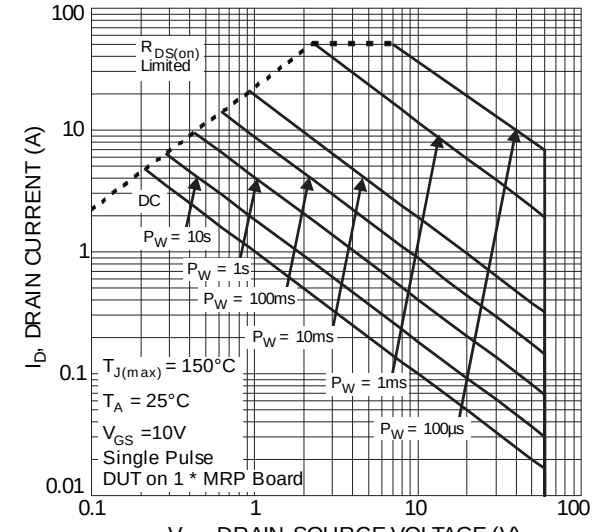


Figure 12 SOA, Safe Operation Area

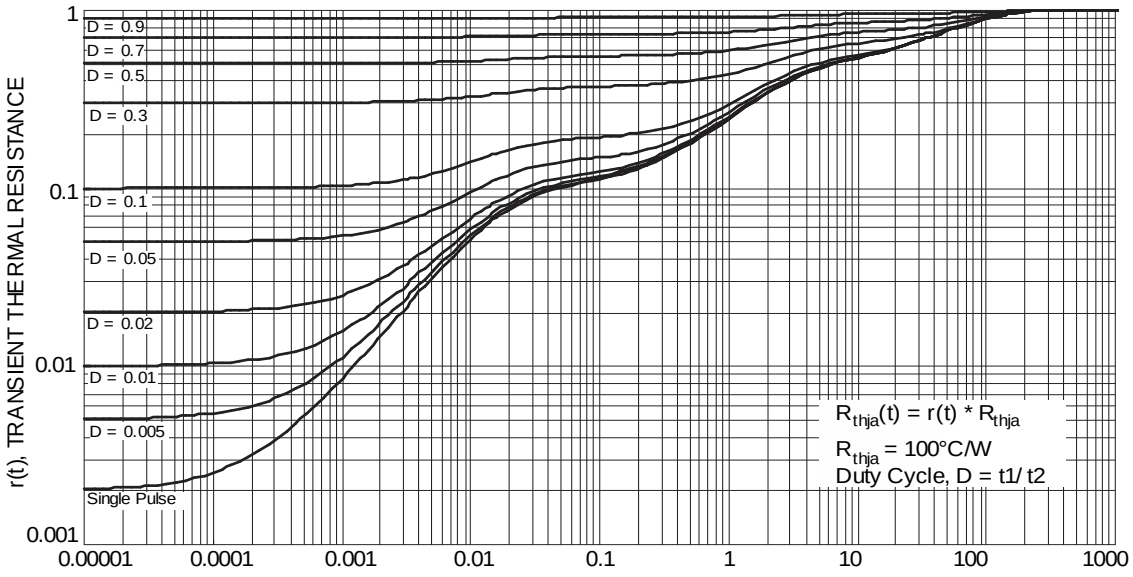
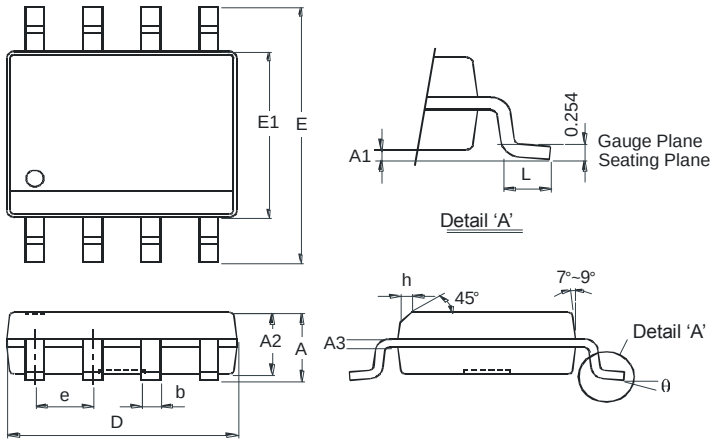



Figure 13 Transient Thermal Resistance

## Package Outline Dimensions

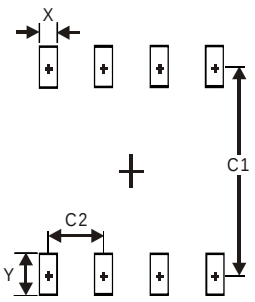
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.




| SO-8 | | |
|---|---|---|
| **Dim** | **Min** | **Max** |
| **A** | - | 1.75 |
| **A1** | 0.10 | 0.20 |
| **A2** | 1.30 | 1.50 |
| **A3** | 0.15 | 0.25 |
| **b** | 0.3 | 0.5 |
| **D** | 4.85 | 4.95 |
| **E** | 5.90 | 6.10 |
| **E1** | 3.85 | 3.95 |
| **e** | 1.27 Typ | |
| **h** | - | 0.35 |
| **L** | 0.62 | 0.82 |
| **θ** | 0° | 8° |
| All Dimensions in mm | | |

## Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.




| Dimensions | Value (in mm) |
|---|---|
| **X** | 0.60 |
| **Y** | 1.55 |
| **C1** | 5.4 |
| **C2** | 1.27 |

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