

LIQUID CRYSTAL DISPLAY MODULE

Product Specification

CUSTOMER	Standard
CUSTOMER PART NUMBER	
PRODUCT NUMBER	DMT035QWNXCSI-1A

Product Mgr	Design Eng
Luo Luo	Eric Wan
Date: 09-Jan-17	Date: 09-Jan-17

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECN no.
1.0	09-Jan-17			Initial Release	ECN8016

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1 MAIN FEATURES

ITEM	CONTENTS
Screen Size	3.5" Diagonal
Display Format	320 x RGB x 480 Dots
N° of Colour	262K
TFT Active Area	48.96 mm (H) x 73.44 mm (V)
LCD Type	TFT
Mode	IPS Transmissive / Normally Black
Viewing Direction	Full view
TFT Interface	8/9/16/18-bit DBI Type B (CPU) interface 3/4-lines SPI +16/18-bit RGB interface; 3/4-lines SPI
PCT Interface	I2C
TFT Driver IC	ILI9488 or equivalent
PCT Driver IC	FT6236
Simultaneous Touch Points	Single point and Gestures
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

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2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

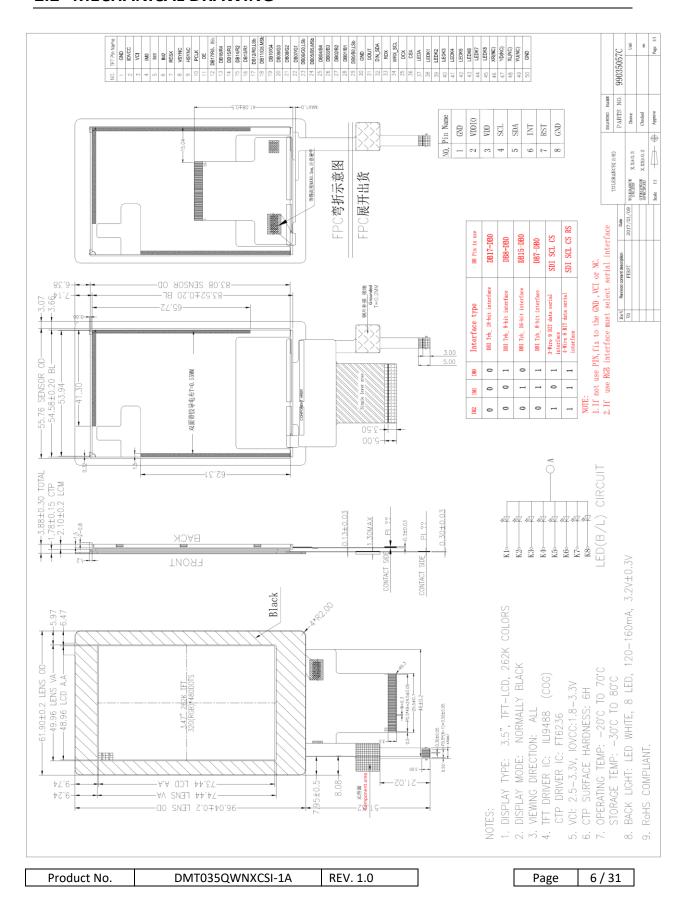
ITEM	CHARACTERISTIC	UNIT
Display Format	320 x RGB x 480 Dots	Dots
Overall Dimensions	61.90 mm (H) x 96.04 mm (V) x 3.88 mm (D)	mm
Active Area	48.96 mm (H) x 73.44 mm (V)	mm
pixel Pitch	153 (H) x 153 (V)	μm
Weight	30	g

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2.2 MECHANICAL DRAWING





3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

3.1.1 TFT

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage	VCI	Ta=25°C	-0.3	4.6	V	
Digital Interface Supply Voltage	IOVCC	Ta=25°C	-0.3	4.6	V	
Operating Temperature	ТОР		-20	70	°C	1
Storage Temperature	TST		-30	80	°C	1,2,3

- Note 1. 90 % RH Max for Ta<50 °C, and 60% RH for Ta≥50°C.
- Note 2. In case of below 0°C, the response time of liquid crystal (LC) becomes slower and the colour of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's characteristic.
- Note 3. Only operation is guaranteed at operating temperature. Contrast, response time, another display quality are evaluated at +25°C.

3.1.2 PCT

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage	VDD	Ta=25°C	-0.3	3.6	V	4
I/O Digital voltage	VDDIO	Ta=25°C	1.8	3.6	V	4
Operating Temperature	ТОР		-20	70	°C	-
Storage Temperature	TST		-30	80	°C	-

Note 4. If used beyond the absolute maximum ratings, FT6236 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

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3.2 DC ELECTRICAL CHARACTERISTICS

3.2.1 TFT

Item	Symbol	Condition	Min	Тур	Max	Unit	Note
Supply Voltage	VCI		2.8	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC		1.8	-	3.3	V	
Input Voltage for Logic	VIH		0.7 IOVCC	-	IOVCC	V	
	VIL		GND	-	0.3 IOVCC	V	
Outrot Valtaga familiasia	VOH		0.8 IOVCC	-	IOVCC	V	
Output Voltage for Logic	VOL		GND	-	0.2 IOVCC	V	
Current Consumption	IDD		-	8		mA	1

Note 1: The specified power consumption is under the conditions of VCI=3.3V, FV=60Hz.

3.2.2 PCT

Item	Symbol	Condition	Min	Тур	Max	Unit	Note
Supply Voltage	VDD		2.8	3.3	3.6	V	
I/O Digital Supply Voltage	VDDIO		1.8	3.3	3.6		
Input Voltage for Logic	VIH		0.7VDDIO	-	VDDIO	V	
	VIL		-0.3	-	0.3VDDIO	V	
Output Voltage for Logic	VOH	IOH=-0.1mA	0.7VDDIO	-	-	V	
	VOL	IOH=0.1mA	-	-	0.3VDDIO	V	
Normal operation mode Current Consumption	IOPR	VDD=2.8V	-	4	-	mA	
Green mode Current Consumption	IMON	Ta=25°C MCLK=17.5	-	1.5	-	mA	
Sleep mode Current Consumption	ISLP	Mhz	-	50	-	uA	

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3.3 INTERFACE PIN ASSIGNMENT

3.3.1 LCM PIN ASSIGNMENT

Recommended connector: MOLEX 51296-5093

NO.	SYMBOL	Description Recommended connector: MOLEX 51296-5093
1	GND	Ground.
2	IOVCC	Supply voltage for IO (IOVCC=1.8V-3.3V).
3	VCI	Supply voltage (VCI=3.3V).
4	IM0	Supply voltage (vol. 5.5 v).
5	IM1	Interface selecting mode signal.
6	IM2	interruce selecting mode signal.
7	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
8	Frame synchronizing signal for DPI I/F mode. If not used, please connect to GND.	
9	HSYNC	Frame synchronizing signal for DPI I/F mode. If not used, please connect to GND.
10	PCLK	Pixel clock signal for DPI I/F mode. If not used, please connect to VCI.
11	DE	A DATA ENABLE signal for DPI I/F mode. If not used, please connect to GND.
12-29	DB17-DB0	Data bus PINS. 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 When Operation in MIPI DPI interface mode, it is an 18-bit bus RGB data bus. 6-bit bus: use DB5-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 Pins not used must be connected to GND.
30	GND	Ground.
31	DOUT	Serial data output pin in serial bus system interface. If not used, please open this pin.
32	DINI_SDA	Serial data input pin or input/output pin in serial bus system inter face. The data is inputted on the rising edge of the SCL signal. If not used, please connect to GND.
33	RDX	DBI Type-B: Serves as a read signal and read data at the low level. If not used, please connect to VCI.

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No	SYMBOL	Description
34	WRX_SCL	DBI Type-B: Serves as a write signal and write data at the low level. DBI Type-C: it servers as SCL (Serial Clock). If not use, please connect to GND.
35	DCX	Data / Command Selection pin. If not use, please connect to GND.
36	CSX	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. If not used, please connect to GND.
37	LEDA	Power supply for Backlight.
38-45	LEDK1-LEDK8	Power supply for Backlight.
46	XR(NC)	NC.
47	YD(NC)	NC.
48	XL(NC)	NC.
49	YU(NC)	NC.
50	GND	Ground.

3.3.2 PCT PIN ASSIGNMENT

Pin NO.	Symbol	Function
1	GND	Ground
2	VDDIO	I/O power supply voltage.
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

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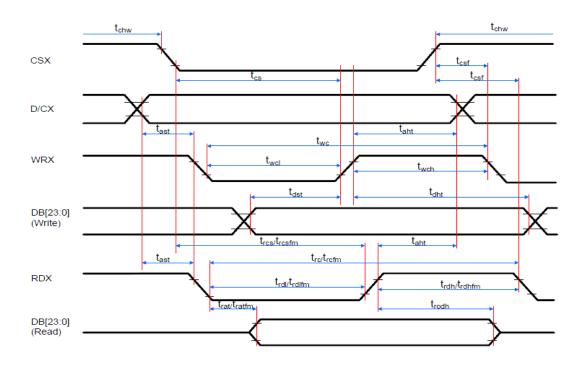
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3.4 TIMING CHARACTERISTICS

Please refer to Ilitech IC ILI9488 datasheet for more information

3.4.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)



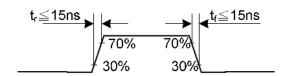
Signal	Symbol	Parameter	min	max	Unit	Description
DOV	tast	Address setup time	0	-	ns	-
DCX	that	Address hold time (Write/Read)	0	-	ns	-
	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
	twc	Write cycle	40	-	ns	-
WRX	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
	trcfm	Read Cycle (FM)	450	-	ns	
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	When read from Frame Memory
	trdlfm	Read Control L duration (FM)	355	-	ns	Welliory
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	When read ID data
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0],	tdst	Write data setup time	10	-	ns	
DB [23.0], DB [17:0],	tdht	Write data hold time	10	-	ns	
DB [15:0],	trat	Read access time	-	40	ns	For maximum, CL=30pF For minimum, CL=8pF
DB [8:0],	tratfm	Read access time	-	340	ns	For minimum, GL=6PF
DB [7:0]	trod	Read output disable time	20	80	ns	

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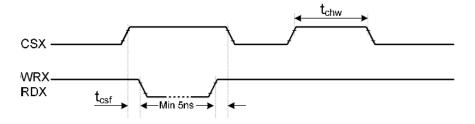


Notes:

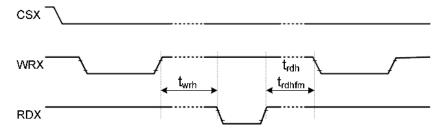
- 1. Ta = -30 to 70 $^{\circ}$ C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
- 2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
- 3. Input signal rising time and falling time:



4. The CSX timing:



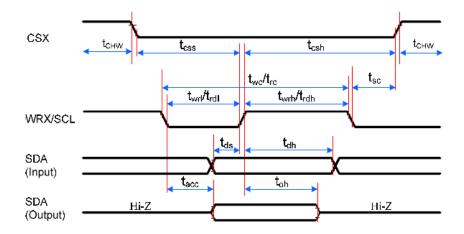
5. The Write to Read or the Read to Write timing:



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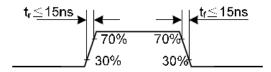


3.4.2 Display Serial Interface Timing Characteristics (3-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
	tsc	SCL-CSX	15	-	ns	
201	tchw	CSX H Pulse Width	40	-	ns	
CSX	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
001	twrl	SCL L Pulse Width (Write)	15	-	ns	
SCL	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA	tds	Data setup time (Write)	10	-	ns	
(Input)	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
(Output)	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

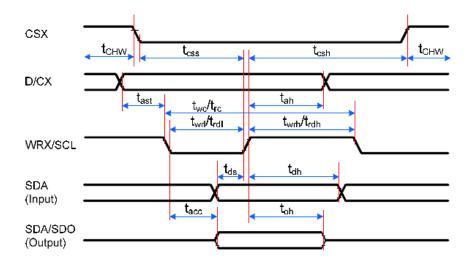
Note: Ta = -30 to 70 $^{\circ}$ C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



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3.4.3 Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
	tcss	Chip select time (Write)	15	-	ns	
CSX	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
001	twrl	SCL L pulse width (Write)	10	-	ns	
SCL	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
5/5/	tas	D/CX setup time	10	-	ns	
D/CX	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA	tds	Data setup time (Write)	10	-	ns	
(Input)	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
(Output)	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

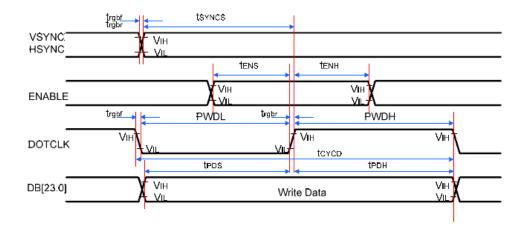
Notes:

- 1. Ta = -30 to 70 $^{\circ}$ C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
- 2. Does not include signal rising and falling times.

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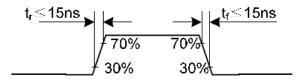


3.4.4 Parallel RGB Interface Timing Characteristics



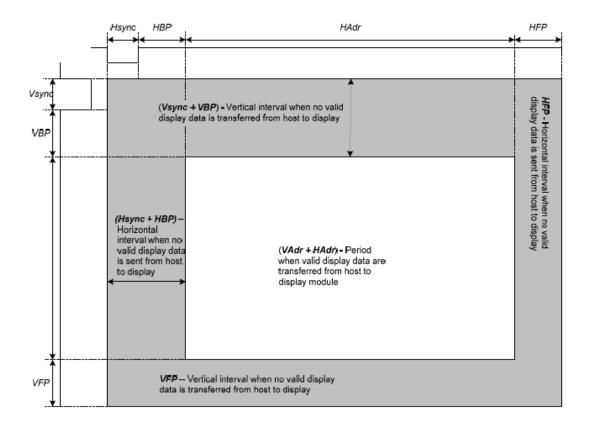
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
ENIA DI E	t _{ENS}	ENABLE setup time	15	-	ns	
ENABLE	t _{ENH}	ENABLE hold time	15	-	ns	
	t _{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus
DB [23:0]	t _{PDH}	Data hold time	15	-	ns	RGB interface mode
	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
DOTCLK	t _{cycp}	DOTCLK cycle time	50	-	ns	
	t _{rgbr} , t _{rgbt}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 $^{\circ}$ C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V



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Parameters	Symbols	Min.	Тур.	Max.	Units
PCLK Cycle	PCLK _{CYC}	100	80	66.6	ns
Horizontal Synchronization	Hsync	3	3		PCLK
Horizontal Back Porch	HBP	3	3		PCLK
Horizontal Address	HAdr	-	320	٠	PCLK
Horizontal Front Porch	HFP	3	3	•	PCLK
Vertical Synchronization	Vsync	2	2		Line
Vertical Back Porch	VBP	2	2	٠	Line
Vertical Address	VAdr	-	480	٠	Line
Vertical Front Porch	VFP	2	2		Line
Vertical Frequency(*)		50	60	80	Hz
Horizontal Frequency(*)		-	33	•	KHz
PCLK Frequency(*)		10	12.5	15	MHz

Notes:

- 1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
- 2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
- Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

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3.4.5 PCT I2C Interface Timing Characteristics

Table 4-1 AC Characteristics of Oscillators

Item	Symbol	Test Cond	lition	Min	Тур.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V;	Ta=25°C	34.65	35	35.35	MHz	

Table 4-2 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Тур.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V; Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V; Ta=25°C	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V; Ta=25°C	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V; Ta=25°C	-	5	-	V	

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure4-1:

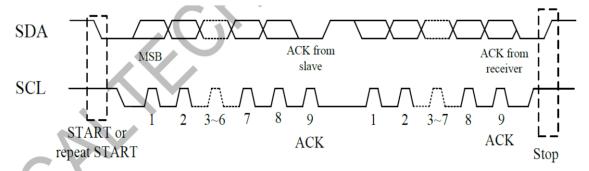


Figure 4-1 I2C Serial Data Transfer Format

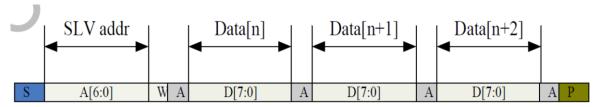


Figure 4-2 I2C master write, slave read

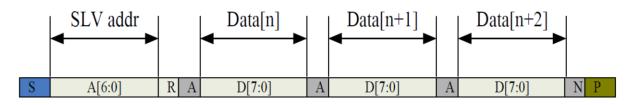


Figure 4-3 I2C master read, slave write

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Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristcs is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

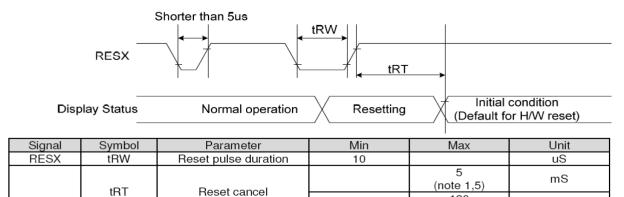
Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

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3.4.6 Reset Timing Characteristics



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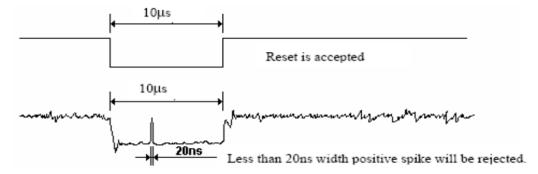
Note 1: The reset cancel includes also required time for loading ID bytes. VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line dose not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode.) and then return to default condition for Hardware Reset.

Note 4: Spike rejection also applies during a valid reset pulse as shown below:



Note 5: When reset applied during Sleep in Mode.

Note 6: When reset applied during Sleep out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Measuring instruments: LCD-5100, Eldim, Topcon BM-7

Driving condition: VCI = 3.3V, VSS = 0V

Backlight: IF=160mA Measured temperature: $Ta = 25^{\circ}C$

	Item	Symbol	Condition	MIN	ТҮР	MAX	Unit	Note
Response Time Contrast Ratio		TR+TF	θ=Ф=0°	-	35	50	ms	2
		CR	Normal Viewing Angle	-	500	-		3
	Left	θL	- CR ≥ 10	-	80	-	deg	
Viewing Angle	Right	θR		ı	80	-	deg	4
Viewing	Up	φU		-	80	-	deg	·
	Down	φD		-	80	-	deg	
	Dad	Rx		-	0.631	0.633	-	
	Red	Ry		-	0.334	0.335	-	
Colour Chromaticity	Croon	Gx		-	0.316	0.318	-	
0.0	Green	Gy	CR ≥ 10	-	0.602	0.605	-	1
Ę	Blue	Вх	CR 2 10	-	0.151	0.152	-	5
nolo	blue	Ву		-	0.047	0.049	=	
8	\A/la:4-a	Wx		-	0.301	0.303	-	
	White	Wy		-	0.335	0.337	-	
Centr	e Brightness			-	500	-	cd/m²	6
Bright	ness Distribution			80	-	-	%	7

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4.1.1 Test Method

Note	Item	Test method
1	Setup	The display should be stabilised at a given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilise the luminance, measurements should be executed after lighting the backlight for 30 minutes in a windless room. Display Center of the Screen Photometer (TOPCONBM-7 Fast) Field of View = 29 Light Shield Room (Ambient Luminance < 1 lux)
2	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. White 100% 90% Black TONE TON
3	Contrast ratio	Measure maximum brightness and minimum brightness at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Brightness of unselected position (white) Contrast Ratio (CR) = Brightness of selected position (black)
4	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10 $\theta = \phi = 0^\circ$
5	Colour chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system
6	Centre brightness	Measure the brightness at the centre of the screen
7	Brightness distribution	(Brightness distribution)= 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points

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5 BACKLIGHT SPECIFICATION

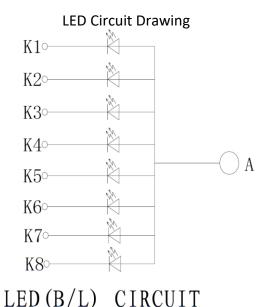
5.1 LED DRIVING CONDITIONS

Item	Symbol	Condition	Min	Тур	Max	Unit
Forward Current	IF	Ta=25 °C, VF=3.2V/LED	150	160	1	mA
Forward Voltage	VF	Ta= 25°C, IF= 20mA/LED		3.2		V
LED life time	Hr			50k		hour

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
 The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

5.2 LED CIRCUIT



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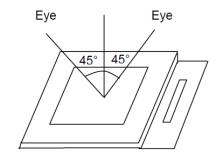
6 QUALITY ASSURANCE SPECIFICATION

6.1 DELIVERY INSPECTION STANDARDS

6.1.1 Inspection Conditions

Inspection distance: 30 cm ± 2 cm

Viewing angle: ±45°



6.1.2 Environmental Conditions

Ambient temperature: $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ Ambient humidity: $65\pm 10\% \text{ RH}$ Ambient illumination: $300^{\sim}700 \text{ lux}$

6.1.3 Sampling Conditions

- 1. Lot size: quantity of shipment lot per model
- 2. Sampling method:

	Campling Plan	GB/T 2828-2003
Sampling Plan		Normal inspection, Class II
401	Major Defect	0.65%
AQL	Minor Defect	1.5%

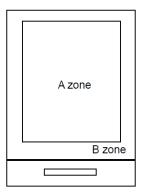
No	Items to be	Criteria	Classification of
	inspected		defects
		1) No display, Open or miss line	
1	Functional defects	2) Display abnormally, Short	
'	Functional defects	3) Backlight no lighting, abnormal lighting.	
		4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing	
J	Oddine dimension	is not allowed	
4	Color tone	Color unevenness, refer to limited sample	
E	Soldering	Good soldering , Peeling off is not allowed.	Minor
5	appearance		Minor
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

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6.1.4 Definition of Area

A zone: active area B zone: viewing area



6.1.5 Basic Principle

A set of sample to indicate the limit of acceptable quality level shall be discussed should a dispute occur.

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6.1.6 Inspection Criteria

Number	Items	Criteria(mm)
1.0 LCD Crack/Broken	(1) The edge of LCD broken	
NOTE:		X Y Z
X: Length Y: Width		≤3.0mm
Z: Height L: Length of ITO, T: Height of LCD	(2)LCD corner broken	X Y Z ≤3.0mm ≤L ≤T
	(3) LCD crack	Crack Not allowed

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Number	Items		Crite	eria (mm)		
2.0	Spot defect	① light dot (LCD	/TP/Polarizer bla	ack/white s	pot , light dot,	pinhole, dent
		stain)				_
		Zone	Acc	cep able Q	ty	
		Size (mm)	Α	В	С	
	X	Ф≤0.10	Ignor	е		
		0.10<Φ≤0.20	3(distance≧	≧10mm)	lanan	
	Φ=(X+Y)/2	0.20<Φ≤0.25	2		lgnor	
		Φ > 0.25	0			
		②Dim spot(LCD/	TP/Polarizer din	n dot, light	leakage、dark	spot)
		Zone	Ac	ceptable Q	ty	
		Size (mm)	Α	В	С	
		Ф≤0.1	Ignore	е		
		0.10<Φ≤0.20	3(distance≧	10mm)	lanore	
		0.20<Φ≤0.30	2		Ignore	
		Ф > 0.30	0			
		③ Polarizer accide	ented spot			_
		Zone	Ac	cceptable C	1	
		Size (mm)	Α	В	С	
		Ф≤0.2	Ignoi			
		0.3<Φ≤0.5	2(distance	≧ 10mm)	Ignore	
		Ф>0.5	0			
	Line defect (LCD/TP			A	ontable Otiv	
	/Polarizer	Width(mm)	Length(mm	0.000	eptable Qty	
	black/white	Φ<0.03	lance	A	ВС	_
	line, scratch,	Φ≤0.03 0.03 <w≤0.05< td=""><td>Ignoe L≤3.0</td><td>Ignore</td><td></td><td></td></w≤0.05<>	Ignoe L≤3.0	Ignore		
	stain)	0.03 <vv≤0.05 0.05<w≤0.08< td=""><td>L≤3.0 L≤2.0</td><td>N≤2 N≤2</td><td></td><td></td></w≤0.08<></vv≤0.05 	L≤3.0 L≤2.0	N≤2 N≤2		
		0.05 <vv≤0.08 0.08<w< td=""><td></td><td>ne as spot o</td><td></td><td>-</td></w<></vv≤0.08 		ne as spot o		-
		0.00<	Deli	ne as spot (ueleci	

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		Zone		Acceptable C	Qty	
3.0	Polarizer	Size (mm)	Α	В	С	
3.0	Bubble	Φ≤0.2 0.2<Φ≤0.4 0.4<Φ≤0.6 0.6<Φ	Ign 3(distanc	ore e≥10 m) 2	Ignore	
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.				

	Size Φ(mm)	Ad	cceptable (Qty	
	Size $\Phi(\Pi\Pi\Pi)$	Α	В	С	
TP bubble/	Ф≤0.1	Igno	ore		
	0.1<Φ≤0.25			Ignore	
accidented	0.25<Φ≤0.3	2	<u> </u>	ignore	
spot	0.3<Ф	0			
Assembly deflection		beyond the edge of backlight ≤0.15mm			

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5.0	TP								
5.0	Related	Newto Ring		Newton Ri NG Newton Ri OK				1規律性 2期類性 似牛顿环	
		TP cor	ner						
		broke	n	X	Y	Z		x Y	
		X : len	gth	X≤3.0mm	Y≤3.0mm	z <l0< td=""><td> -</td><td></td></l0<>	-		
		Y : wic	dth	* Circuitry b	oroken is no	ot allow	ed.		
		Z : hei	ght						
		TP ed		x	Υ	Z	\neg	XXXX	
		broke X : len		X≤6.0mm	Y≤2.0mm	Z <lc thickne</lc 		Z	
		Y : wic	dth						
		Z : hei	ght	* Circuitry broken is not allowed.		ed.			
N				14.5	me			Critorio (mm)	
Number				Items No diamer.				Criteria (mm) Not allowed	
1			No display				NOT AllOWED		

Number	Items	Citteria (IIIII)	
1	No display	Not allowed	
2	Missing segment	Not allowed	
3	Short	Not allowed	
4	Backlight no lighting	Not allowed	
5	TP no function	Not allowed	

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6.1.7 Classification of Defects

Visual defects (except no or wrong label) are treated as minor defects, while electrical defects are treated as major defects.

Two minor defects are equal to one major defect in lot sampling inspection.

6.1.8 Identification / marking criteria

Any unit with illegible / wrong / double or no marking / label shall be rejected.

6.2 DEALING WITH CUSTOMER COMPLAINTS

6.2.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.2.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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7 RELIABILITY SPECIFICATION

7.1 RELIABILITY TESTS

	Test Item	Test Condition			
	High Temperature Storage	Ta= 80°C	96h		
	Low Temperature Storage	Ta=-30°C	96h		
	Temperature Cycle Storage		C ON/OFF, 20 cycles. ON time over 10 ime over 10 seconds		
	High Temperature Operation	Tp= 70°C	96h		
st	Low Temperature Operation	Tp= -20°C	96h		
Durability Test	High Temperature & Humidity Operation	· •	p= 70°C RH= 90% 96h Ion condensing		
Durab	ESD Test	150Pf, 330Ω, ±6KV (Contact)/±8KV (Air), 5 Points/panel, 10 times/point			
	Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours			
	Box Drop Test	1 Corner 3 Edges 6 faces, 66 cm (Medium Box)			

Note: Ta=ambient temperature Tp= Panel temperature

Notes:

- 1. No dew condensation to be observed.
- 2. The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.
- 3. No cosmetic or functional defects should be allowed.
- 4. Total current consumption should be less than twice the initial value.

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8 HANDLING PRECAUTIONS

Safety

If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface. Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS. Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height. To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH. Store the display in a clean environment, free from dust, organic solvents and corrosive gases.

Do not crash, shake or jolt the display (including accessories).

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