



N-Channel Depletion-Mode Vertical DMOS FETs

Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Normally-on switches
- ▶ Battery operated systems
- ▶ Voltage to current converters
- ▶ Constant current sources
- ▶ Current and voltage limiters

General Description

These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
DN2450K4-G	TO-252 (D-PAK)	2000/Reel
DN2450N8-G	TO-243AA (SOT-89)	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availability.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Product Summary

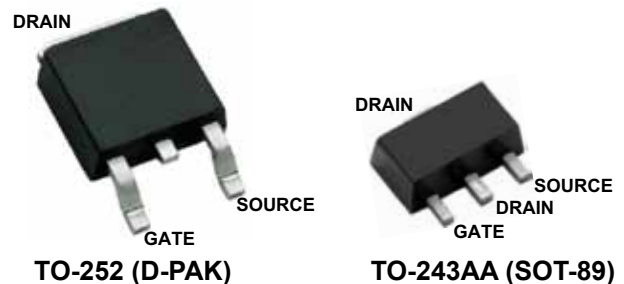
BV_{DSX}/BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)
500V	10Ω	700mA

Absolute Maximum Ratings

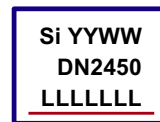
Parameter	Value
Drain-to-source voltage	BV_{DSX}
Drain-to-gate voltage	BV_{DGX}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Maximum junction temperature	150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-252 (D-PAK)



W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-243AA (SOT-89)

Typical Thermal Resistance

Package	θ_{ja}
TO-252 (D-PAK)	81°C/W
TO-243AA (SOT-89)	133°C/W

Thermal Characteristics

Package	I_D (continuous) [†]	I_D (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	I_{DR} [†]	I_{DRM}
TO-252	350mA	1.0A	2.5W [‡]	350mA	1.0A
TO-243AA	230mA	900mA	1.6W [‡]	230mA	900mA

Notes:

- [†] I_D (continuous) is limited by max rated T_r .
- [‡] Mounted on FR4 board, 25mm x 25mm x 1.57mm.

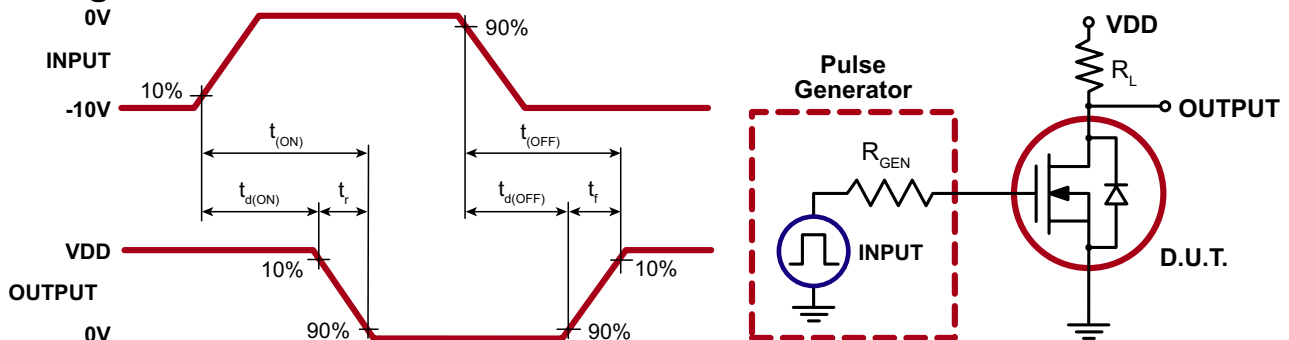
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	500	-	-	V	$V_{GS} = -5.0\text{V}, I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	$V_{DS} = 25\text{V}, I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/°C	$V_{DS} = 25\text{V}, I_D = 10\mu\text{A}$
I_{GSS}	Gate body leakage [‡]	-	-	100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	1.0	μA	$V_{DS} = \text{Max rating}, V_{GS} = -10\text{V}$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = -10\text{V}, T_A = 125^\circ\text{C}$
I_{DSS}	Saturated drain-to-source current	700	-	-	mA	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	7.0	10	Ω	$V_{GS} = 0\text{V}, I_D = 300\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/°C	$V_{GS} = 0\text{V}, I_D = 300\text{mA}$
G_{FS}	Forward transconductance	500	-	-	mmho	$V_{DS} = 10\text{V}, I_D = 300\text{mA}$
C_{ISS}	Input capacitance	-	150	200	pF	$V_{GS} = -10\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$
C_{OSS}	Common source output capacitance	-	40	55		
C_{RSS}	Reverse transfer capacitance	-	15	25		
$t_{d(ON)}$	Turn-on delay time	-	-	15	ns	$V_{DD} = 25\text{V}, I_D = 300\text{mA}, R_{GEN} = 25\Omega,$
t_r	Rise time	-	-	20		
$t_{d(OFF)}$	Turn-off delay time	-	-	15		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = -5.0\text{V}, I_{SD} = 300\text{mA}$
t_{TR}	Reverse recovery time	-	800	-	ns	$V_{GS} = -5.10\text{V}, I_{SD} = 300\text{mA}$

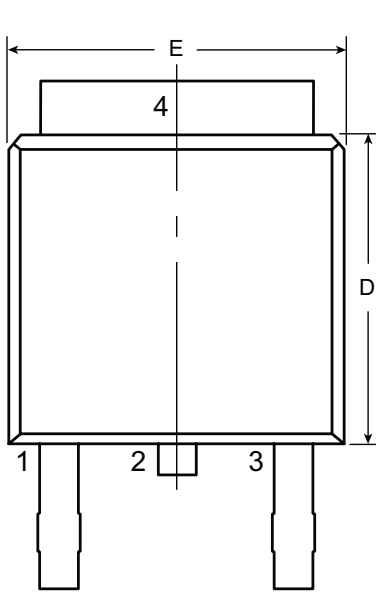
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

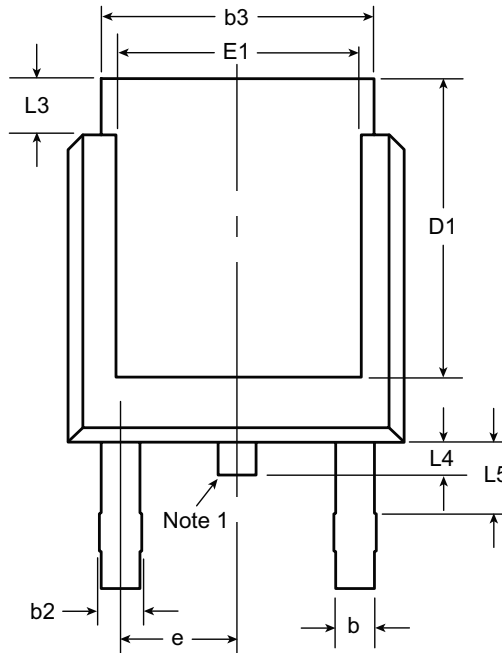
Switching Waveforms and Test Circuit



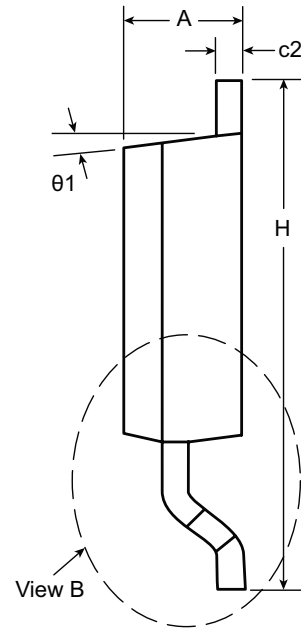
3-Lead TO-252 (D-PAK) Package Outline (K4)



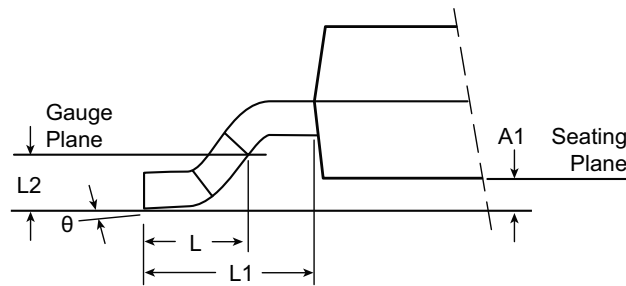
Front View



Rear View



Side View



View B

Note:

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol	A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1		
Dimension (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0°	0°		
	NOM	-	-	-	-	-	-	.240	-	-	-	-	.060			-	-	-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*	.410	.070			.050	.040	.060	10°	15°		

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.

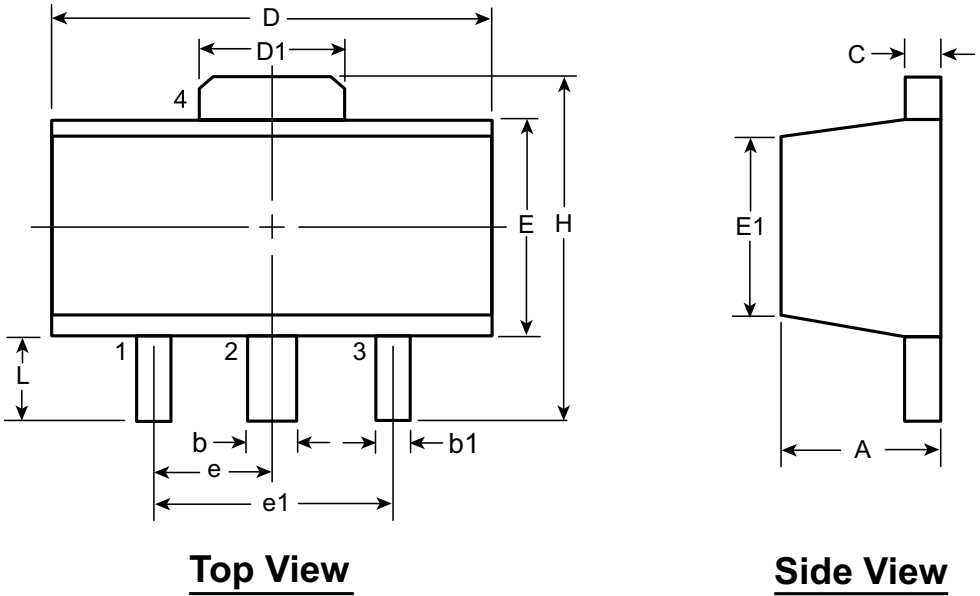
* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO252K4, Version F040910.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View

Side View

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.73 [†]		
	NOM	-	-	-	-	-	-	-	-			-	-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20		

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version F111010.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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