matched dual n-channel JFETs *designed for...*

Siliconix

Performance Curves
NCB-D
See Section 4

■ Dual FET

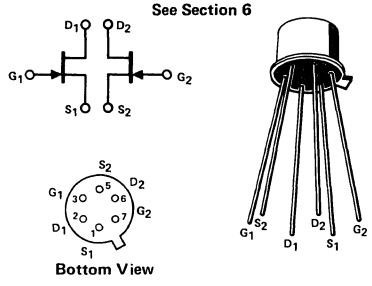
BENEFITS

- High Density
- Matched Switch Resistance
- Constant $r_{DS(on)}$ with Signal

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage . . . . . ±80 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 2.2 mW/°C) . . . . . 325 mW
Total Device Dissipation, T_A = 25°C
(Derate 3.3 mW/°C) . . . . . 650 mW
Storage Temperature Range . . . . . −65°C to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		−100	pA	V_{GS} = −20 V, V_{DS} = 0	
2					−200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40		V	I_G = 1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		2.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	60	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYN	C_{gd}	Drain-Gate Capacitance		7	pF	V_{GS} = −10 V	f = 1 MHz
9		C_{gs}	Gate-Source Capacitance		7		V_{DS} = 10 V	
10	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.9	1	–	V_{DS} = 15 V, V_{GS} = 0	
11		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		20	mV		
12		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.9	1	–		f = 1 kHz

NOTES: NCB-D

1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.