Product Specification

❖ **Product Name: AMOLED**

❖ **Model Name: DO0143PFST03**

❖ **Description: 1.43 inch (466 x 466)**

Proposed by			Customer's Approval
Designed	Checked	Approved	

Document Revision History

Rev. No.	Date	Contents	Remark
0.0	2023-12-12	-.Initial issue	Preliminary

1.General Description:

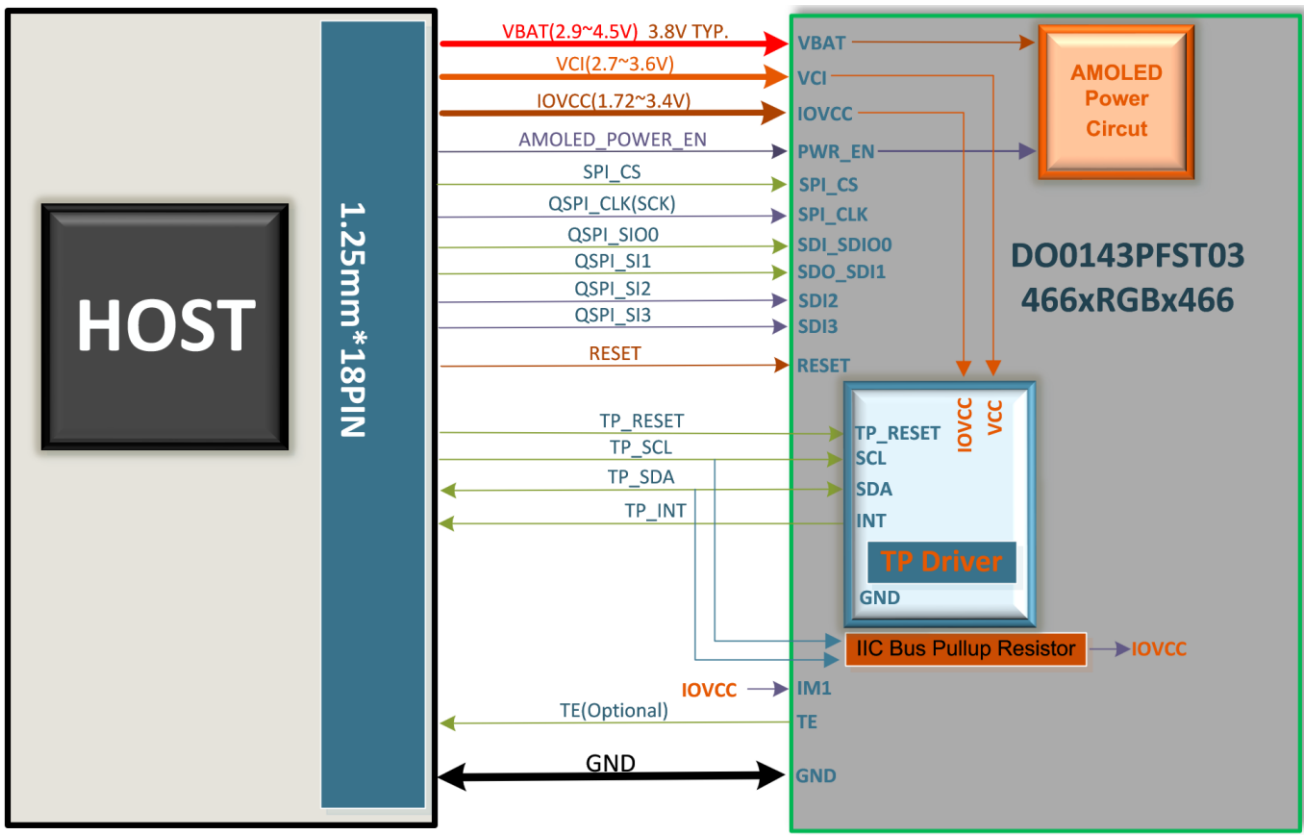
- Driving Mode: Active Matrix.
- Color Mode: Full Color (16.7M color)
- Display Format: 1.8" (368 x 448)
- Display Driver IC : SH8601 or Compatible
- Touch Driver IC : FT3168 or Compatible
- Display Interface: SPI 3-wire / QSPI
- Touch Interface: IIC [**Slave Addr A[6:0]---0X38**]
- Application: Handheld & PDA
- RoHS Compatible

2.Mechanical Data

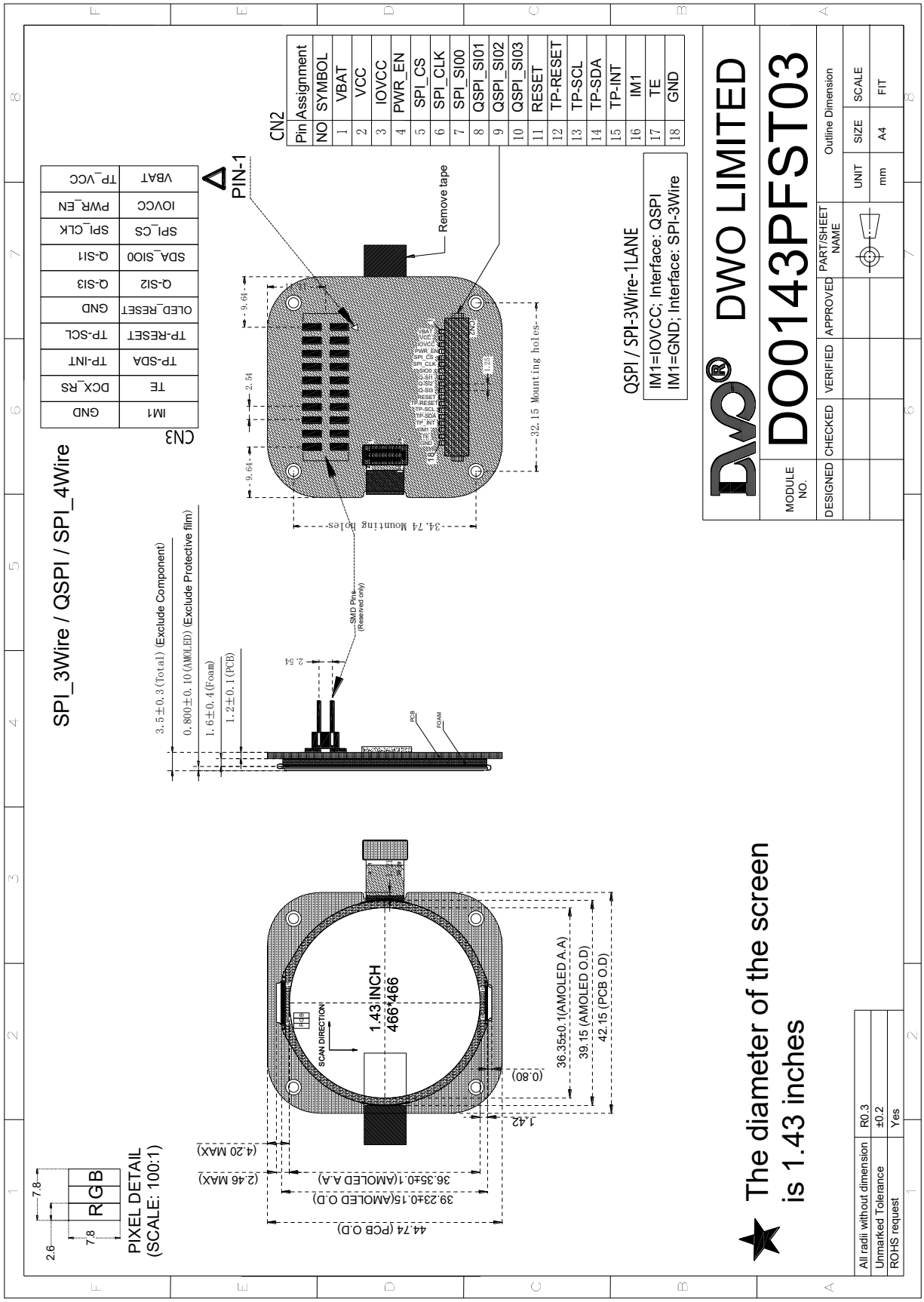
Item	Specifications	Unit
MODULE Dimensional outline(X*Y)	42.15(W) * 44.74 (H)*Thickness	mm
AMOLED Dimensional outline(X*Y)	39.15(W) * 39.23 (H)*0.8	mm
Thickness	Total 3.5(T) --- AMOLED=0.8mm; --- Foam=1.5mm; --- PCB=1.2mm	mm
Number of dots	466(W) x RGB x 466(H)	Dots
Active area	36.35(W) x 36.35(H)	mm
Pixel Size	78.0*78.0	um
Diameter Inch	1.43	inch
Frame rate	45@16.7M color /60@65K color	Hz

***See attached drawing for details.**

3.Block Diagram



4.Dimension


DWO LIMITED
DO0143PFST03
Outline Dimension
MODULE NO.
DESIGNED
CHECKED
VERIFIED
APPROVED
PART/SHEET NAME
UNIT
mm
SIZE
A4
SCALE
FIT
CN2
Pin Assignment
NO SYMBOL
1 VBAT
2 VCC
3 IOVCC
4 PWR_EN
5 SPI_CS
6 SPI_CLK
7 SPI_SI00
8 QSPI_SI01
9 QSPI_SI02
10 QSPI_SI03
11 RESET
12 TP-RESET
13 TP-SCL
14 TP-SDA
15 TP-INT
16 IM1
17 TE
18 GND
CN3
VBAT TP_VCC
IOVCC PWR_EN
SPI_CS SPI_CLK
SDA_SIO0 Q-SI1
Q-SI2 Q-SI3
OLED_RESET GND
TP-RESET TP-SCL
TP-SDA TP-INT
TE DCX_RS
IM1 GND
PIN-1
Remove tape
32.15 Mounting holes
34.74 Mounting holes
QSPI / SPI-3Wire-1LANE
IM1=IOVCC; Interface: QSPI
IM1=GND; Interface: SPI-3Wire
SPI_3Wire / QSPI / SPI_4Wire
3.5±0.3 (Total) (Exclude Component)
0.800±0.10 (AMOLED) (Exclude Protective film)
1.6±0.4 (Foam)
1.2±0.1 (PCB)
2.54
SMD Pins (Reserved only)
PCB
FOAM
1.43 INCH
466*466
SCAN DIRECTION
36.35±0.1(AMOLED A.A)
39.15 (AMOLED O.D)
42.15 (PCB O.D)
(0.80)
1.42
(4.20 MAX)
(2.46 MAX)
36.35±0.1(AMOLED A.A)
39.23±0.15(AMOLED O.D)
44.74 (PCB O.D)
PIXEL DETAIL
(SCALE: 100:1)
RGB
7.8
7.8
2.6
The diameter of the screen is 1.43 inches
All radii without dimension R0.3
Unmarked Tolerance ±0.2
ROHS request Yes

5.Pin Description

CN2

NO.	Pin Name	I/O	Description
1	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)
2	VCC	P	Power supply for display driver IC analog system.
3	IOVCC	P	Power supply for display driver IC interface and logic system
4	PWR_EN	I	Power IC enable control pin.
5	SPI_CS	I	Chip select input pin (“Low” enable)
6	SPI_CLK	I	SCL: A synchronous clock signal in SPI I/F.
7	SIO0	I/O	Serial Data Input input & output in QSPI,data Lane 0
8	Q-SI1	I	Serial Data Input in QSPI,data Lane 1
9	Q-SI2	I	Serial Data Input in QSPI,data Lane 2
10	Q-SI3	I	Serial Data Input in QSPI,data Lane 3
11	SPI_RESET	I	Display driver reset, must be applied to properly initialize the chip. Signal is active low.
12	TP_RESET	I	TP driver reset. Signal is active low.
13	TP-SCL	I	Touch Panel Clock Input. Communication Voltage follow IOVCC If not used, please open this pin.
14	TP_SDA	I/O	Touch Panel Data Input and output. Communication Voltage follow IOVCC If not used, , please open this pin.
15	TP-INT	O	Touch Panel Interrupt Output. If not used, please open this pin.
16	IM1	I	Dsipaly Interface type selection; When IM=1: Dsipaly Interface type is QSPI; When IM=0: Dsipaly Interface type is SPI-3Wire;
17	TE	O	Tearing Effect
18	GND	P	Ground

6. DC Characteristics

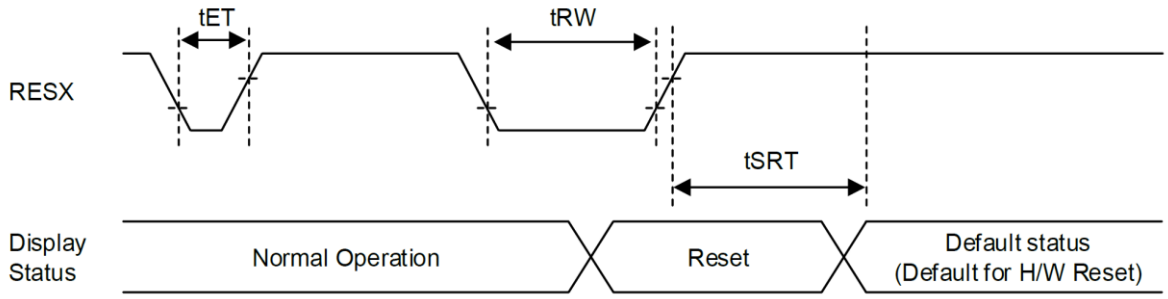
Test Conditions :Voltage Referenced to GND=VSS=0V, VCCC=3.3V,IOVCC = 1.8 V,TA = 25℃
Unless otherwise specified

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage		IOVCC	-	1.72	1.8	3.4	V
		VCC	-	2.7	3.3	3.36	
		VBAT	-	2.9	3.8	4.5	
Input Voltage	"H" level	VIH	-	0.8*IOVCC	-	IOVCC	V
	"L" level	VIL	-	-0.2	-	0.2*IOVCC	
Output Voltage	"H" level	VOH	IOH = -0.1mA IOL = 0.1mA	0.8*IOVCC	-	IOVCC	V
	"L" level	VOL		-0.2	-	0.2*IOVCC	
Leakage Current	Input	ILI	Vin=IOVCC or VSS	-1.0	-	1.0	uA
	Output	ILO		-3.0	-	3.0	uA
Current (Display)	Sleep out mode	I_{VCC}	Full white display, 350nits,	-	13	19.5	mA
		I_{IOVCC}		-	1.5	3	mA
		I_{VBAT}		-	55	95	mA
	Sleep in mode	I_{VCC}		-	20	50	uA
		I_{IOVCC}		-	50	100	uA
		I_{VBAT}		-	50	100	uA
	Deep Standby Mode	I_{VCC}		-	2	4	uA
		I_{IOVCC}		-	2	4	uA
		I_{VBAT}		-	50	-	uA
Frame Frequency		f_{FRM}		-	45	-	Hz

7.AC characteristics

7-1 Reset Timing

Reset timing characteristic



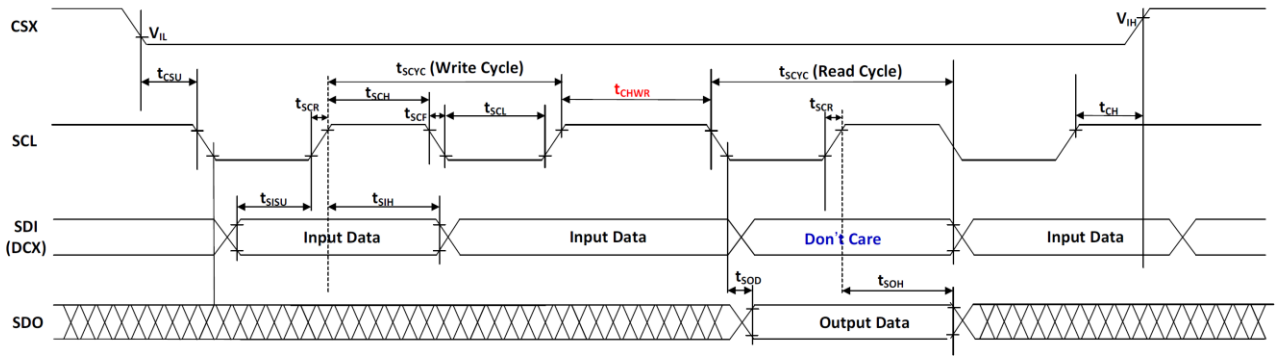
VSS=0V, VDDIO=1.72V to 3.3V, VCI=2.5V to 3.3V,Ta = -30 to 70℃

Parameter	Symbol	Pad	Min.	Typ.	Max.	Unit	Note
Reset low pulse width	tRW	RESX	10	–	–	μs	–
Secure reset completion time	tSRT	RESX	–	–	5	ms	Reset during Sleep In mode
		RESX	–	–	150		Reset during Sleep Out mode
Reset un-reacted pulse width	tET	RESX			5	μs	–

7-2 SPI Timing

SPI-3Wire/ SPI-4Wire Interface Characteristics

3/4-wire SPI



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCYC}	Write	20			ns
		Read	300			ns
Clock high pulse width	t_{SCH}	Write	6.5			ns
	t_{SCH}	Read	140			ns
Clock low pulse width	t_{SCL}	Write	6.5			ns
	t_{SCL}	Read	140			ns
Clock rise time	t_{SCR}	0.2*VDDI -> 0.8*VDDI			3.5	ns
Clock fall time	t_{SCF}	0.8*VDDI -> 0.2*VDDI			3.5	ns
Chip select setup time	t_{CSU}		10			ns
Chip select hold time	t_{CH}		10			ns
Data input setup time	t_{SISU}	To V_{IL} of SCL's rising edge	5			ns
Data input hold time	t_{SIH}		5			ns
Access time of output data	t_{SOD}	From V_{IL} of SCL's falling edge			120	ns
Hold time of output data	t_{SOH}	From V_{IH} of SCL's rising edge	5			ns
Transition time from Write cycle to Read cycle	t_{CHWR}	From V_{IH} of SCL's rising edge	150			ns

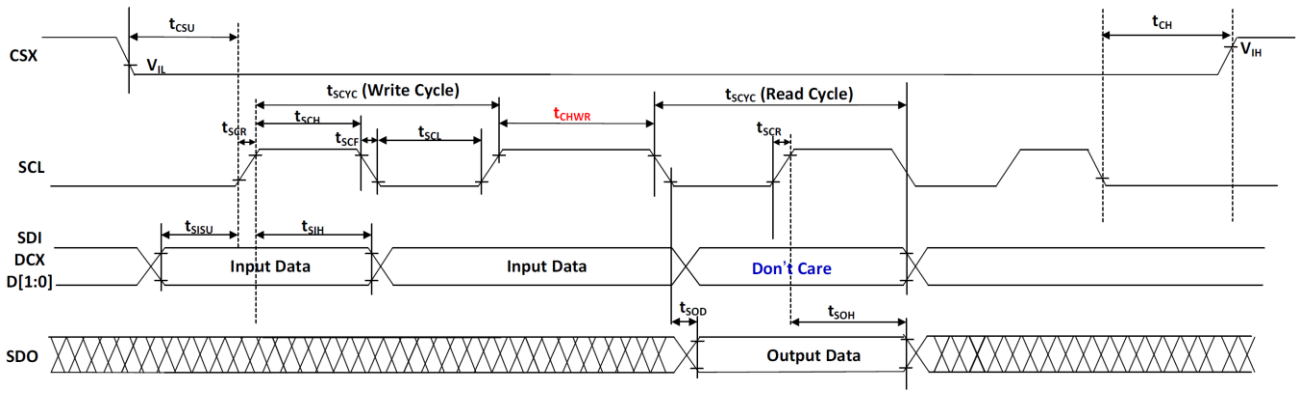
Notes:

(1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.

(2) For the 4-wire SPI, the DCX's timing is the same as input data.

(3) Ta = -30°C to 70°C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, and VSS=0V

7-3 QSPI Interface Characteristics



Note: The max SCL frequency for each pixel data format is specified as the below table.

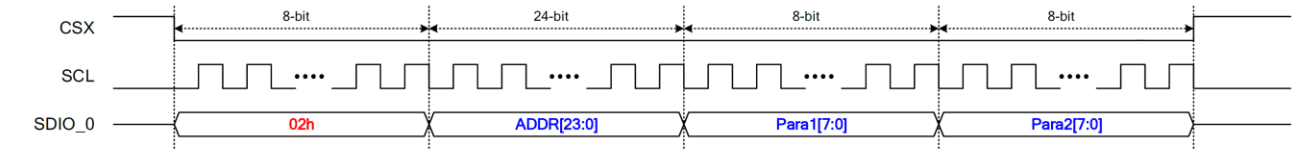
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V

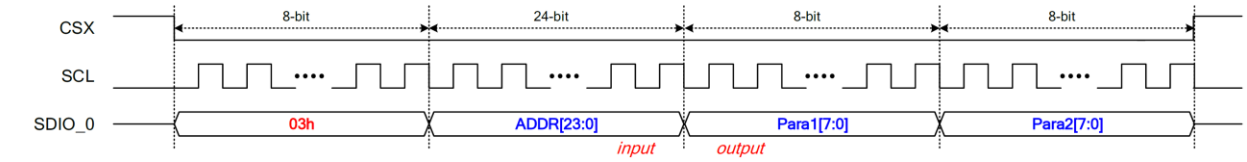
QSPI Timing

Quad SPI Interface Protocol – Register Read and Write

Command Write

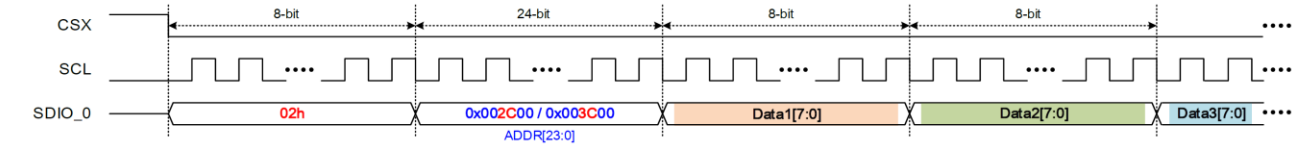


Command Read

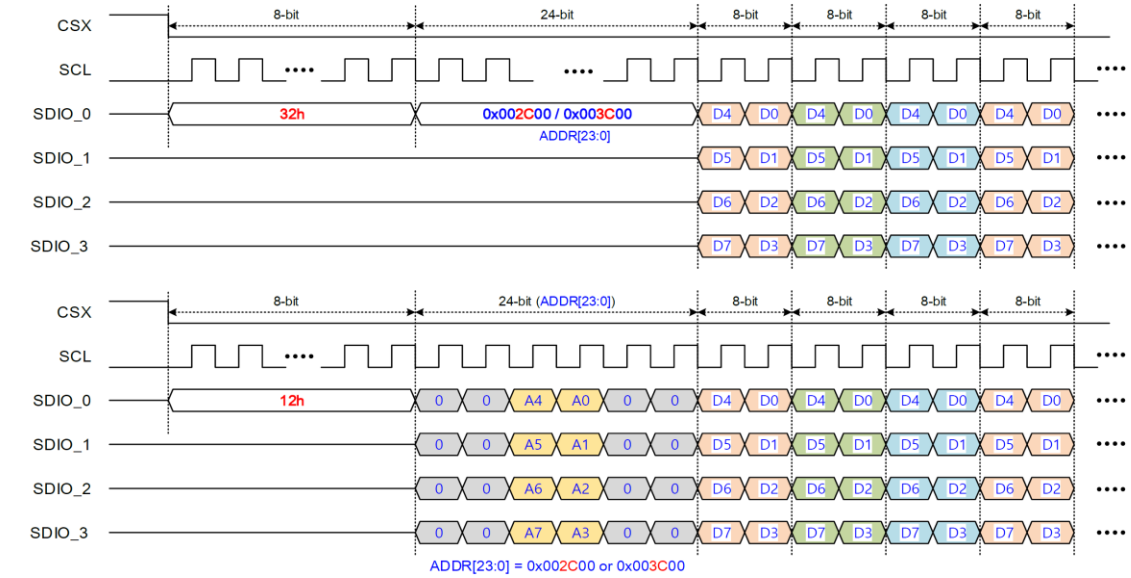


Quad SPI Interface Protocol – Pixel Interface

1-Wire Pixel Write

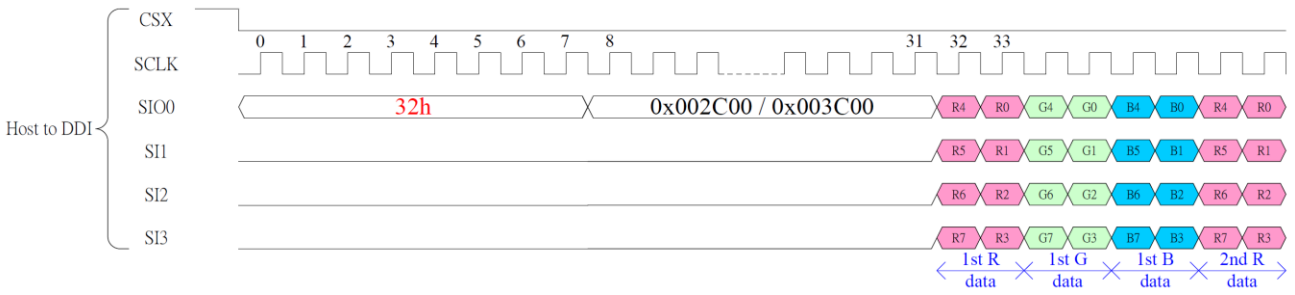


4-Wire Pixel Write

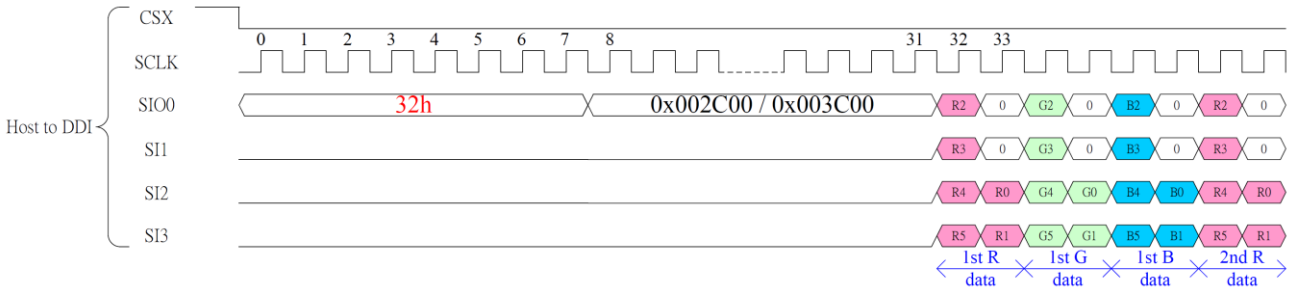


SPI-4Lanes Pixel Write Data Waveform

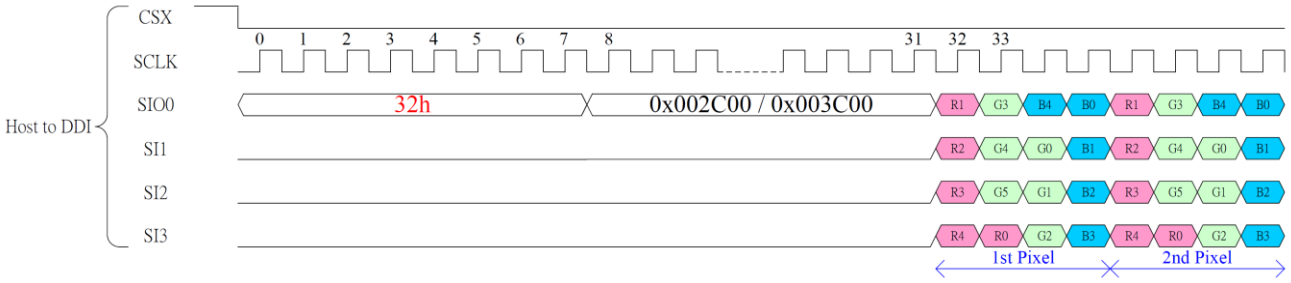
RGB888 – 4-Lanes



RGB666 – 4-Lanes

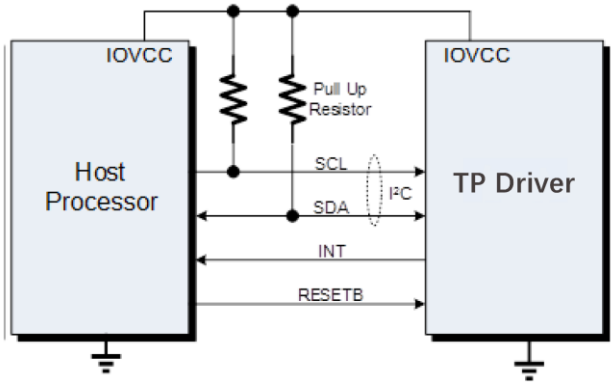


RGB565 – 4-Lanes

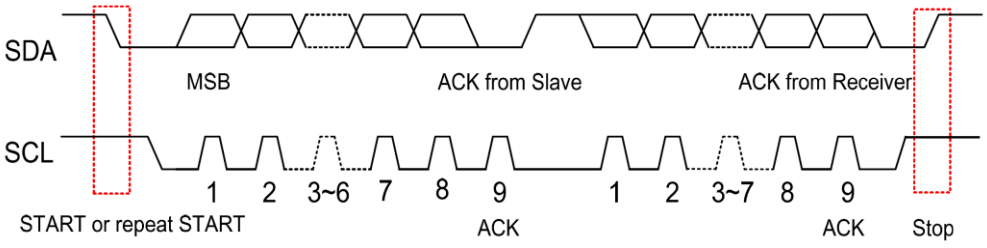


7-5 Touch Panel(TP) IIC Timing Characteristics

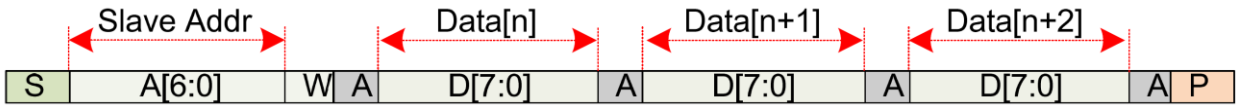
The TP driver communicates to the host through the IIC interface and follows the IIC protocol. IIC bus utilize the SCL and SDA, a two-wire synchronous communication interface and can operate at a maximum bit rate of 400kbps.



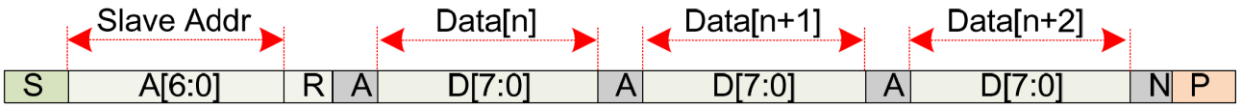
IIC Serial Data Transfer Format



IIC Interface Timing



IIC Master Write, Slave Read



IIC Master Read, Slave Write

TP Driver IC Slave Addr A[6:0]---0X38

Mnemonics	Description
S	I^2C Start or I^2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

IIC Timing Characteristics

Parameter	Standard Mode		Fast Mode		Unit
	Min	Max	Min	Max	
SCL frequency (fast mode support)	0	100	0	400	KHz
Clock low period	4.7	-	1.3	-	us
Clock high period	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	4.7	-	1.3	-	us
Hold time (repeated) START condition	4.0	-	0.6	-	us
Data setup time	250	-	100	-	ns
Setup time for a repeated START condition	4.7	-	0.6	-	us
Setup Time for STOP condition	4.0	-	0.6	-	us

TP I/O Communication Voltage follow IOVCC

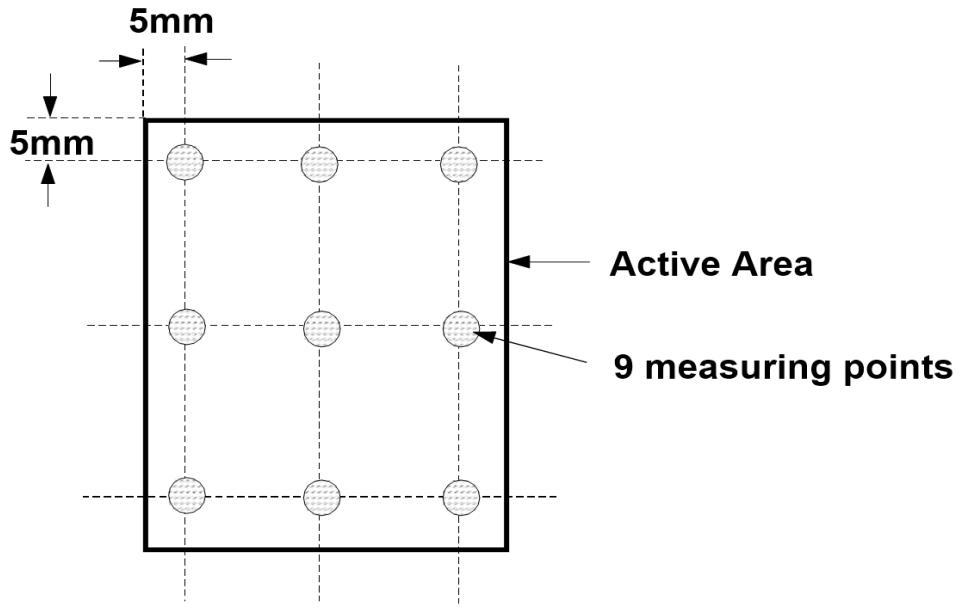
TP DC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 × IOVCC	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	0.3 × IOVCC	V	
Output high -level voltage	VOH	IOH=－0.1mA	0.7 × IOVCC	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	0.3 × IOVCC	V	
I/O leakage current	ILI	Vin=0~AVDD	-1	-	1	μA	
Current consumption （Normal operation mode）	Iopr	AVDD=2.8V Ta=25℃ MCLK=15MHz	-	1.5	-	mA	
Current consumption （Monitor mode）	Imon	AVDD=2.8V Ta=25℃ MCLK=15MHz	-	30	-	μA	
Current consumption （Sleep mode）	Islp	AVDD=2.8V Ta=25℃	-	10	-	μA	
Power Supply voltage	AVDD		2.8	-	3.6	V	

8.Electro-optical characteristics

Item		Symbol	Temp	Condition	Min.	Typ.	Max.	Unit	Note
Brightness			25℃	Normal (White Mode)	300	350	400	cd/m²	Center brightness
Uniformity			25℃	Normal (White Mode)	85	90	-	%	(1)
Contrast ratio		K	25℃	Φ=0°,θ=0°	60,000		-	-	(1),(2)
Color of CIE coordinate	White	x	25℃	Φ=0° θ=0°	0.275	0.295	0.315	-	(1),(2),(3)
		y			0.295	0.315	0.335	-	
	Red	x			0.630	0.660	0.690	-	
		y			0.310	0.340	0.370	-	
	Green	x			0.170	0.220	0.270	-	
		y			0.680	0.730	0.780	-	
	Blue	x			0.115	0.140	0.165	-	
		y			0.025	0.050	0.075	-	
Color Gamut			25℃	vs. NTSC	85	100	-	%	
Life Time(5)			25℃	50% Brightness drop @250cd/m², Full White	-	30,000	-	Hr	(4)

Note 1): Uniformity Measuring Point

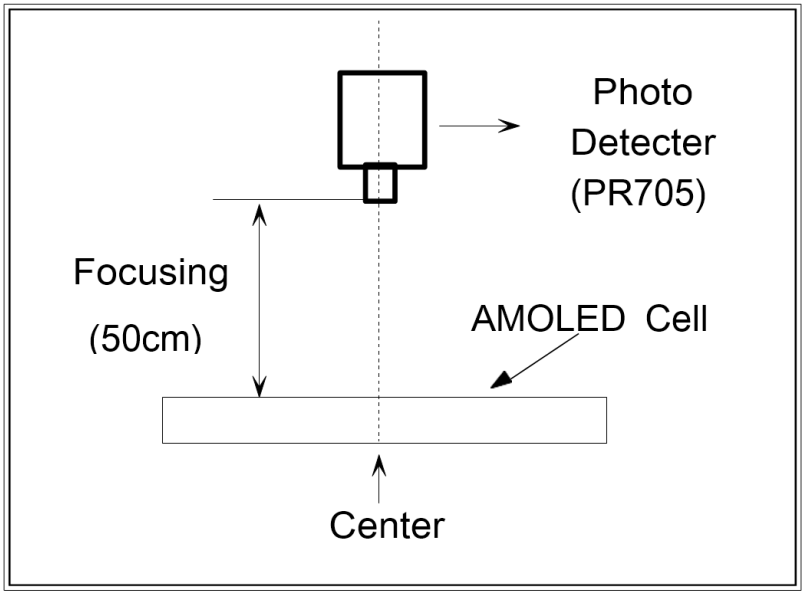


Uniformity = Lmin / Lmax * 100 [%]

Note 2): Definition of contrast ratio (K)

$$\text{Contrast Ratio(K)} = \frac{\text{Brightness of selected dot (White patterned area) at 250cd/m}^2}{\text{Brightness of non-selected dot (Black patterned area) at 250cd/m}^2}$$

Note 3): Optical measuring system： temperature regulated chamber



Note 4): Life Time

The elapsed time that the full white brightness decreases to the half of initial value

9.Recommended Operating Sequence

Please refer to “DO0143PFST03_Demo_Code.c”

10. Standard Specification For Reliability

No	Item	Condition	Cycles	Judgment Criterion
1	High Temperature Operation	80℃/ 240hours	10	1. No clearly visible defects or remarkable deterioration of display quality.However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted. 2. No function-related abnormalities.
2	Low Temperature Operation	-30℃/ 240hours	10	
3	High Temperature Storage	85℃/ 240hours	5	
4	Low Temperature Storage	-40℃/ 240hours	5	
5	High Temperature Humidity Operation	60℃/90%RH/ 240hours	5	
6	Thermal Shock	-40℃~85℃ / 100cycles	5	

Note: The results must be measured after 2 hours later under room temperature keeping.

- END -