

Product Specification

❖ **Product Name: AMOLED**

❖ **Model Name: DO0200FAT07**

❖ **Description: 1.91 inch (240x536)**

Proposed by			Customer's Approval
Designed	Checked	Approved	

Document Revision History

Rev. No.	Date	Contents	Remark
0.0	2023-08-15	-.Initial issue	Preliminary
0.1	2024-05-14	-.Modify Size Description	

1.General Description:

- Driving Mode: Active Matrix.
- Color Mode: 16.7M/262K/65K color
- Display Format: 1.91" (240RGB x 536)
- Pixel arrangement: Real RGB arrangement
- Display Driver IC : RM67162 or Compatible
- Touch Driver IC : FT3168 or Compatible
- Interface: SPI-3Wire / SPI-4Wire / i8080-8Bits / QSPI / MIPI-1Lane
- Application: Handheld & PDA & Wearable
- RoHS Compatible

2.Mechanical Data

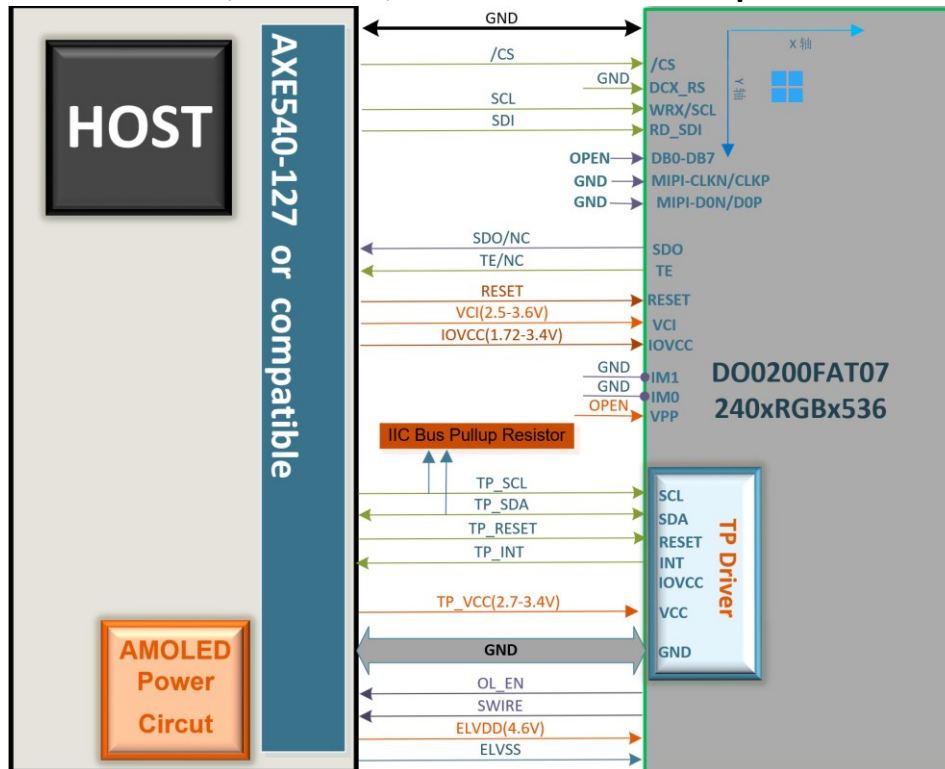
Item	Specifications	Unit
Dimensional outline [With Cover Lens]	33.57(W) x41.2(H) x Thickness	mm
Thickness	2.09(Total) --- 0.7 (COVER LENS) --- 0.25 (Film + OCA) --- 0.85 (AMOLED)	mm
Number of dots	240(W) x RGB x 536(H)	Dots
Active area	19.80(W) x 44.22(H)	mm
Diagonal Inch	1.91	inch

***See attached drawing for details.**

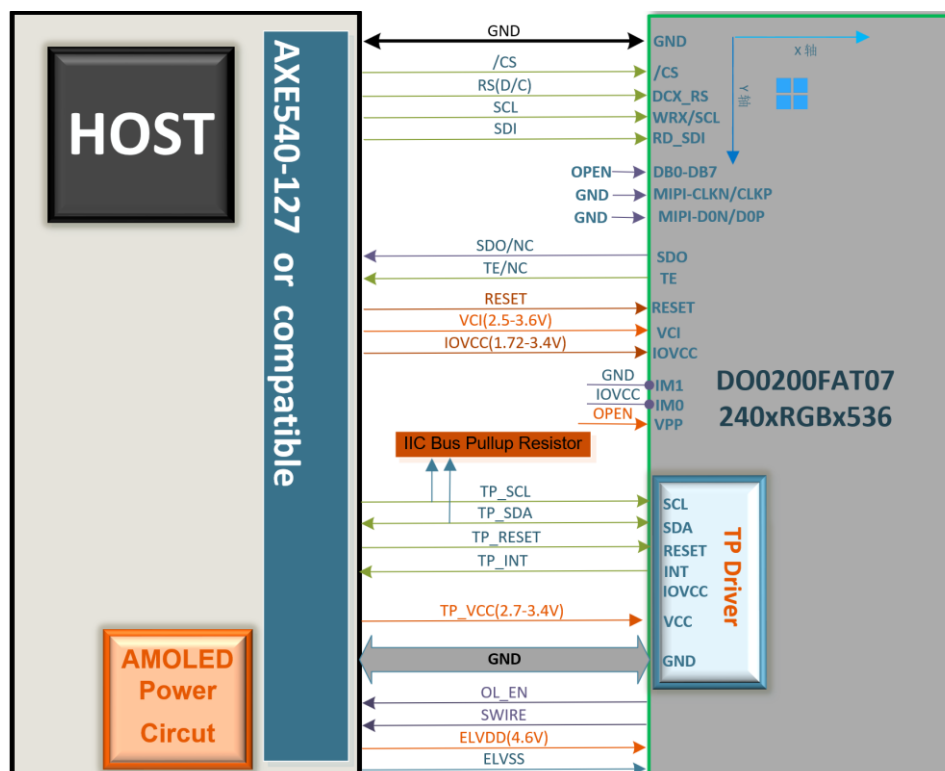
3. Block Diagram

DO0200FAT07 support various interfaces, and interfaces are selected by setting the IM[1:0] pins.

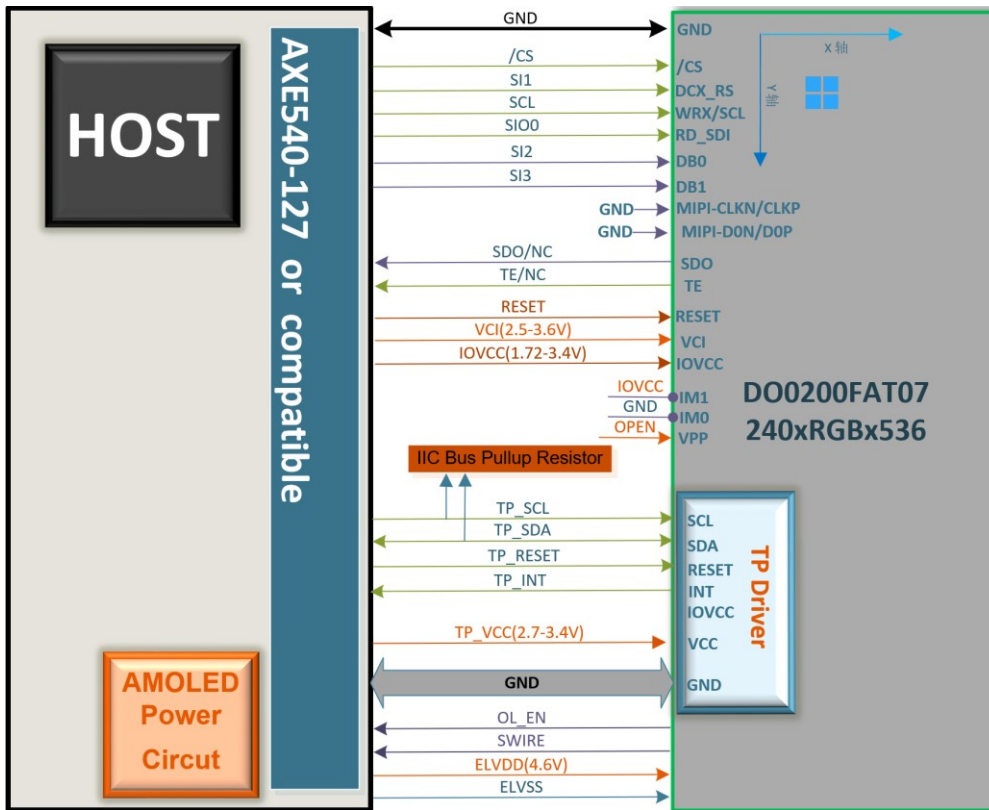
A: If IM1=GND, IM0=GND, DO0200FAT07 set to **spi-3wire interface**



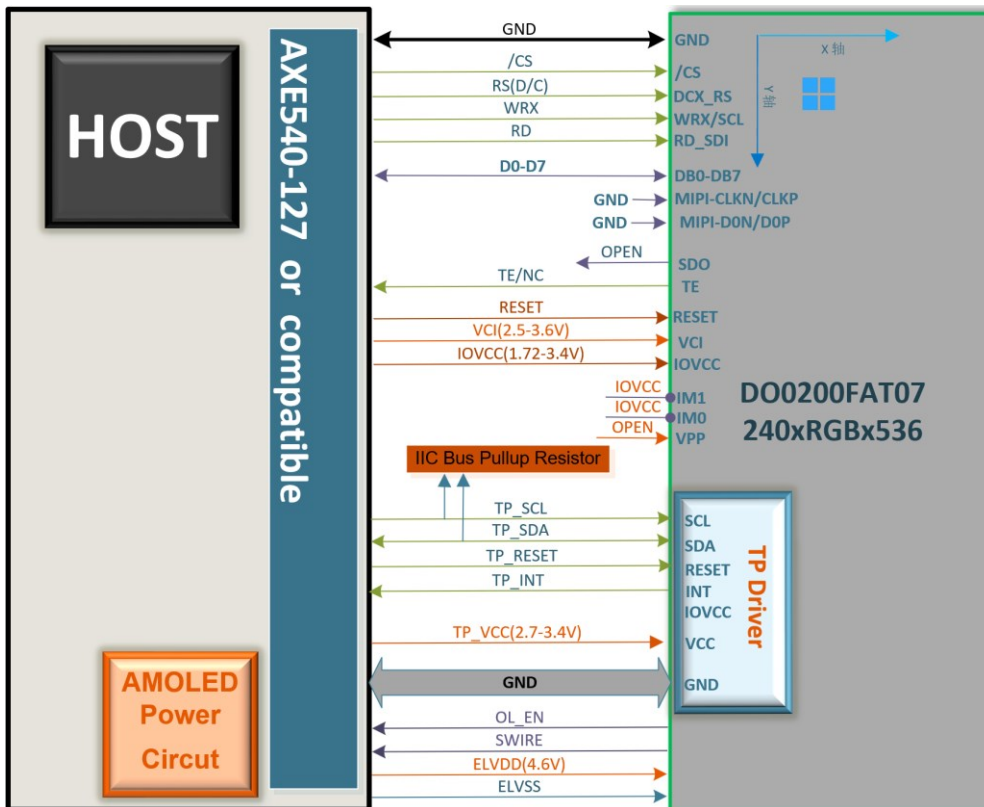
B: If IM1=GND, IM0=IOVCC, DO0200FAT07 set to **spi-4wire interface**



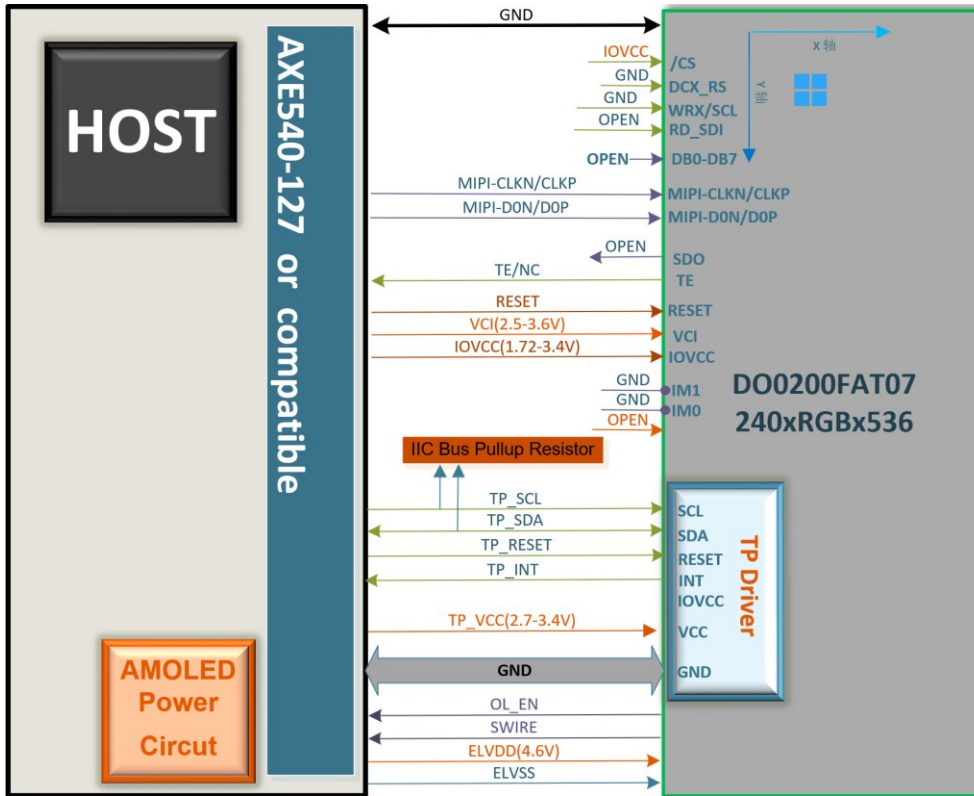
C: If IM1=IOVCC,IM0=GND, DO0200FAT07 set to **QSPI** interface



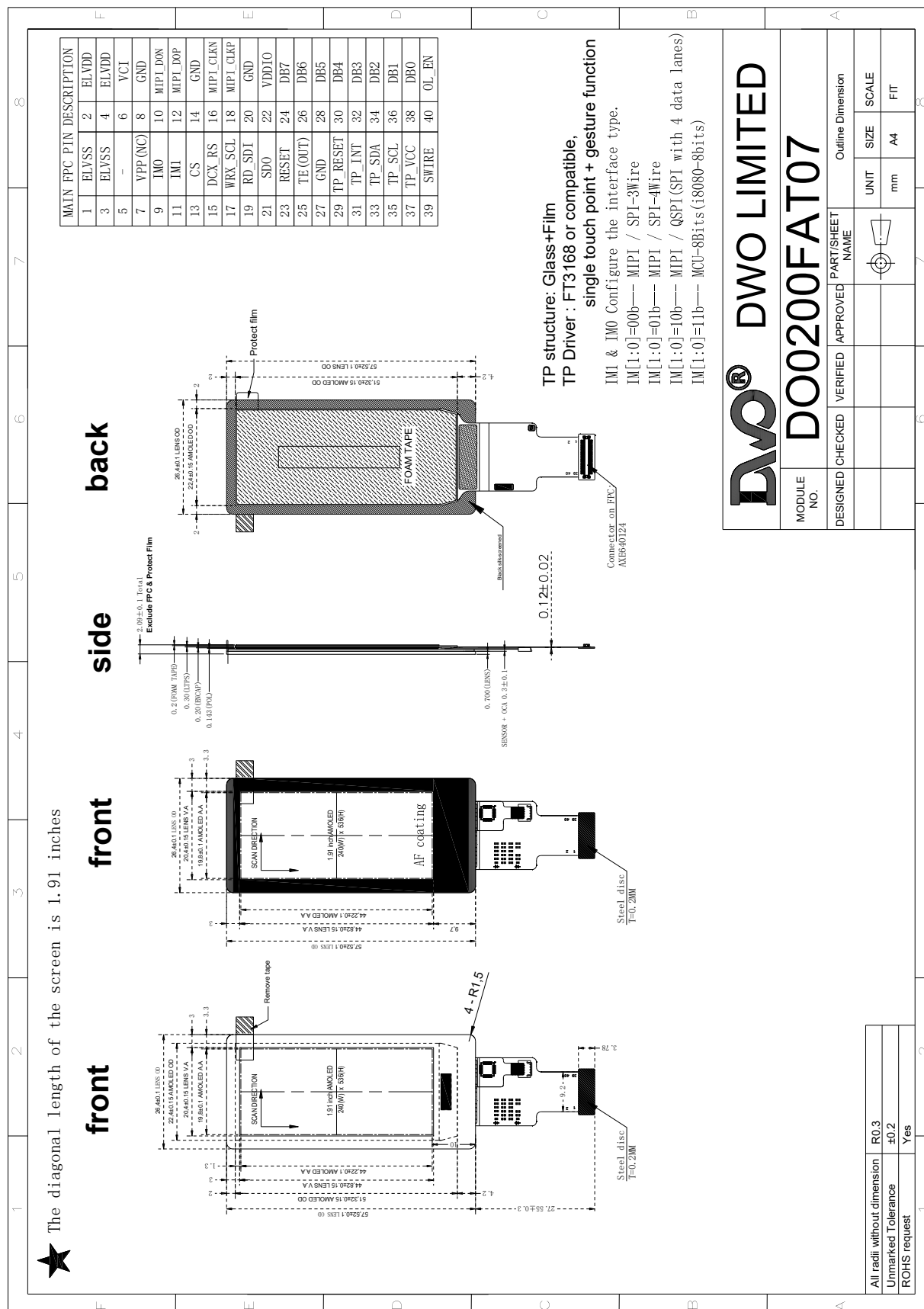
D: If IM1=IOVCC,IM0=IOVCC, DO0200FAT07 set to **i8080-8bits** interface



E: If IM1=GND, IM0=GND, and CS=IOVCC, DO0200FAT07 set to **MIPI-DSI** interface



★ The diagonal length of the screen is 1.91 inches



5.Pin Description

NO.	Pin Name	I/O	Description
1	ELVSS	P	AMOLED power negative
3	ELVSS	P	
5	NC	-	No connect
7	VPP	P	OTP Power Supply(Let it open)
9	IM0	I	Interface type selection
11	IM1	I	Interface type selection
13	CS	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F.
15	DCX_RS	I	Display data / command selection in 80-series MPU I/F and SPI 4-wire I/F. D/CX = "0" : Command; D/CX = "1" : Display data or Parameter
17	WRX_SCL	I	WRX : Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F.
19	RD_SDI	I	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. RDX : Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface.
21	SDO	O	Serial output signal in SPI I/F.
23	RESET	I	AMOLED Reset signal Input
25	TE	O	Tearing Effect
27	GND	P	Ground Terminal
29	TP_RESET	I	TP Reset signal Input Communication Voltage follow IOVCC
31	TP_INT	O	Touch Panel Interrupt Output. Communication Voltage follow IOVCC If not used, please open this pin.
33	TP_SDA	I/O	Touch Panel Data Input. Communication Voltage follow IOVCC If not used, please open this pin.
35	TP_SCL	I	Touch Panel Clock Input. Communication Voltage follow IOVCC If not used, please open this pin.
37	TP_VCC	P	Analog Voltage for TP Driver (2.7~3.4V)
39	SWIRE	O	Swire protocol setting pin of Power IC
NO.	Pin Name	I/O	Description
2	ELVDD	P	AMOLED power positive
4	ELVDD	P	
6	VCI	P	Analog Voltage for Driver (2.7~3.4V)
8	GND	P	Ground Terminal

10	MIPI_D0N	I/O	Differential data signals if MIPI interface. If not used, please connect these pins to GND.
12	MIPI_D0P	I/O	Differential data signals if MIPI interface. If not used, please connect these pins to GND.
14	GND	P	Tearing Effect
16	MIPI_CLKN	I	Differential clock signals if MIPI interface. If not used, please connect these pins to GND.
18	MIPI_CLKP	I	Differential clock signals if MIPI interface. If not used, please connect these pins to GND.
20	GND	P	Ground Terminal
22	IOVCC	P	Driver IC Digital I/O Power Supply(1.7~3.3V)
24	DB7	I/O	Bi-directional data bus for 80-series MPU I/F [MSB]
26	DB6	I/O	Bi-directional data bus for 80-series MPU I/F
28	DB5	I/O	Bi-directional data bus for 80-series MPU I/F
30	DB4	I/O	Bi-directional data bus for 80-series MPU I/F
32	DB3	I/O	Bi-directional data bus for 80-series MPU I/F
34	DB2	I/O	Bi-directional data bus for 80-series MPU I/F
36	DB1	I/O	Bi-directional data bus for 80-series MPU I/F
38	DB0	I/O	Bi-directional data bus for 80-series MPU I/F [LSB]
40	OL_EN	O	Power IC enable control pin

6. DC Characteristics

6.1 DC Characteristics Requirements

Item	Symbol	Values			Unit	Remark
		Min	Type	max		
Analog power supply Vo	VCI	2.7	3.3	3.6	V	
I/O Supply Voltage	VDDIO	1.7	1.8	3.4	V	
OLED input voltage	ELVDD	4.55	4.6	4.65	V	
OLED input voltage	ELVSS	-5.2	-4.0	-2.0	V	
Input High Voltage	VIH	0.8*VDDI	--	VDDI	V	
Input Low Voltage	VIL	0	--	0.2*VDDI	V	
Output High Voltage	VOH	0.8*VDDI	--	VDDI	V	
Output Low Voltage	VOL	0	--	0.2*VDDI	V	

6.2 Power Consumption of Display Power Supply: IOVCC=1.8V, VCI=3.3V;

Item		Symbol		Condition	Symbol	Min.	Typ.	Max.	Uni	Remark	
ELVDD		ELVDD		Normal	-	-	4.6	-	V	External Power	
ELVSS		ELVSS		Normal	-	-	-4.0	-	V		
VCI		VCI		Normal	-	-	3.3	-	V		
VDDIO		VDDIO		Normal	-	-	1.8	-	V		
Power Consumption	Display on mode (Normal)	Display IC	VCI	100% Pixel On,350nits, 60Hz	Ivci		12.0	15.0	mA		
			VDDIO		Ivddio		1.3	1.6	mA		
		Panel	EL		I _{ELVDD}		85		mA		
					I _{ELVSS}		TBD		mA		
Frame Rate		F _{frm}		-30°C~80°C	F _{frm}	55.2	60	64.8	Hz		
				25°C		58.2	60	61.8	Hz		

7. Electro-optical characteristics

Item		Symbol	Condition	Value			Unit	Remark
				Min	Typ	Max		
Luminance		L	θ=0° Φ=0° without CG	315	350	385	cd/m2	
Uniformity				85	90	-	%	Note 2
Viewing Angle	Left	θ _L	Cr≥200	80	85	-	Deg.	
	Right	θ _R		80	85	-		
	Top	ψ _T		80	85	-		
	Bottom	ψ _B		80	85	-		
Contrast Ratio		CR	θ=0°	5000	10000	-	-	
Adobe cover Ratio		SOR	ICE1931	-	100	-	%	Note 1
Response Time		Tr+Tf	Φ=0°	-	2	4	ms	
Color Coordinate of CIE1931	Red	X	θ=0° Φ=0°	0.64	0.67	0.70	-	
		Y		0.30	0.33	0.36		
	Green	X		0.17	0.21	0.25		
		Y		0.69	0.73	0.77		
	Blue	X		0.11	0.14	0.17		
		Y		0.01	0.04	0.07		
	White	X		0.28	0.30	0.32		
		Y		0.29	0.31	0.33		
NTSC Ratio		NTSC	CIE1931	100	103	-	%	
Color Uniformity		Δ u′	θ=0 deg. Condition 1	-	-	0.007	Δ u′	Note 2
		Δ v′				0.007	Δ u′	
Flicker		-	60Hz, Worst pattern	-	-30	-	dB	
Gamma		-	θ=0 deg.	2.0	2.2	2.4		
Crosstalk			-	-	-	TBD	%	Note 3
Color temperature		CT		6700	7500	8300	K	
Luminance decrease ratio of full white			θL=30°		40	45	%	
			θR=30°		40	45	%	
			ψT=30°		40	45	%	
			ψB=30°		40	45	%	
White color shift		WAD	G255, 0 to 45 deg.	-	-	0.022	Δ u′v′	Note 4

Measurements condition as below, if not otherwise specified. Include touchpanel, OCA and Cover glass

Room temp: 25°C, Frame frequency=60Hz

Image Enhancement :OFF

Measurement points: Display center, $\theta=0$ deg.

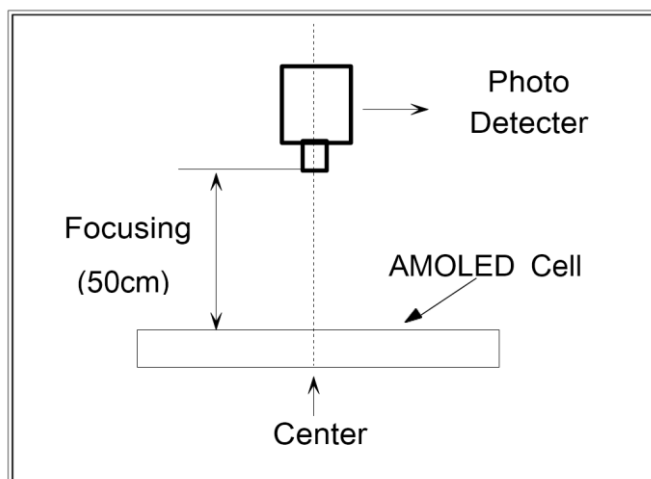
Measurement instrument: Uniformity CA2500,

Flicker CA310 or equivalent device. Other items CS2000

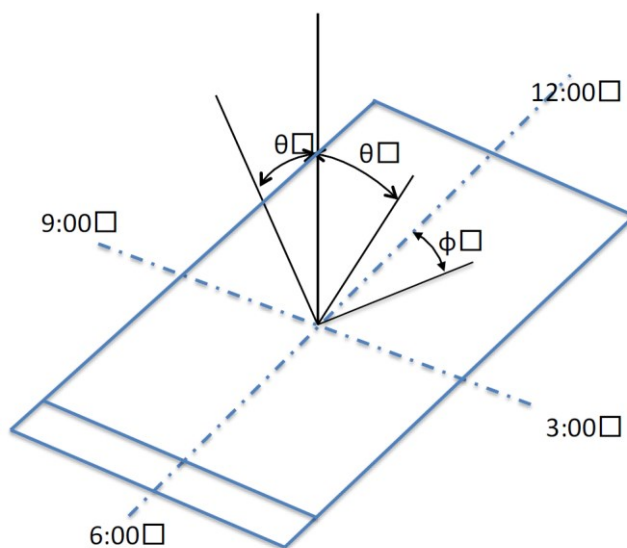
CS2000: To be measured on the center area of Panel with a viewing cone of 1° by luminance mater, after 15min operation

CA2500: To be measured on the Active area of Panel with a viewing cone of 35pixel/circle by luminance mater, after 15min operation

CA310: To be measured on “CA-P32/35” Probe



Viewing angle



Note1: Define of Adobe cover ratio

Green: RGB color chromaticity of this module

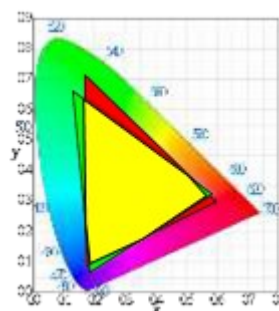
Rad : RGB color chromaticity of Adobe RGB

R: x0.64, y0.330

G: x0.21, y0.71

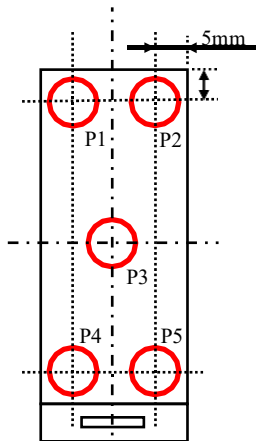
B: x0.15, y0.06

Yellow : The area where red and yellow are piled



$$\text{Adobe RGB cover Ratio} = \text{Yellow} / \text{Rad} * 100[\%]$$

Note2: Define of Brightness uniformity and Color uniformity



$$\text{Brightness uniformity} = \frac{\text{Minimum value}[P1:P5]}{\text{Maximum value}[P1:P5]}$$

$$\text{Color uniformity} = \text{Maximum value}[P1:P5] - \text{Minimum value}[P1:P5]$$

Note3: Define of Brightness uniformity and Color uniformity

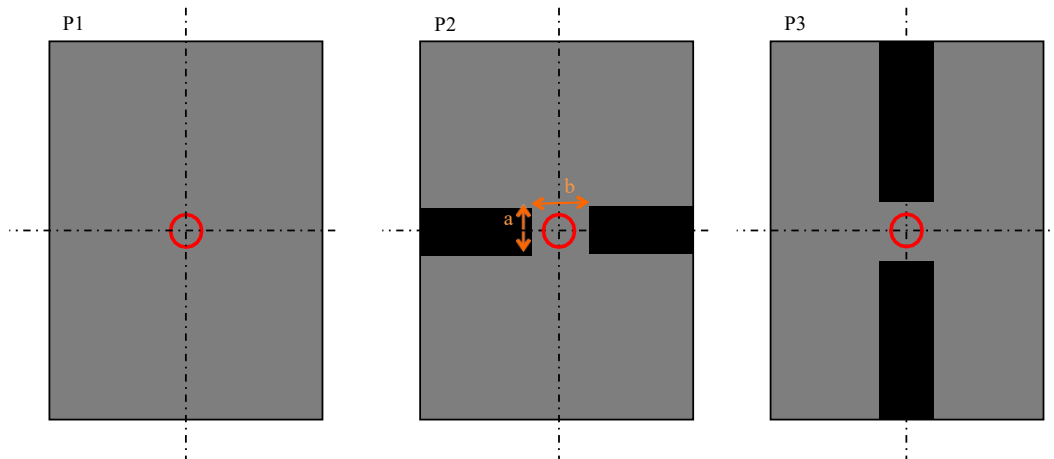
Define of crosstalk

Base color : V127

Measurement area (a,b) :

144dots*144dots Bar color :

white, red, green, blue, Black.



$$\text{Cross talk ratio P2} = \frac{|P1-P2|}{P1}$$

$$\text{Cross talk ratio P3} = \frac{|P1-P3|}{P1}$$

Cross talk ratio: maximum value of cross talk P2 and P3

Note4: Define of White color shift

White color shift is Maximum value of Color shift WADu' and Color shift WADv'

$$WADu' = |u'_{0} - u'_{45}|$$

$$WADv' = |v'_{0} - v'_{45}|$$

$$\Delta u'v' = \sqrt{WADu'^2 + WADv'^2}$$

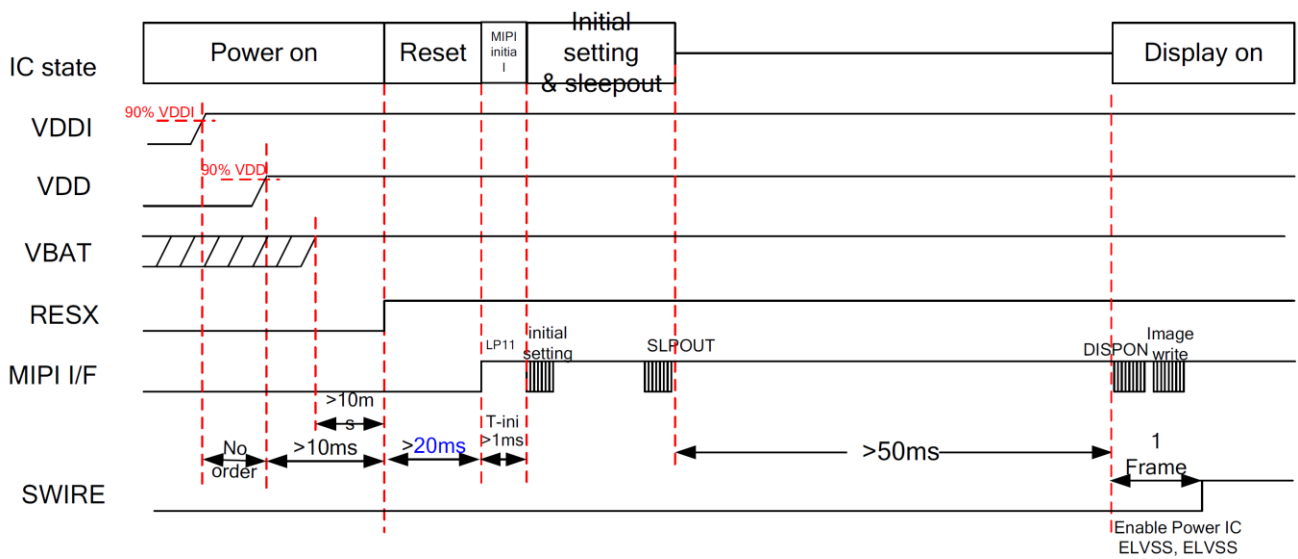
u'_{0}, v'_{0} : white color chromaticity at $\Theta = 0\text{deg}$

u'_{45}, v'_{45} : white color chromaticity at $\Theta = 45\text{deg}$ * (φ = all angle)

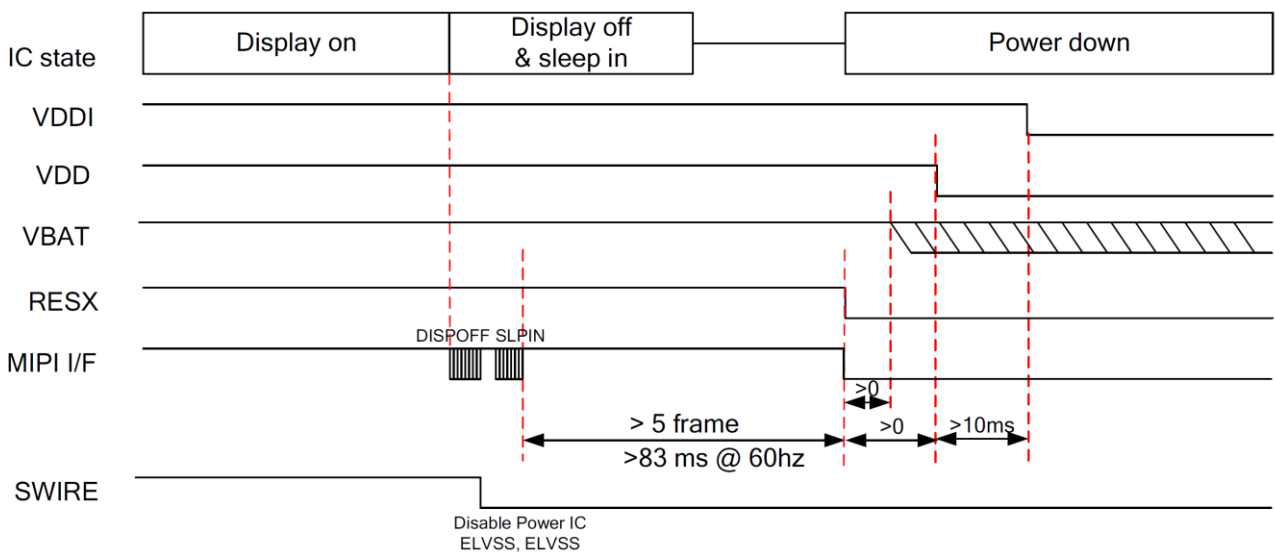
8. Recommended Operating Sequence

8.1 Power on/off sequence and timing

Power On sequence

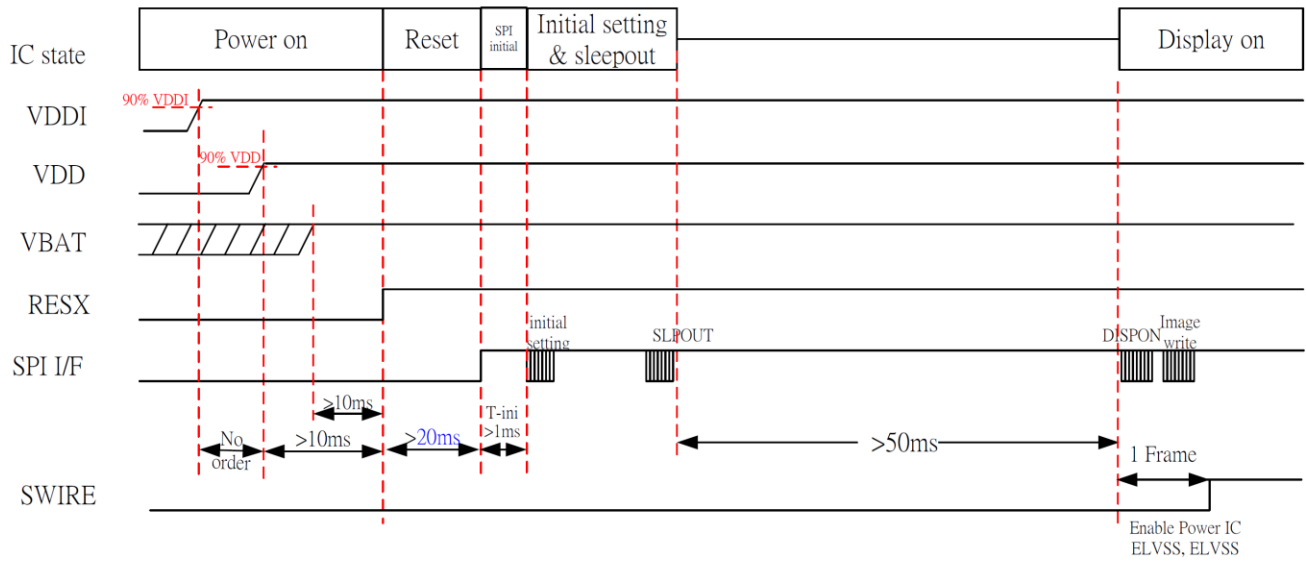


Power Off sequence



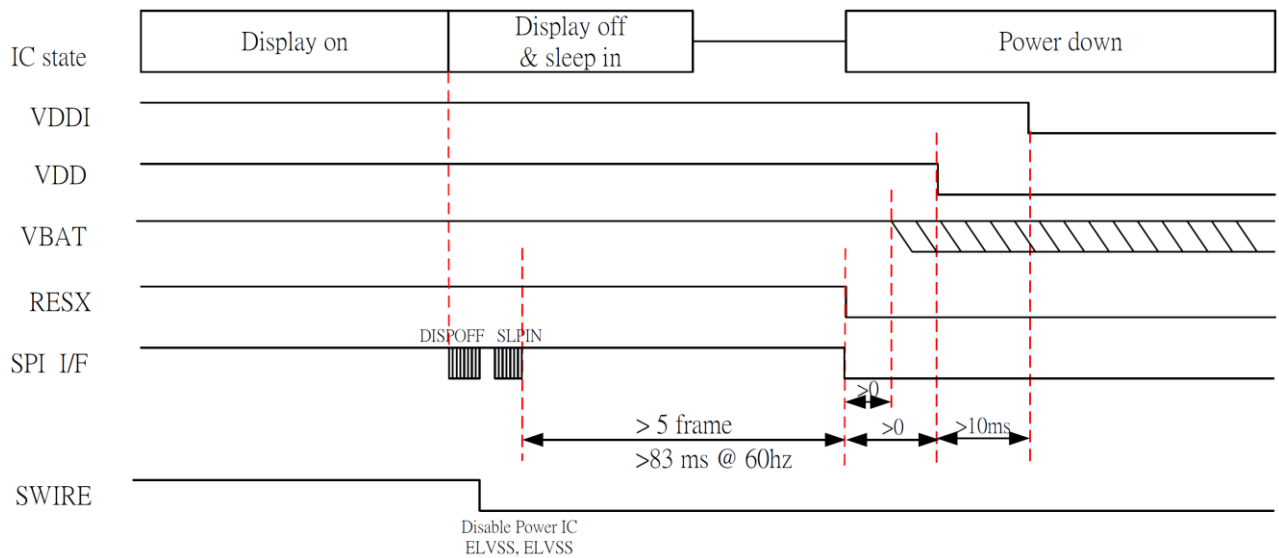
Power On sequence

SPI Interface



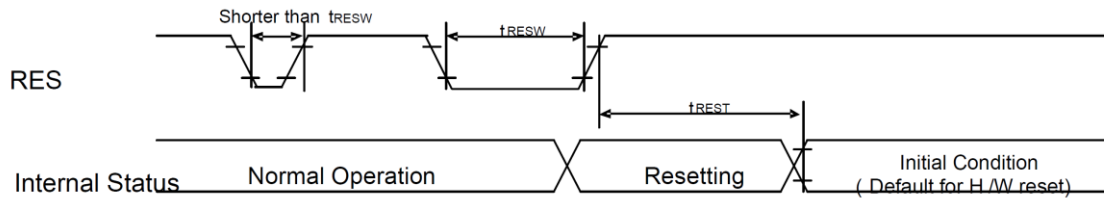
Power Off sequence

SPI Interface



9.AC characteristics

9.1 Reset Timing Sequence Requirement



Reset input timing:

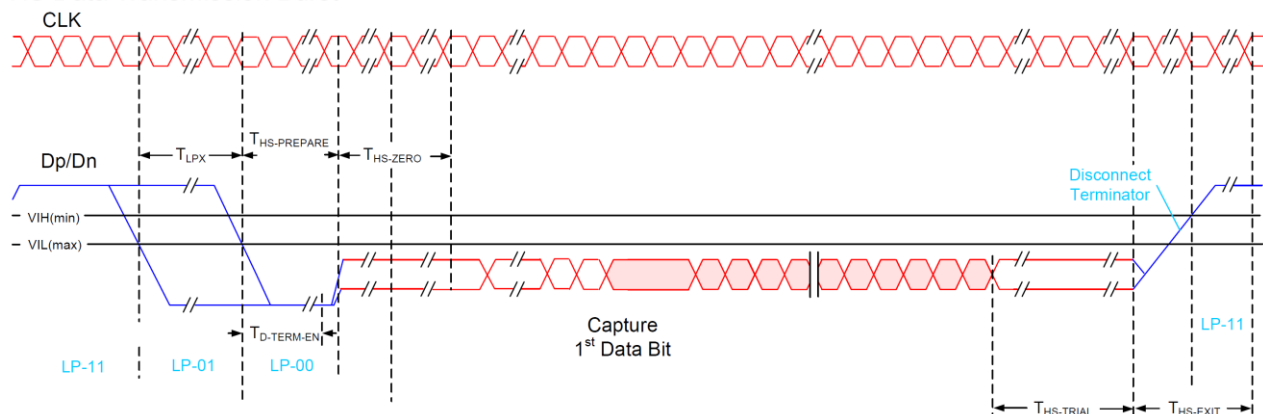
VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t _{RESW}	*1) Reset low pulse width	RESX	30	-	-	-	μs
t _{REST}	*2) Reset complete time	-	-	-	20	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

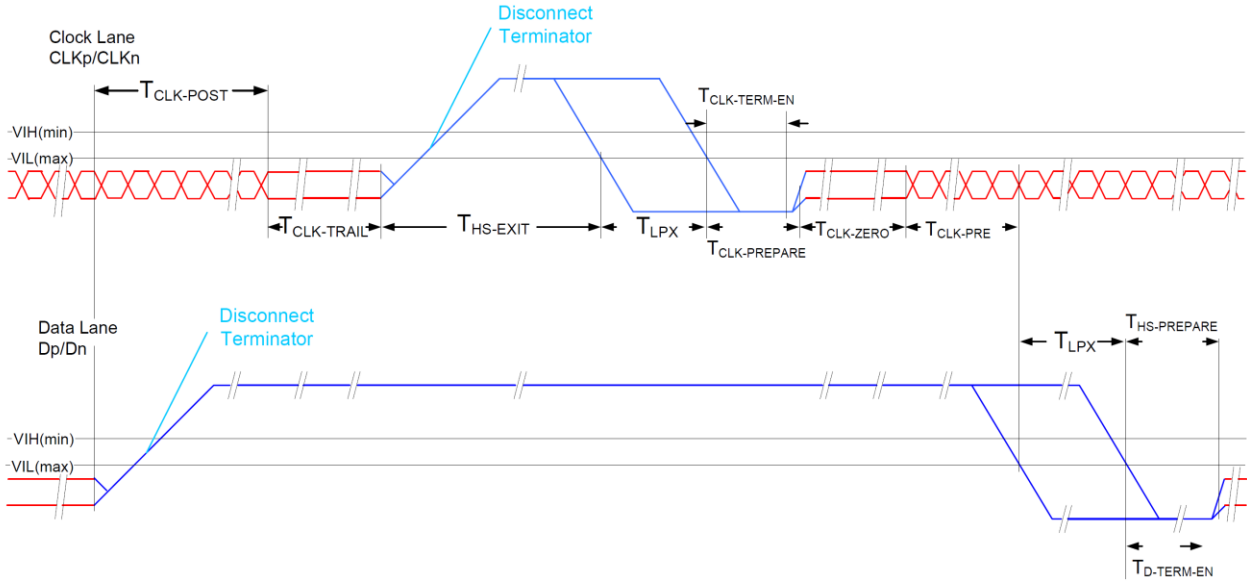
9.2 Communication Interface timing

9.2.1 MIPI-DSI 1 lane Interface Characteristics

HS Data Transmission Burst



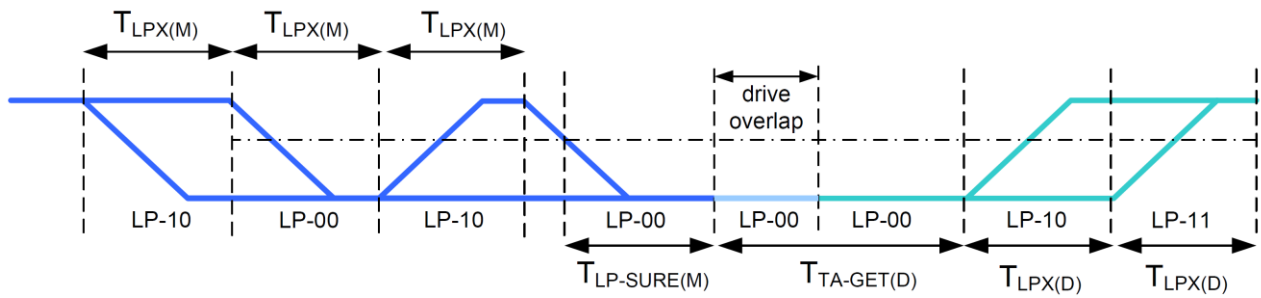
HS clock transmission



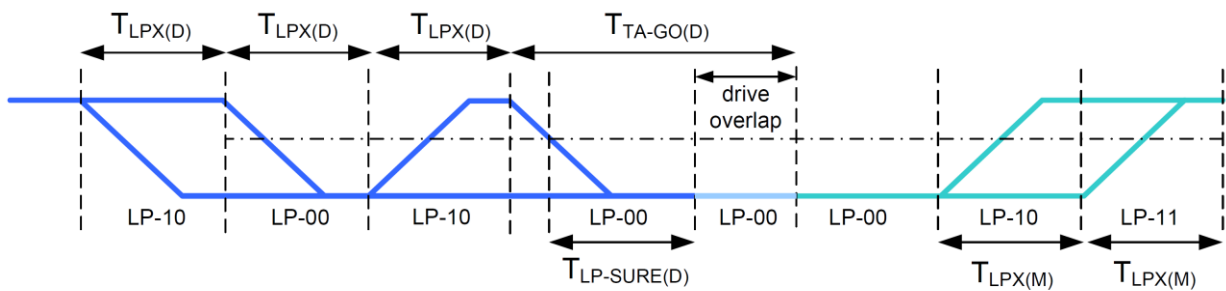
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns + 52*UI$			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		$35 ns + 4*UI$	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85 ns + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$60ns + 4*UI$			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

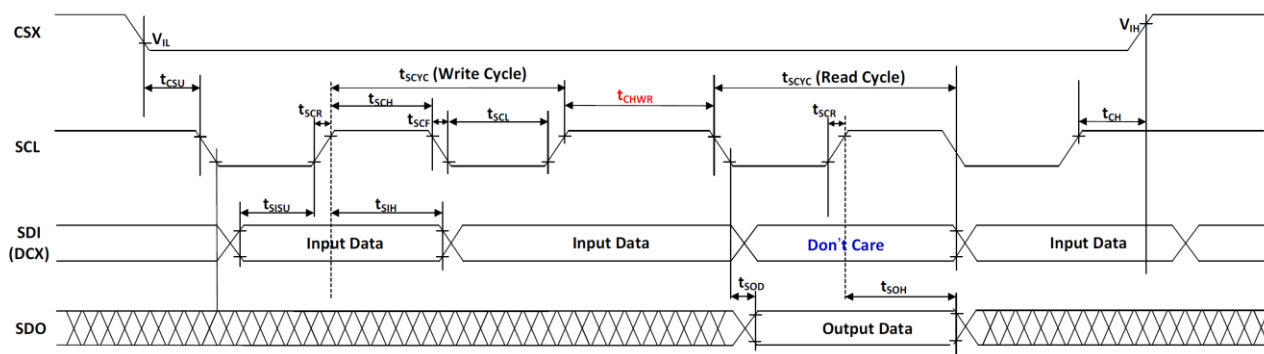
Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2 \cdot T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5 \cdot T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4 \cdot T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2 \cdot T_{LPX(D)}$	ns	2

NOTE:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

9.2.2 SPI-3Wire/ SPI-4Wire Interface Characteristics

3/4-wire SPI

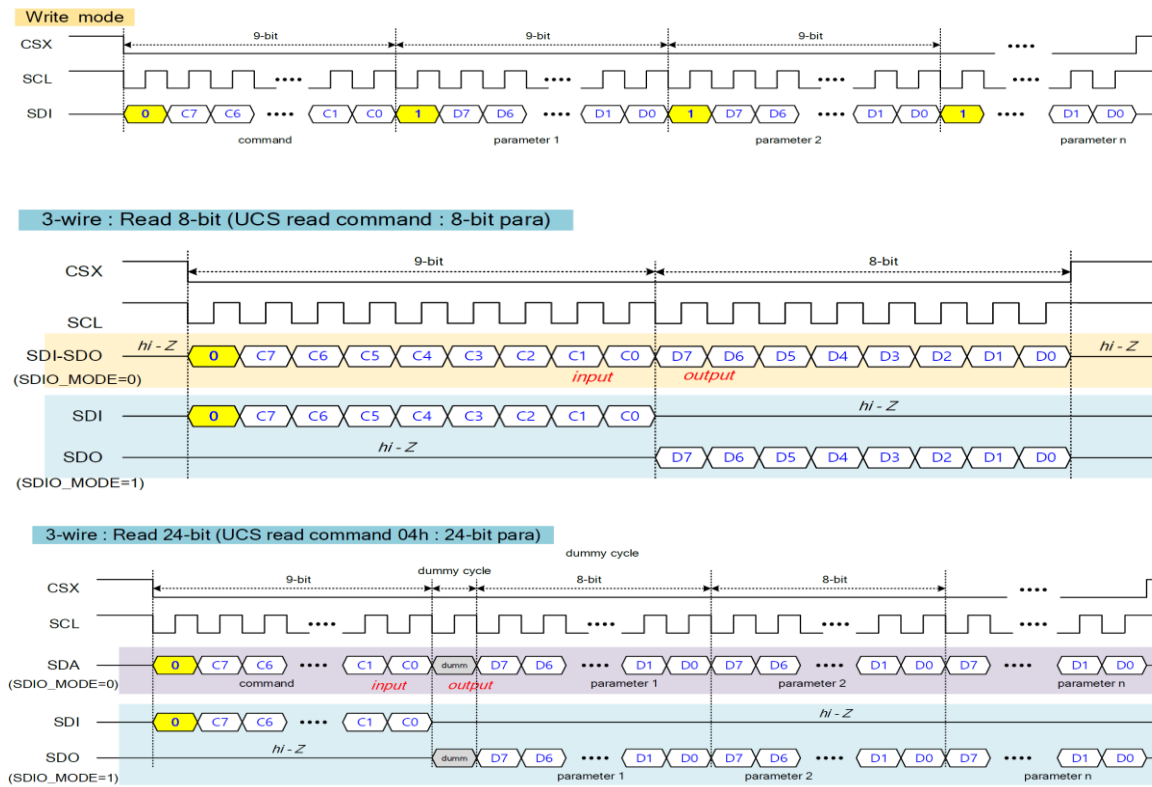


Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCYC}	Write	20			ns
		Read	300			ns
Clock high pulse width	t_{SCH}	Write	6.5			ns
		Read	140			ns
Clock low pulse width	t_{SCL}	Write	6.5			ns
		Read	140			ns
Clock rise time	t_{SCR}	$0.2 \cdot V_{DDI} \rightarrow 0.8 \cdot V_{DDI}$			3.5	ns
Clock fall time	t_{SCF}	$0.8 \cdot V_{DDI} \rightarrow 0.2 \cdot V_{DDI}$			3.5	ns
Chip select setup time	t_{CSU}		10			ns
Chip select hold time	t_{CH}		10			ns
Data input setup time	t_{SISU}	To V_{IL} of SCL's rising edge	5			ns
Data input hold time	t_{SIH}		5			ns
Access time of output data	t_{SOD}	From V_{IL} of SCL's falling edge			120	ns
Hold time of output data	t_{SOH}	From V_{IH} of SCL's rising edge	5			ns
Transition time from Write cycle to Read cycle	t_{CHWR}	From V_{IH} of SCL's rising edge	150			ns

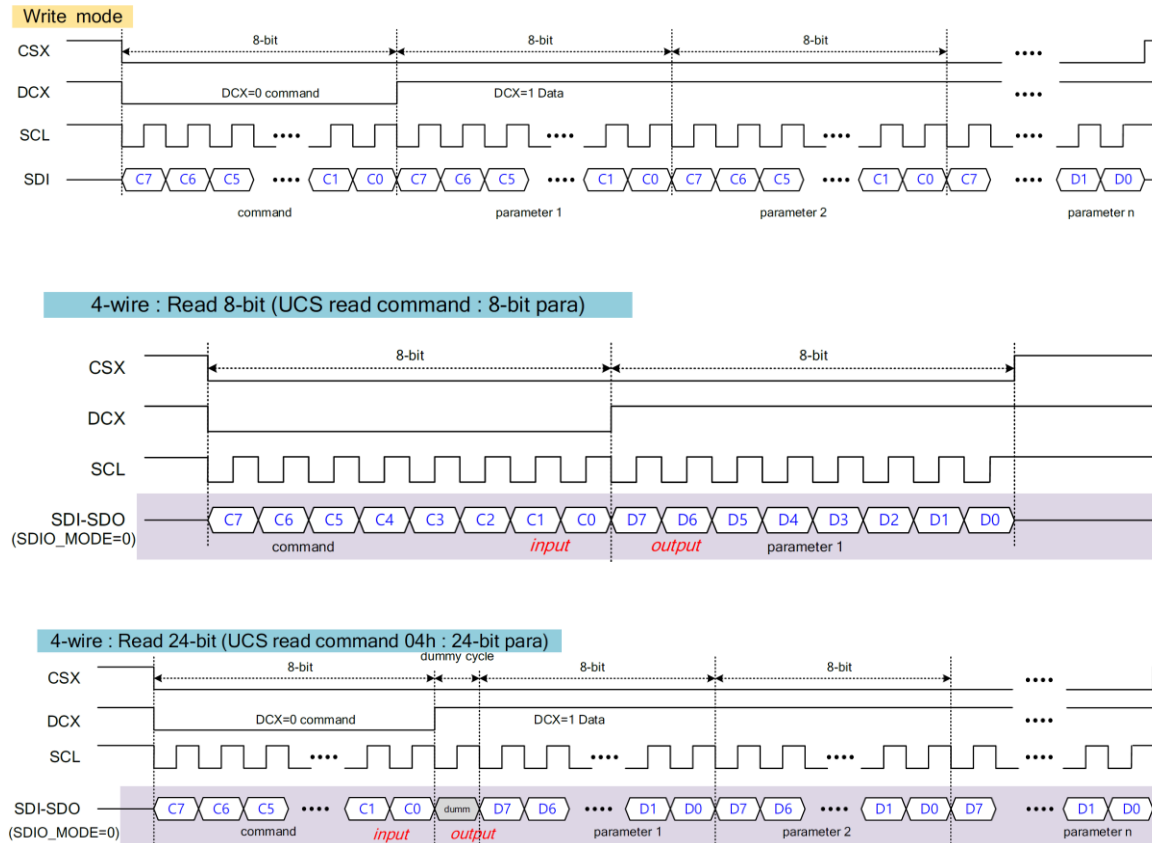
Notes:

- (1) Logic high and low levels are specified as 80% and 20% of V_{DDI} for Input signals.
- (2) For the 4-wire SPI, the DCX's timing is the same as input data.
- (3) $T_a = -30^{\circ}\text{C}$ to 70°C , $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{CI}=2.7\text{V}$ to 3.6V , and $V_{SS}=0\text{V}$

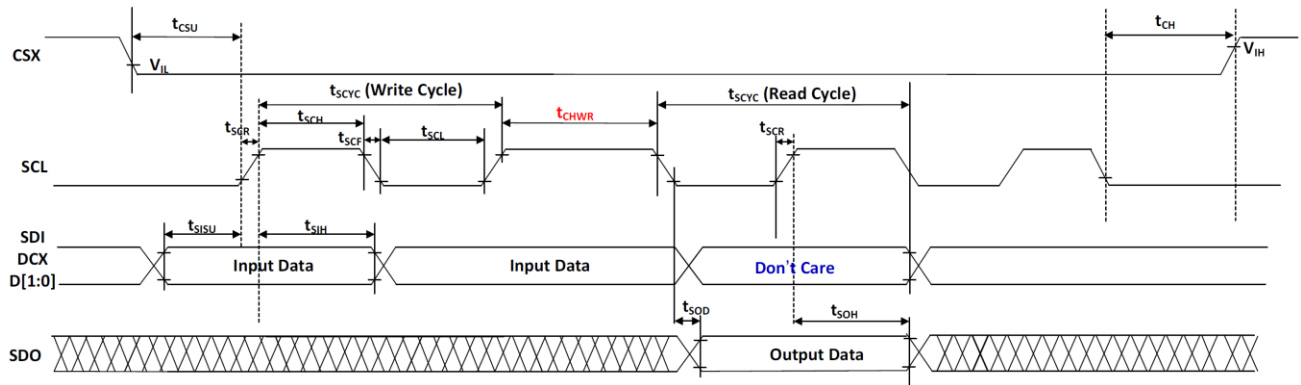
SPI-3 Wire (9-Bit) Interface Protocol – Register Write and Read



SPI-4 Wire (8-Bit) Interface Protocol – Register Write and Read



9.2.3 QSPI Interface Characteristics



Note: The max SCL frequency for each pixel data format is specified as the below table.

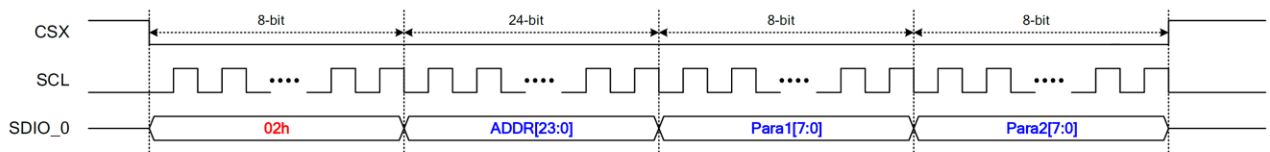
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: $T_a = -30$ to 70°C , $V_{DDI} = 1.65\text{V}$ to 3.3V , $V_{CI} = 2.7\text{V}$ to 3.6V , $GND = 0\text{V}$

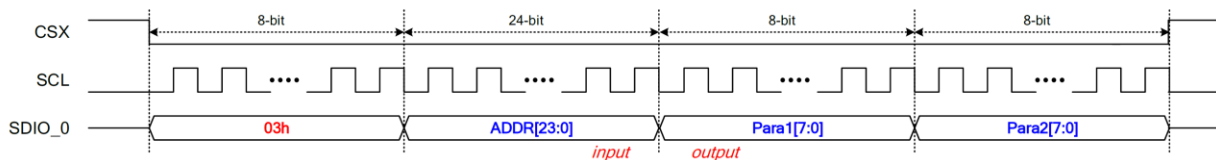
QSPI Timing

Quad SPI Interface Protocol – Register Read and Write

Command Write

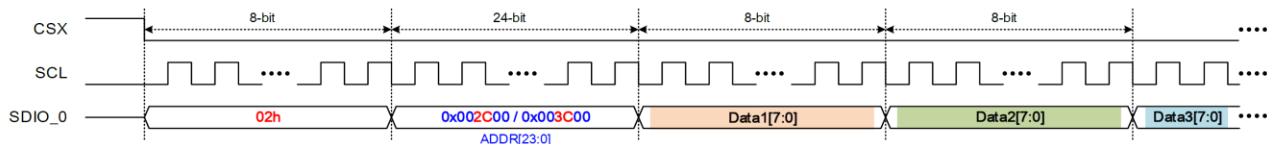


Command Read

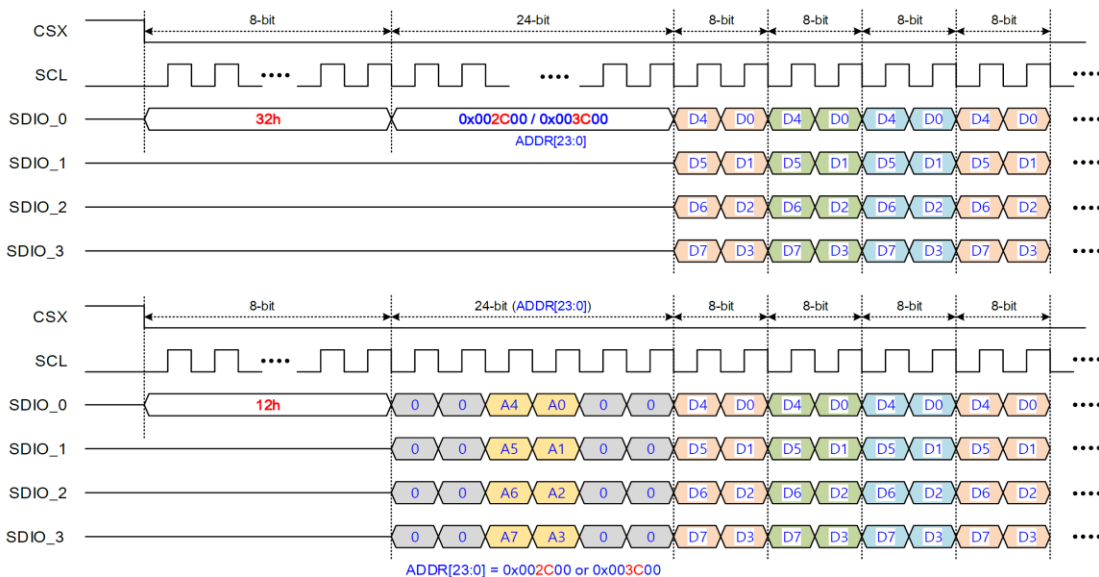


Quad SPI Interface Protocol – Pixel Interface

1-Wire Pixel Write

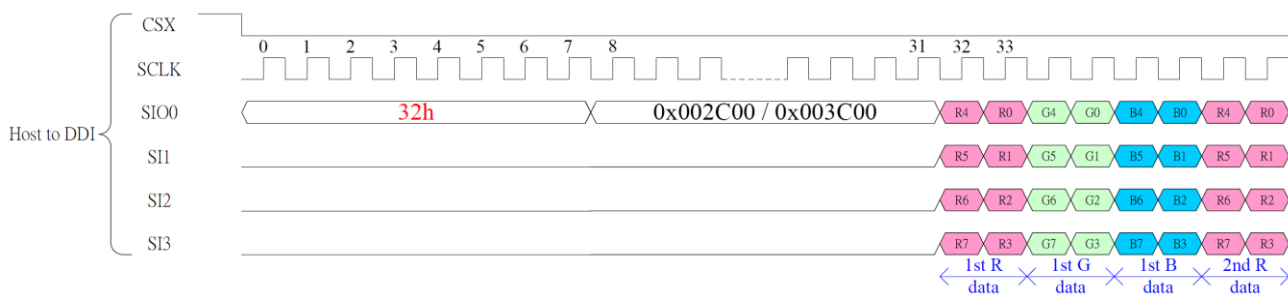


4-Wire Pixel Write

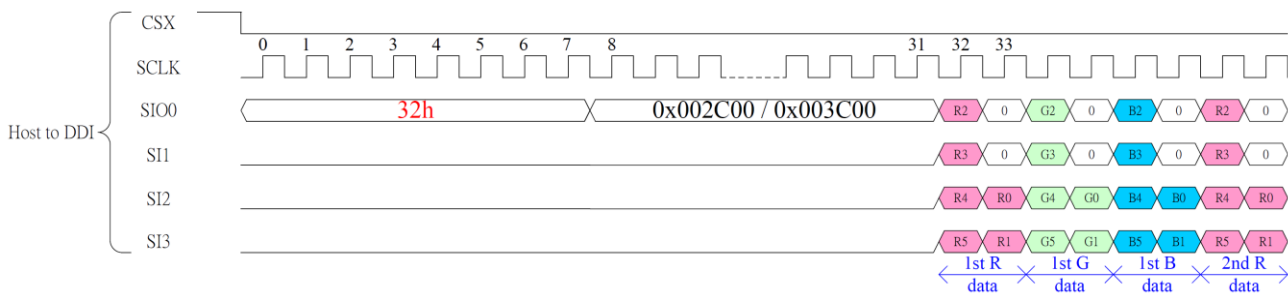


SPI-4Lanes Pixel Write Data Waveform

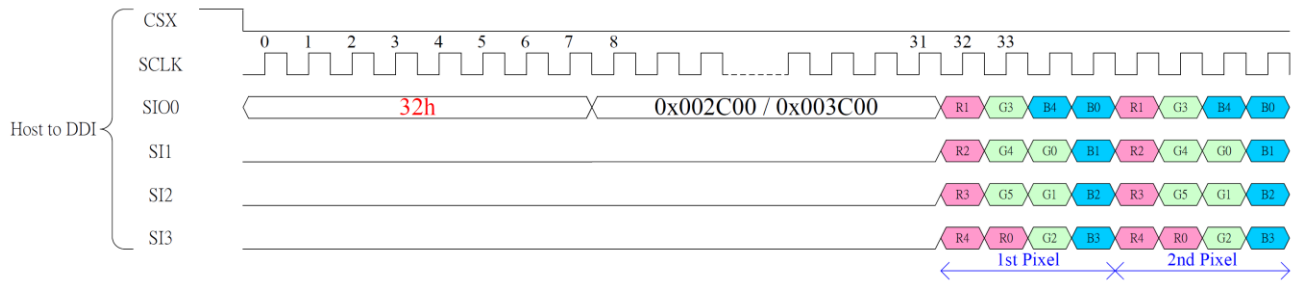
RGB888 – 4-Lanes



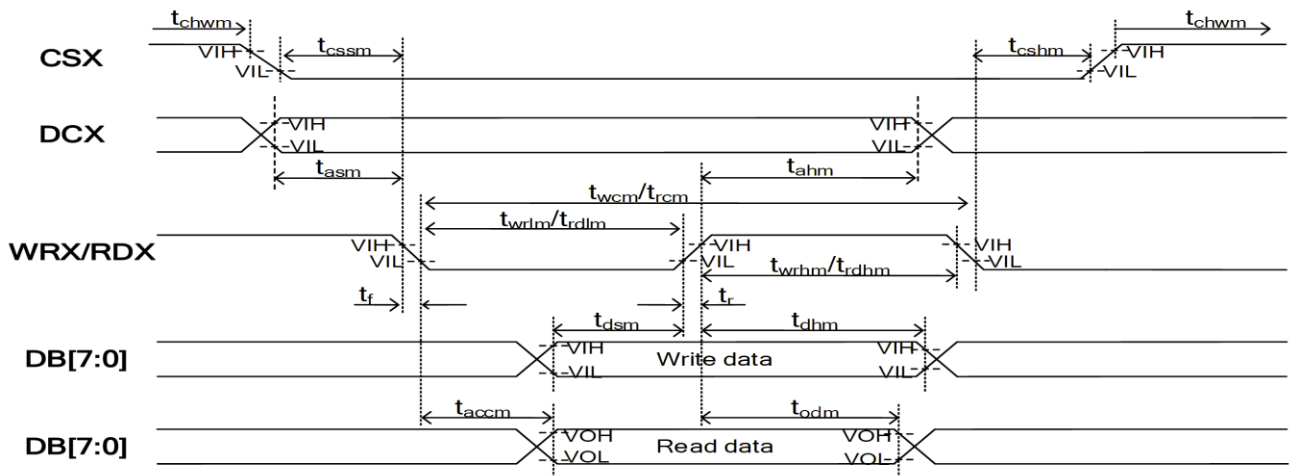
RGB666 – 4-Lanes



RGB565 – 4-Lanes



9.2.4 i8080-8Bits Interface Characteristics



Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{cssm}	10	—	ns
Chip select hold time		t_{cshh}	10	—	ns
Chip select “High” pulse width		t_{chwm}	20	—	ns
Address setup time	DCX	t_{asm}	10	—	ns
Address hold time(Write/Read)		t_{ahm}	10	—	ns
Write cycle time	WRX (Write)	t_{wcm}	20	—	ns
WRX “High” period (Write)		t_{wrhm}	10	—	ns
WRX “Low” period (Write)		t_{wrlm}	10	—	ns
Read cycle time (Register Read)	RDX (Register Read)	t_{rcm}	100	—	ns
RDX “High” period (Register Read)		t_{rdhm}	50	—	ns
RDX “Low” period (Register Read)		t_{rdlm}	50	—	ns
Read cycle time (Memory Read)	RDX (Memory Read)	t_{rcm}	200	—	ns
RDX “High” period (Memory Read)		t_{rdhm}	100	—	ns
RDX “Low” period (Memory Read)		t_{rdlm}	100	—	ns
Data setup time	DB[7:0]	t_{dsm}	10	—	ns
Data hold time		t_{dhm}	10	—	ns
Access time	DB[7:0]	t_{accm}	—	40	ns
Output disable time		t_{odm}	20	—	ns
Rise/Fall time	-	t_r/t_f	—	1	ns

10. Standard Specification For Reliability

No	Item	Condition	Cycles	Judgment Criterion
1	High Temperature Operation	80°C/ 240hours	10	1. No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted. 2. No function-related abnormalities.
2	Low Temperature Operation	-30°C/ 240hours	10	
3	High Temperature Storage	85°C/ 240hours	5	
4	Low Temperature Storage	-40°C/ 240hours	5	
5	High Temperature Humidity Operation	60°C/90%RH/ 240hours	5	
6	Thermal Shock	-40°C~85°C / 100cycles	5	

Note: The results must be measured after 2 hours later under room temperature keeping.

- END -