

Product Specification

❖ **Product Name: AMOLED**

❖ **Model Name: DO0241VMST07**

❖ **Description: 2.41 inch (450x600)**

Proposed by			Customer's Approval
Designed	Checked	Approved	

Document Revision History

Rev. No.	Date	Contents	Remark
0.0	2024-05-22	-.Initial issue	Preliminary

1.General Description:

- Driving Mode: Active Matrix.
- Color Mode: 16.7M/262K/65K color
- Display Format: 2.41" (450RGB x 600)
- Pixel arrangement: Real RGB arrangement
- Display Driver IC : RM690B0 (1/3RAM) or Compatible
- Touch Driver IC : FT6336U or Compatible
- Display Interface: SPI-3Wire/SPI-4Wire/QSPI/MIPI-DSI
- Touch Interface: IIC [**Slave Addr A[6:0]---0X38**]
- Application: Handheld & measuring equipment & sports camera
- RoHS Compatible

2.Mechanical Data

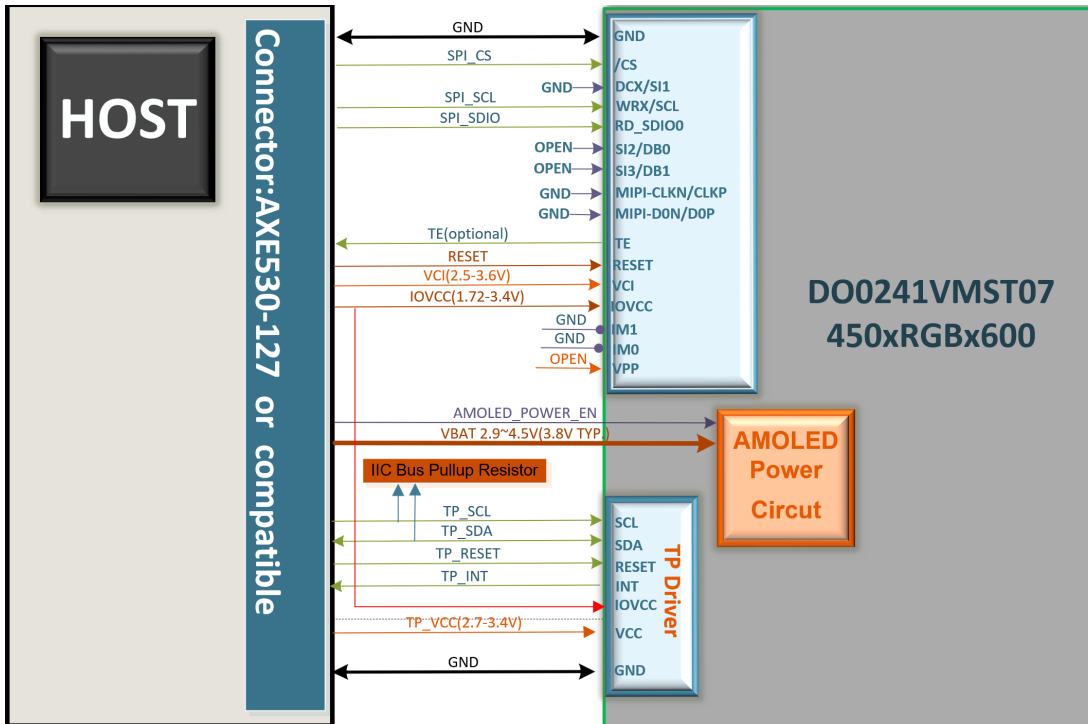
Item	Specifications	Unit
Dimensional outline	44.72(W) x61.56(H) x Thickness	mm
Thickness	1.93(Total) --- 0.7 (COVER LENS) --- 0.43 (Sensor + OCA) --- 0.8 (AMOLED)	mm
Number of dots	450(W) x RGB x 600(H)	Dots
Active area	36.72(W) x 48.96(H)	mm
Pixel Size	81.6 x 81.6	um
Diagonal Inch	2.41	inch
Frame rate	60 (MIPI Video Mode)	Hz

*See attached drawing for details.

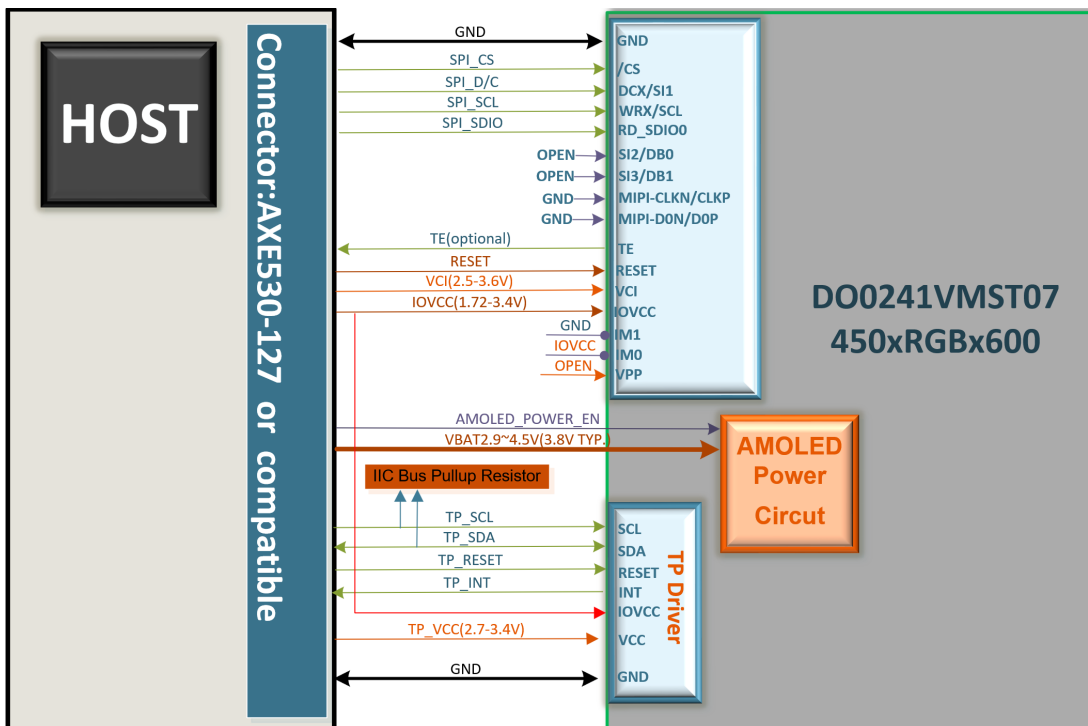
3. Block Diagram

DO0241VMST07 support various interfaces, and interfaces are selected by setting the **IM[1:0]** pins.

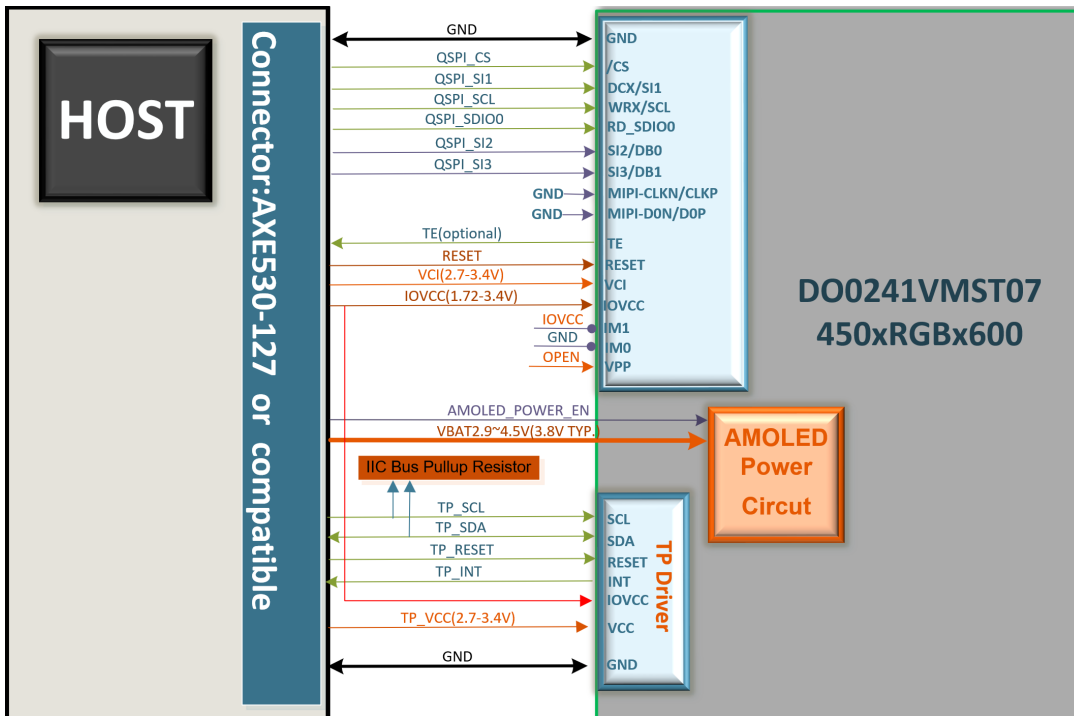
A: If IM1=GND,IM0=GND, DO0241VMST07 set to **spi-3wire interface**



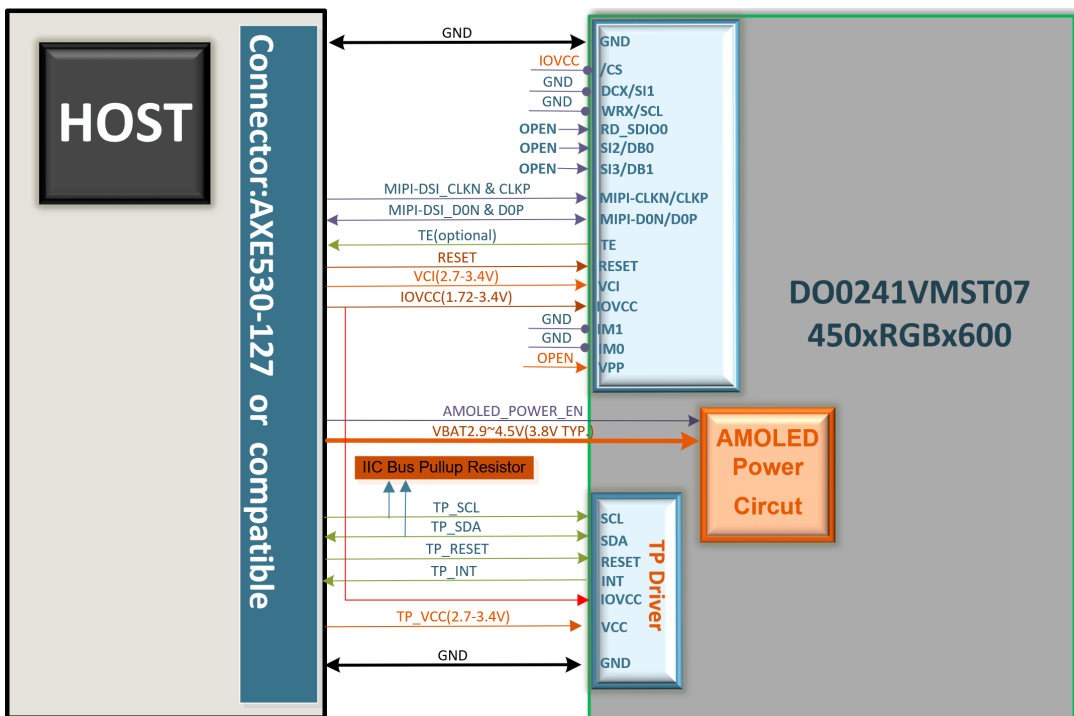
B: If IM1=GND,IM0=IOVCC, DO0241VMST07 set to **spi-4wire interface**



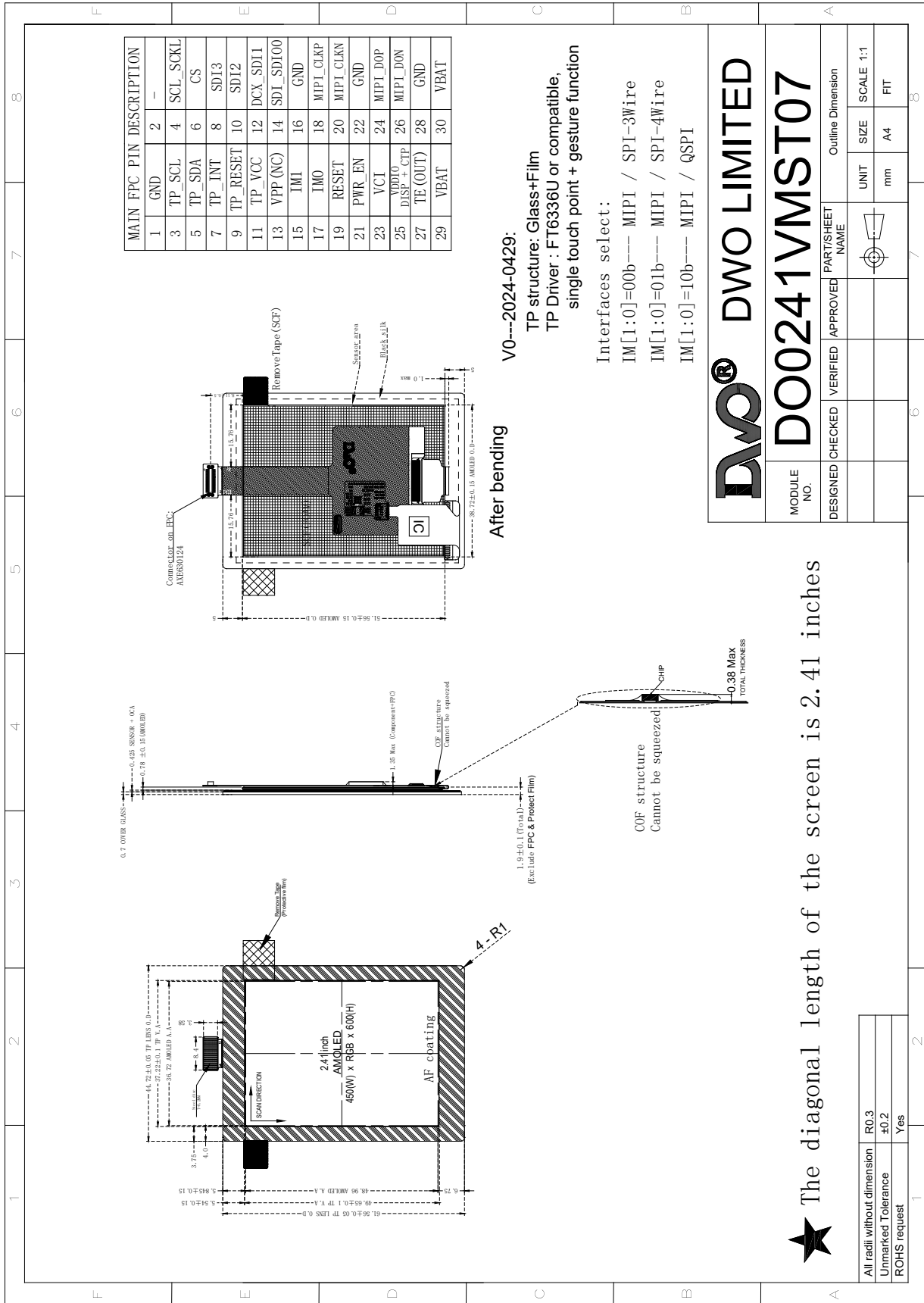
C: If IM1=IOVCC,IM0=GND, DO0241VMST07 set to QSPI interface



D: If IM1=GND,IM0=GND, CS=IOVCC, DO0241VMST07 set to MIPI-DSI interface



4.Dimension



5.Pin Description

Recomend Connector : AXE530-127.(AXE630124 on AMOLED)

NO.	Pin Name	I/O	Description
1	GND	P	Ground Terminal
3	TP_SCL	I	Touch Panel Clock Input. Communication Voltage follow IOVCC. If not used, please open this pin.
5	TP_SDA	I/O	Touch Panel Data Input and output. Communication Voltage follow IOVCC. If not used, , please open this pin.
7	TP_INT	O	Touch Panel Interrupt Output. If not used, please open this pin.
9	TP_RESET	I	TP Reset signal Input. Communication Voltage follow IOVCC. If not used, , please open this pin.
11	TP_VCC	P	Analog Voltage for TP Driver (2.7~3.4V)
13	VPP(NC)	P	OTP Power Supply(Let it open).
15	IM1	I	Interface type selection
17	IM0	I	Interface type selection
19	RESET	I	AMOLED Reset signal Input
21	PWR_EN	I	Power IC enable control pin.
23	VCI_IN	P	Analog Voltage for Display Driver (2.7~3.6V)
25	VDDIO(IOVCC)	P	Driver IC(Touch + Display) Digital I/O Power Supply(1.72~3.4V)
27	TE	O	Tearing Effect
29	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)
NO.	Pin Name	I/O	Description
2	-	-	
4	WRX_SCL	I	SCL: A synchronous clock signal in SPI I/F. If not used, please connect to GND.
6	CS	I	Chip select input pin ("Low" enable) SPI I/F. If not used(MIPI Interface), please connect these pin to IOVCC.
8	SDI3	I	Serial Data Input in QSPI,data Lane 3. If not used, please open this pin.
10	SDI2	I	Serial Data Input in QSPI,data Lane 2. If not used, please open this pin.
12	DCX_SD11	I/O	Serial Data Input in QSPI,data Lane 2. Serial Data Output in SPI_3Wire/ SPI_4Wire Data Input Signal at Dual Input Mode. Display data / command selection in SPI 4-wire I/F.

			D/CX = "0" : Command; D/CX = "1" : Display data or Parameter If not used, please connect to GND..
14	RDX_SDIO0	I/O	Serial Data Input in QSPI,data Lane 0. Serial Data input in SPI_3Wire/ SPI_4Wire Data Input Signal at Dual Input Mode. If not used, please leave it Open.
16	GND	P	Ground Terminal
18	MIPI_CLKP	I	Differential clock signals if MIPI interface. If not used, please connect these pins to GND.
20	MIPI_CLKN	I	Differential clock signals if MIPI interface. If not used, please connect these pins to GND.
22	GND	P	Ground Terminal
24	MIPI_D0P	I/O	Differential data signals if MIPI interface. If not used, please connect these pins to GND.
26	MIPI_D0N	I/O	Differential data signals if MIPI interface. If not used, please connect these pins to GND.
28	GND	P	Ground Terminal
30	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)

Note: The connections of IM[1:0] which not shown in table are invalid

IM[1:0]	Display Data	Command
00	MIPI / SPI 3-wire	MIPI / SPI 3-wire
01	MIPI / SPI 4-wire	MIPI / SPI 4-wire
10	MIPI / QSPI	MIPI / QSPI

6. DC Characteristics

6.1 DC Characteristics Requirements

Item	Symbol	Values			Unit	Remark
		Min	Type	max		
Analog power supply Vo	VCI	2.7	3.3	3.4		
I/O Supply Voltage	VDDIO	1.65	1.8	3.4	V	
OLED input voltage	VBAT	2.9	3.8	4.5	V	
VCI_EN Voltage	VCI enable signal	VIL:0.4V VIH:1.2V				
Input High Voltage	VIH	0.8*VDDI	--	VDDI	V	
Input Low Voltage	VIL	0	--	0.2*VDDI	V	
Output High Voltage	VOH	0.8*VDDI	--	VDDI	V	
Output Low Voltage	VOL	0	--	0.2*VDDI	V	
Frame Frequency (60Hz)	frame	58	60	62	HZ	

6.2 Power Consumption of Display

Power Supply: IOVCC=1.8V , VCI=3.3V,VBAT=3.3V ;

Item	Symbol	Condition	Symbol	Min.	Typ.	Max.	Uni	Remark	
VBAT	VBAT	Normal	-	2.9	3.8	4.5	V		
VCI	VCI	-	-	2.65	2.8	3.4	V		
VDDIO	VDDIO	-	-	1.72	1.8	3.4	V		
Power Consumption	Display on mode (Normal)	100% Pixel On,800nits,	Display IC	VCI		3.9	⁵	mA	
				VDDIO		1.8	³	mA	
			Panel	VBAT		180	240	mA	
Frame Rate	F _{frm}	-30°C~80°C	F _{frm}	55.2	60	64.8	Hz		
		25°C		58.2	60	61.8	Hz		

7. Electro-optical characteristics

Test condition : VCC= 3.3V, VDDIO=1.8V , VBAT=3.3V, Ta=25°C

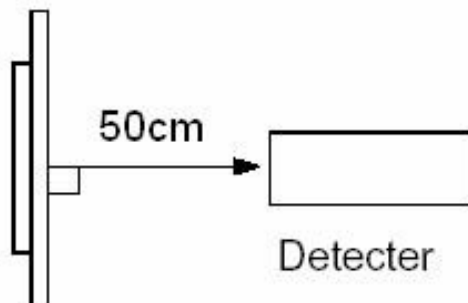
Item	Symbol	Condition	Min	Typ	Max	Unit	Note	
Luminance (with pol&lens)	Normal mode Bp	$\theta=0^\circ \phi=0^\circ$	750	800	900	cd/m ²		
Uniformity	Δ Bp		90	--	--	%		
Viewing Angle	Left	θ_L	Cr \geq 10	80	--	--	deg	
	Right	θ_R		80	--	--		
	Top	ψ_T		80	--	--		
	Bottom	ψ_B		80	--	--		
Contrast Ratio	Cr	$\theta=0^\circ \phi=0^\circ$	100000:1		--	-		
Response Time	Tr		--	--	2	ms		
	Tf		--	--	2	ms		
	Tgray		--	--	2	ms		
Color Coordinate of CIE193 1	Red	x	$\theta=0^\circ \phi=0^\circ$	0.660	0.680	0.700		
		y		0.300	0.320	0.340		
	Green	x		0.205	0.245	0.285		
		y		0.675	0.715	0.755		
	Blue	x		0.121	0.141	0.161		
		y		0.023	0.043	0.063		
	White	x		0.280	0.300	0.320		
		y		0.290	0.310	0.330		
Color temperature	CT		7000	7500	8000	K		
Flicker	amount	60HZ @Interval screen	--	--	-30	dB		
	amount	60HZ @255Gray	--	--	-50	dB		
	amount	45HZ, @255Gray	--	--	-40	dB		
	amount	30HZ, @255Gray	--	--	-30	dB		
	amount	15HZ, @255Gray	--	--	-30	dB		
Gamma	Normal mode		2.0	2.2	2.4			

Reflectance (With lens)	Rf	550nm	--	--	5.5	%	
Transmittance (Without lens)	Tr	400~700nm	--			%	
Polarization direction of front polarizer	PdF		--	135	--	deg	
Color shift		$\theta L=30^\circ$	--	3	4	JNCD	
		$\theta R=30^\circ$	--	3	4	JNCD	
		$\psi T=30^\circ$	--	3	4	JNCD	
		$\psi B=30^\circ$	--	3	4	JNCD	

7.1 Luminance measurement

The test condition is at 25°C and measured on the surface of OLED module.

- The data are measured after OLEDs are lighted on for more than 5 minutes and displays
- equipment CS2000/CS2000A or similar equipments (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measured value at the center point of panel must be after more than 5 minutes while light up

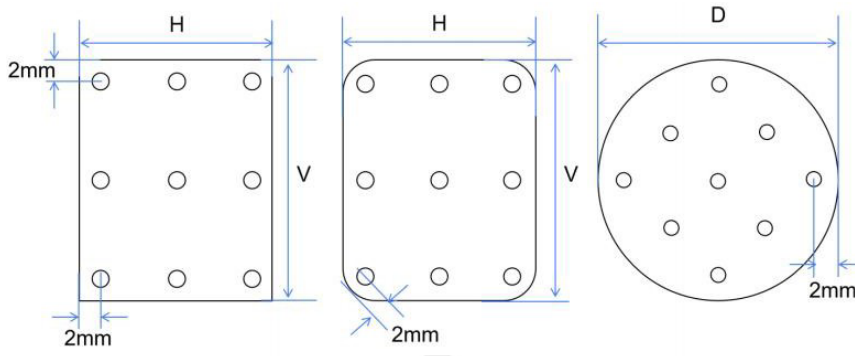


7.2 Uniformity

- The test condition is at 25°C and measured on the surface of display module
- Measurement equipment: CS2000/CS2000A or similar equipment.
- The luminance uniformity is calculated by using following formula.

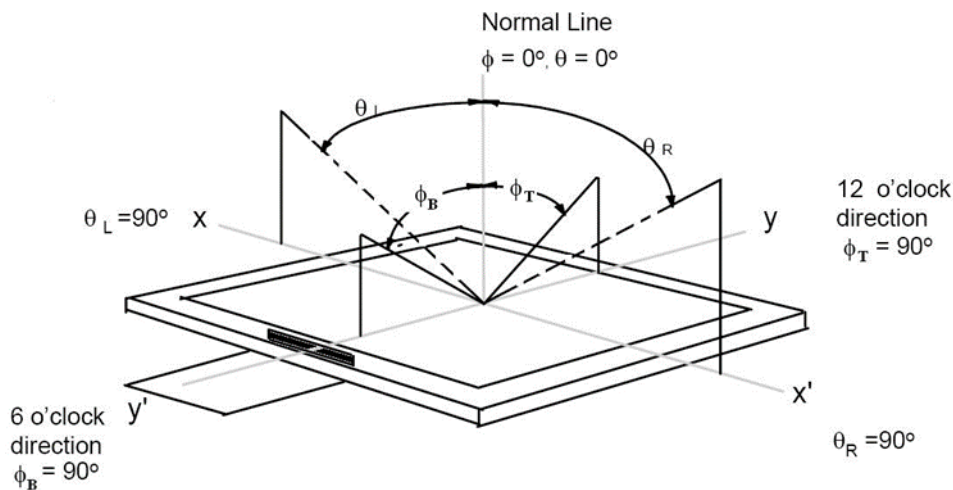
$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

- $Bp (\text{Max.})$ = Maximum brightness in 9 measured spots
- $Bp (\text{Min.})$ = Minimum brightness in 9 measured spots.



7.3 The definition of Viewing Angle

Refer to the graph below marked by θ and Φ



7.4 The definition of Contrast Ratio (Test OLED using CS2000/CS2000A or similar equipments):

Luminance is at "White" state

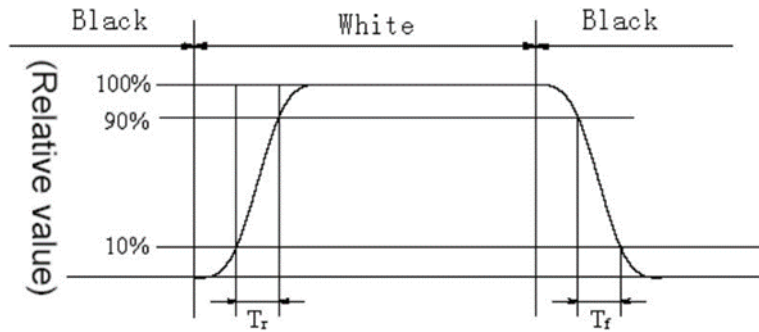
$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance is at "White" state}}{\text{Luminance is at "Black" state}}$$

Luminance is at "Black" state

(Contrast Ratio is measured in optimum common electrode voltage. Black state display pure black color and luminance < 0.002 nits.)

7.5 Definition of Response time. (Test module using DMS 803 or similar equipment):

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (Voltage falling time) and from "white" to "black" (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 80% of amplitudes. Refer to figure as below.



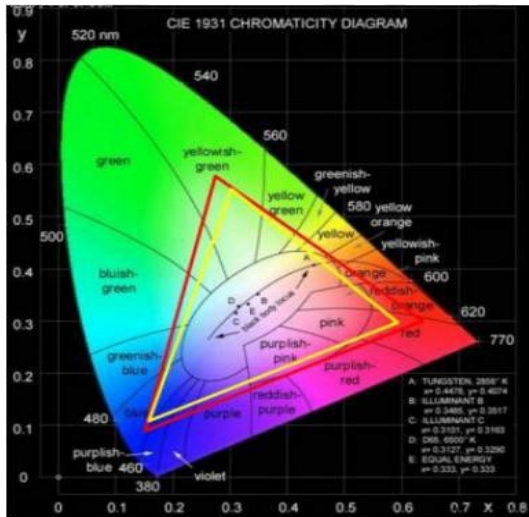
Response time of gray to gray:

- Measurement equipment: DMS803 or similar equipment.
- Test method: we define 8 grays L0-L7, the grays of L0-L7 were defined as:0,36,73, 109, 146, 182, 219, 255. The output signals of photo detector are measured when the input signals are changed from “Lx” to “Ly”, x, y= [0, 7]. The response time is defined as the time interval between the 10% and 90% of amplitudes. The result of the test can be noted as below:

	L0	L1	L2	L3	L4	L5	L6	L7
L0								
L1								
L2								
L3								
L4								
L5								
L6								
L7								

7.6 Definition of Color of CIE Coordinate and NTSC Ratio.

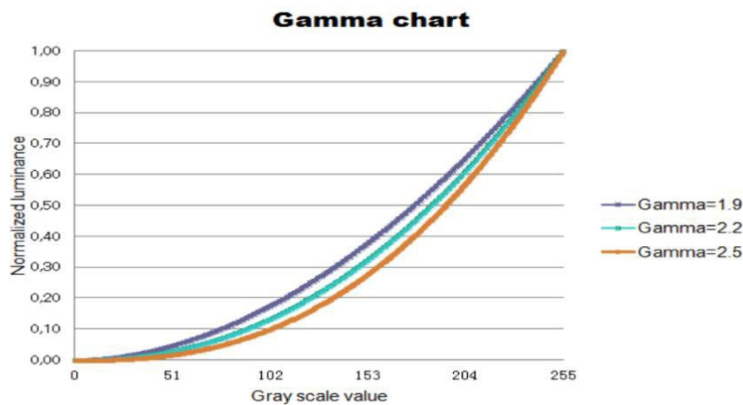
$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$



7.7 gamma curve control

- For gamma curve control, request as below:
- the whole curve's tolerance must control within +/-0.3, will test the gray scale below: 0~255gray, interval 8 gray (0,8,16,24.....255)
- According to below formula chart the curves

$$TR\%x = \sqrt{\frac{Gx - G0}{G255 - G0}}$$



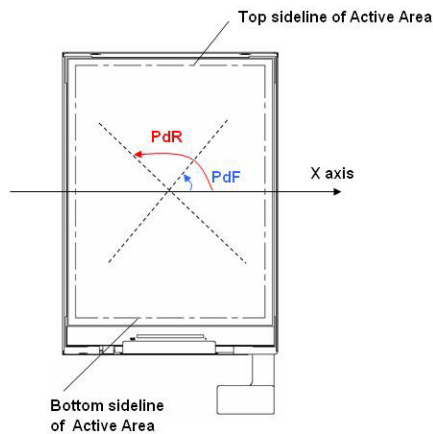
7.8 Reflectance Ratio

- Measurement equipment: Hunter Lab USPRO, Konica-Minolta CM-3600
- Measurement parameter: Reflectance Ratio @550nm

7.9 Polarization Direction Definition

- Viewing direction is normal user viewing direction which is vertical to the displaysurface
- The X axis is defined as parallel line to top&bottom sidelines of the Active Area
- PdF which is marked in blue arrow is polarization degree of Front polarizer

- The polarization degree parameter must be indicated in range of 0deg to 180deg according to above definition
- The angle definition of Polarization: The angle between polarized axis of Polarizer and zero of LCD
- Reference: Transmission axis 90deg for normal LCD POL; 45deg for normal OLED POL; TBD for sunglass POL;



Polarization Definition

7.10 Color Shift JNCD

- For JNCD measure:
 - Fix on one pattern like white pattern,
 - On the condition $\theta=0$ $F=0^\circ$, we can get the color coordinate (u_1', v_1') and on $\theta_L=30^\circ$ we can get another color coordinate (u_2', v_2')
 - $\Delta = \text{Square Root}((u_2' - u_1')^2 + (v_2' - v_1')^2)$
 - JNCD stands for "Just Noticeable Color Difference"
 - For the (u', v') color space $\text{JNCD}=0.0040$.
 - 2JNCD means $\Delta u'v' < 0.0080$
 - For color shift we need to measure white/red/green/blue pattern.

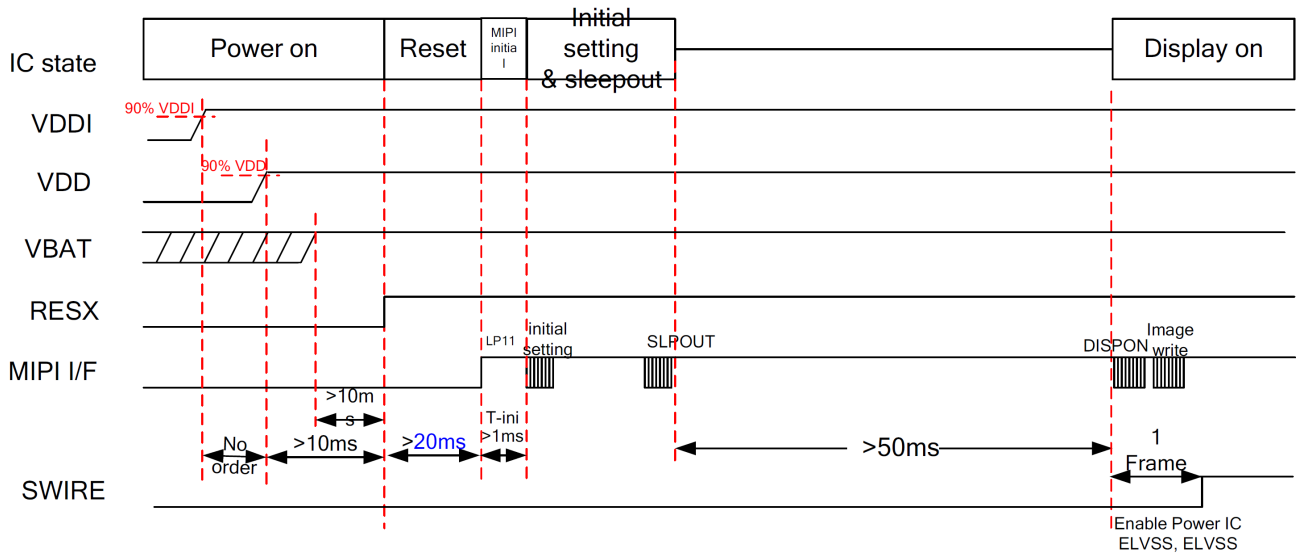
7.11 OLED lifetime

- Test samples 5pcs;
- Measurement equipment: CS2000/CS2000A or similar equipment.
- At room temperature(25°C), light the module with typical value brightness, display a white pattern,
 - To record the brightness every 24 hours.
 - $\text{LT}_{95} > 290\text{h}$.

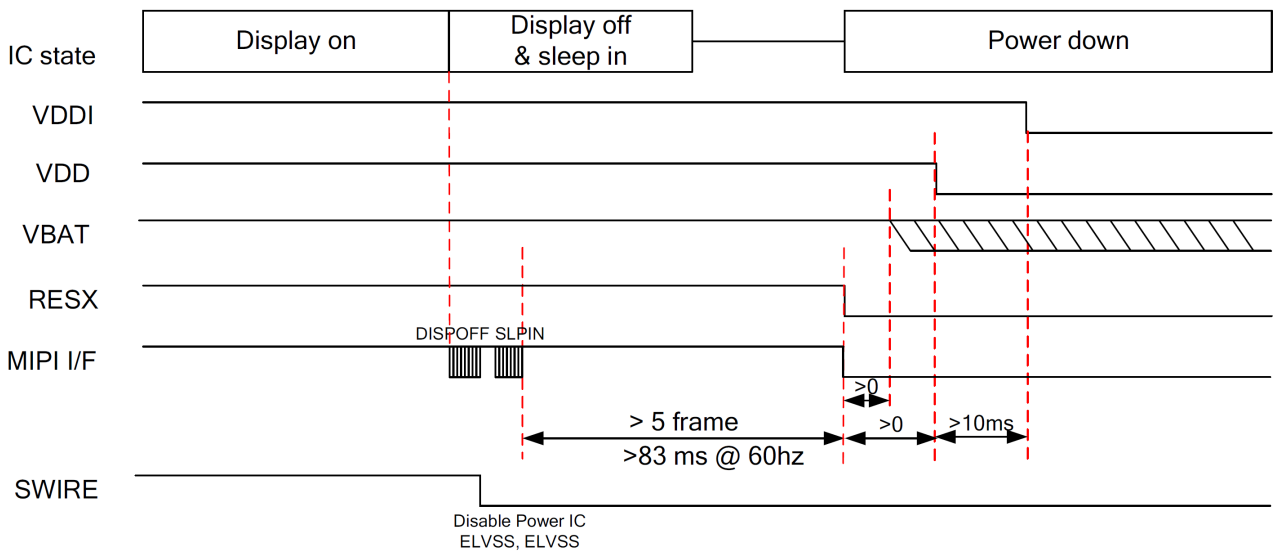
8. Timing Characteristics

8.1 Power on/off sequence and timing

Power On sequence

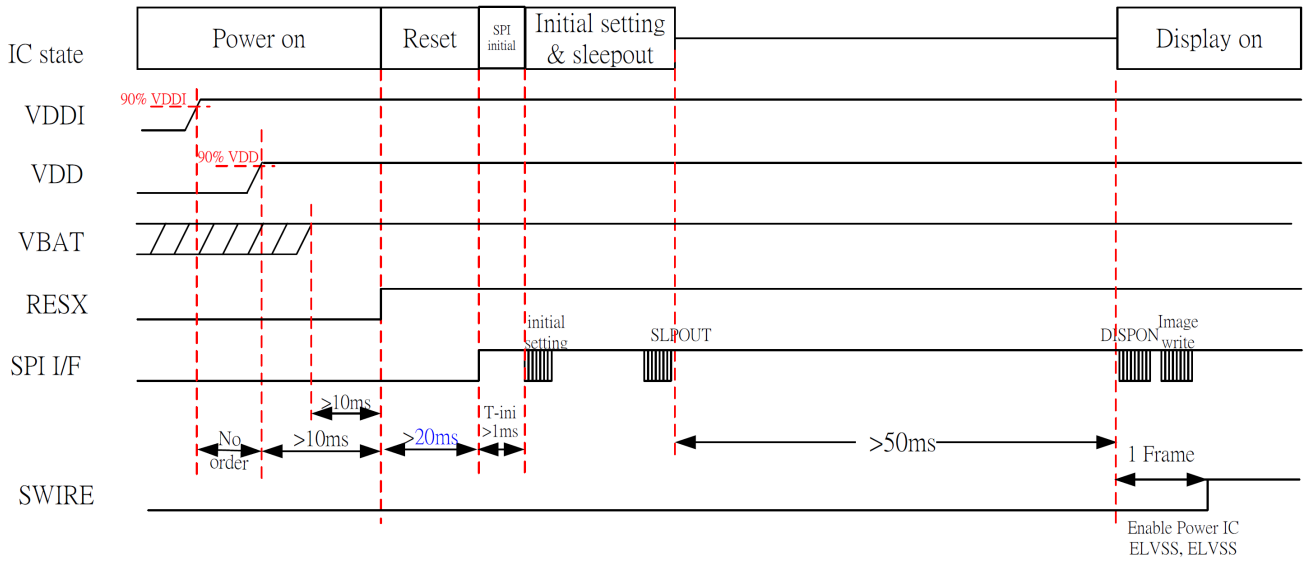


Power Off sequence



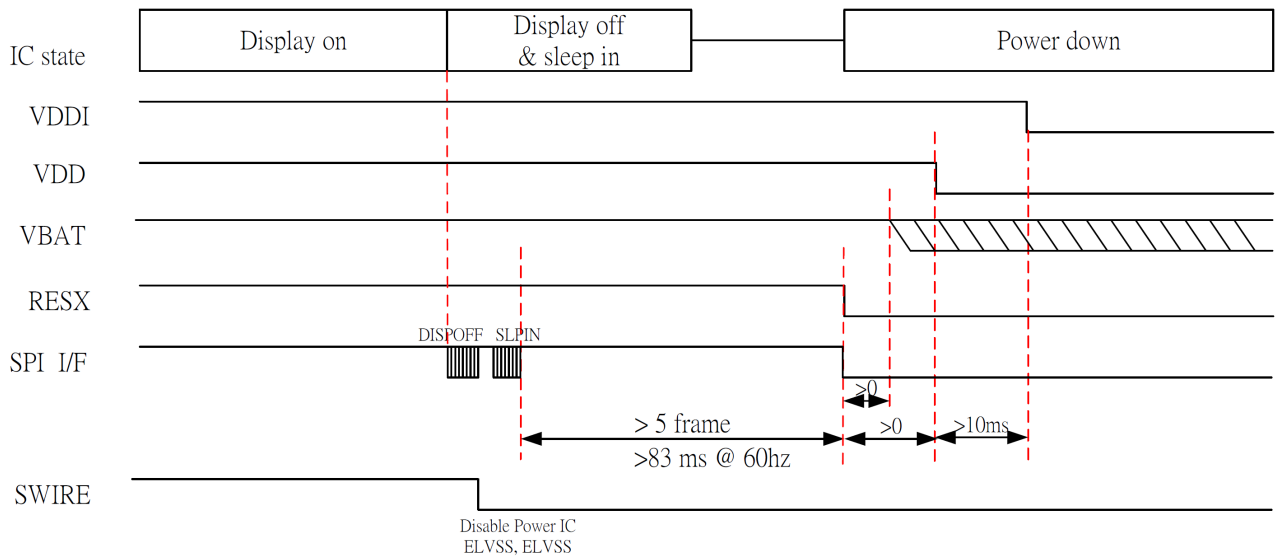
Power On sequence

SPI Interface

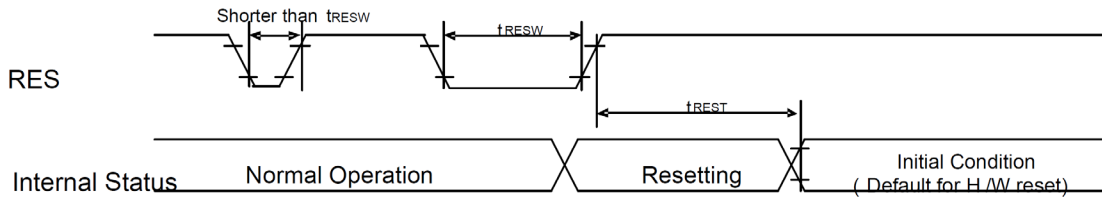


Power Off sequence

SPI Interface



8.2 Reset Timing Sequence Requirement



Reset input timing:

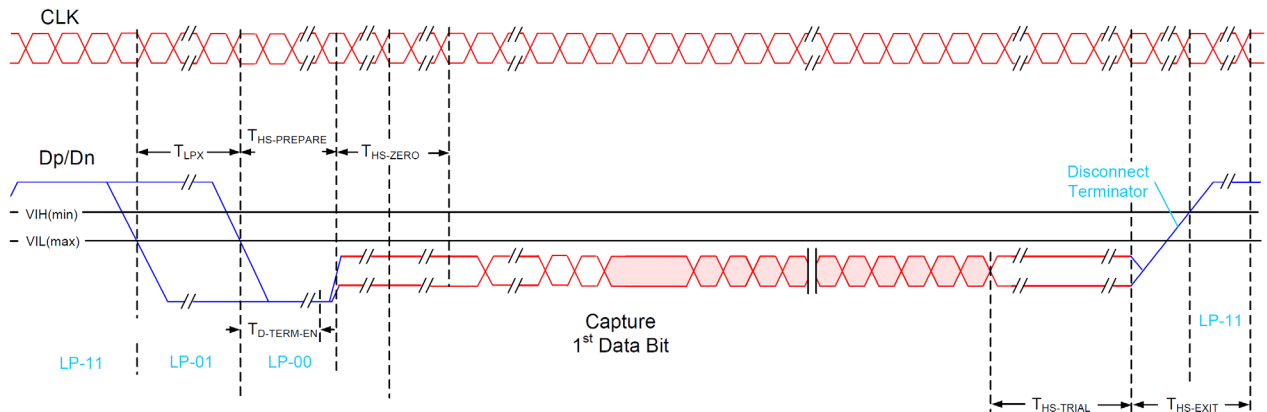
VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	30	-	-	-	μ s
t_{REST}	*2) Reset complete time	-	-	-	20	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

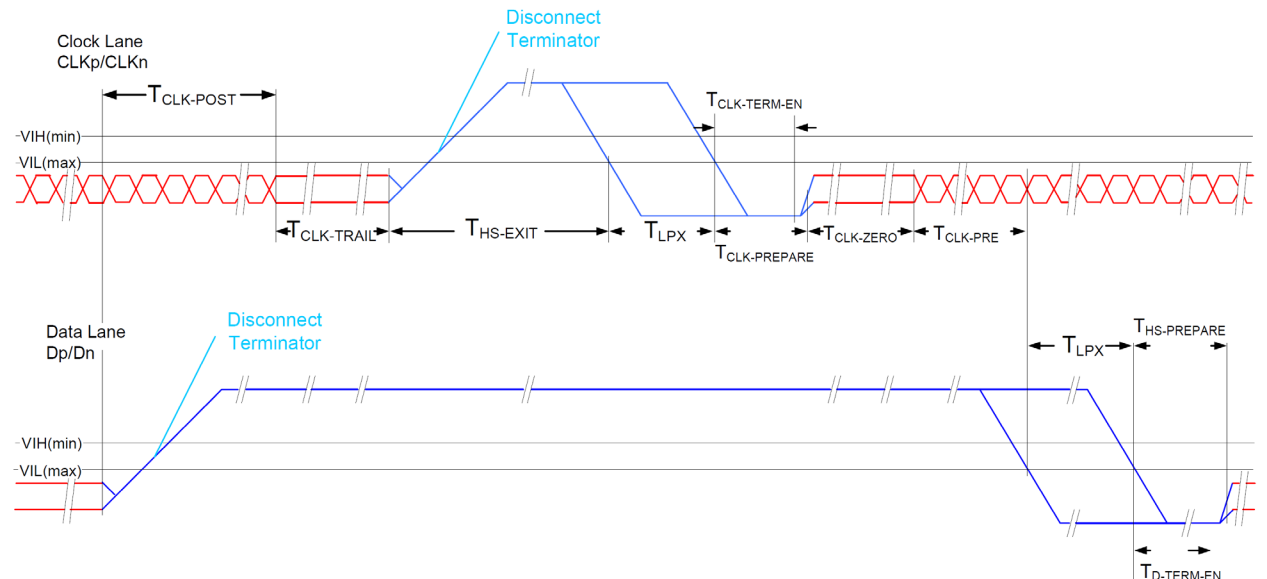
8.3 Communication Interface timing

8.3.1 MIPI-DSI 1 lane Interface Characteristics

HS Data Transmission Burst

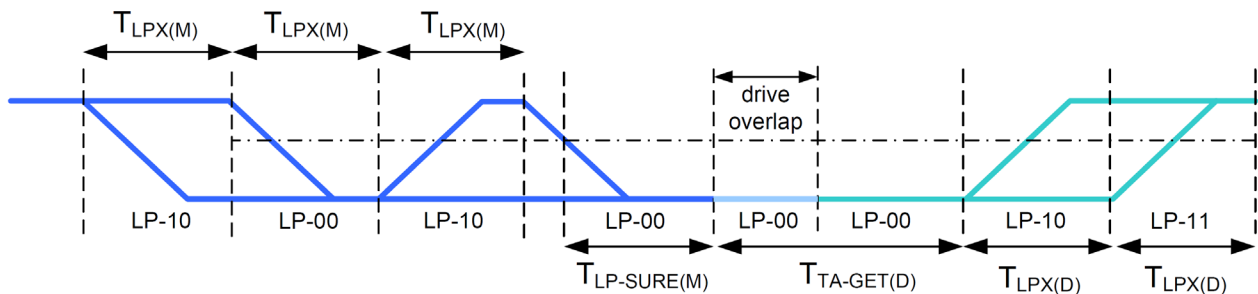


HS clock transmission

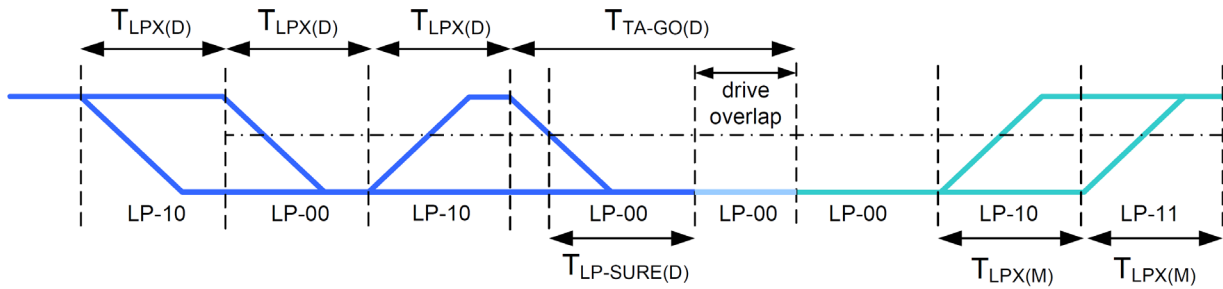


Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns + 52*UI$			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		$35 ns + 4*UI$	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85 ns + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$60ns + 4*UI$			ns

Turnaround Procedure


Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

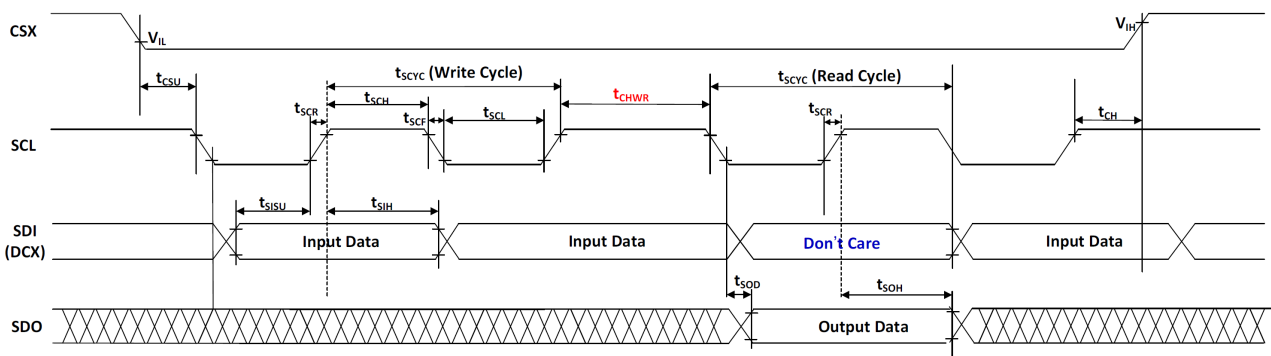
Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2 * T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5 * T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4 * T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2 * T_{LPX(D)}$	ns	2

NOTE:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

8.3.2 SPI-3Wire/ SPI-4Wire Interface Characteristics

3/4-wire SPI

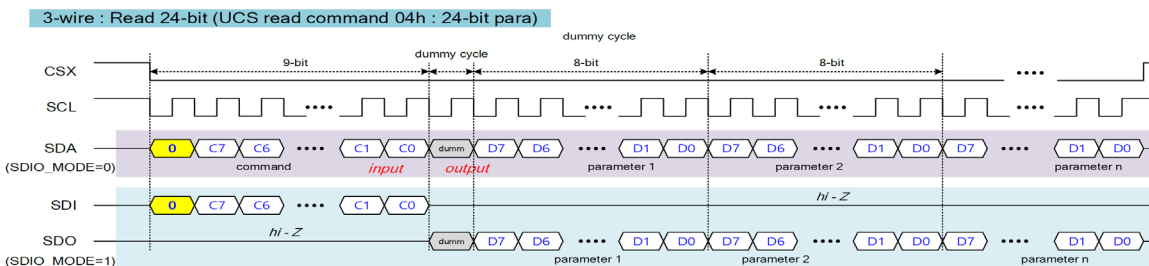
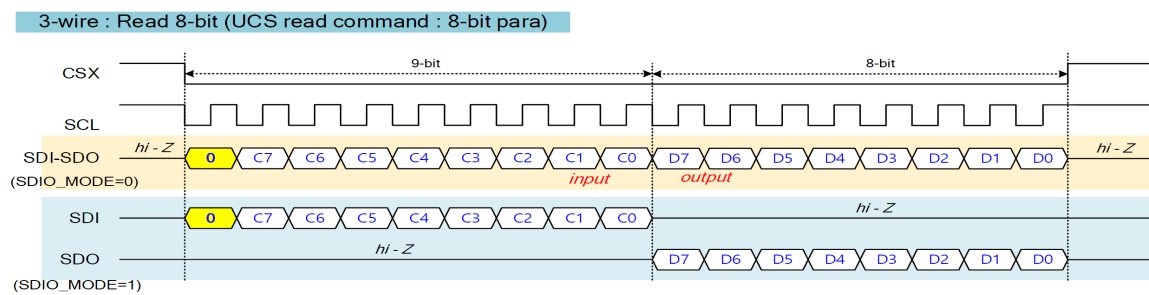
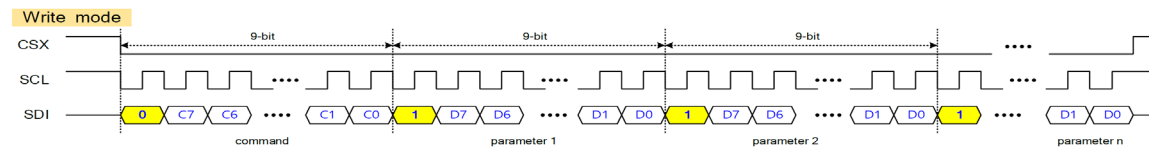


Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCYC}	Write	20			ns
		Read	300			ns
Clock high pulse width	t_{SCH}	Write	6.5			ns
		Read	140			ns
Clock low pulse width	t_{SCL}	Write	6.5			ns
		Read	140			ns
Clock rise time	t_{SCR}	$0.2*VDDI \rightarrow 0.8*VDDI$			3.5	ns
Clock fall time	t_{SCF}	$0.8*VDDI \rightarrow 0.2*VDDI$			3.5	ns
Chip select setup time	t_{CSU}		10			ns
Chip select hold time	t_{CH}		10			ns
Data input setup time	t_{SISU}	To V_{IL} of SCL's rising edge	5			ns
Data input hold time	t_{SIH}		5			ns
Access time of output data	t_{SOD}	From V_{IL} of SCL's falling edge			120	ns
Hold time of output data	t_{SOH}	From V_{IH} of SCL's rising edge	5			ns
Transition time from Write cycle to Read cycle	t_{CHWR}	From V_{IH} of SCL's rising edge	150			ns

Notes:

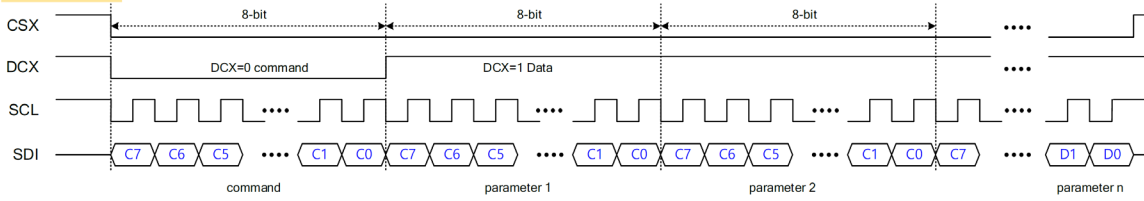
- (1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.
- (2) For the 4-wire SPI, the DCX's timing is the same as input data.
- (3) $T_a = -30^{\circ}C$ to $70^{\circ}C$, $VDDI=1.65V$ to $3.3V$, $VCI=2.7V$ to $3.6V$, and $VSS=0V$

SPI-3 Wire (9-Bit) Interface Protocol – Register Write and Read

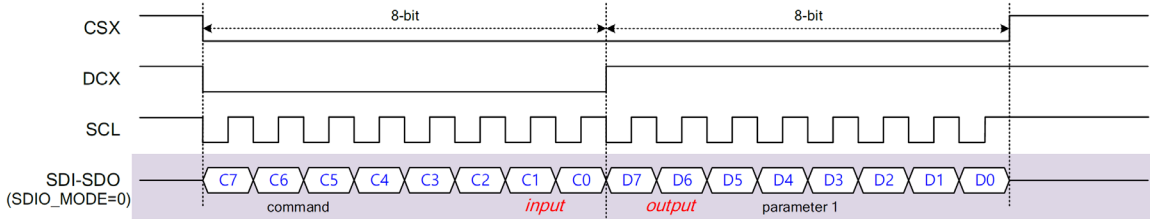


SPI-4 Wire (8-Bit) Interface Protocol – Register Write and Read

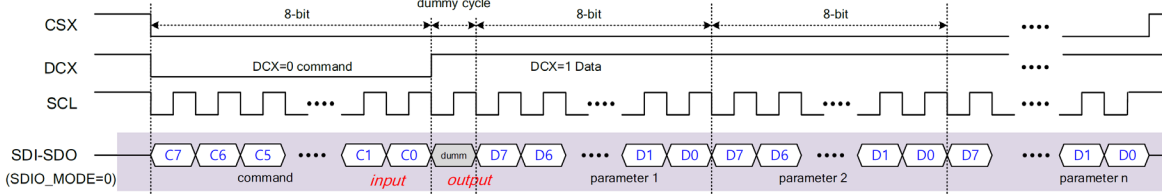
Write mode



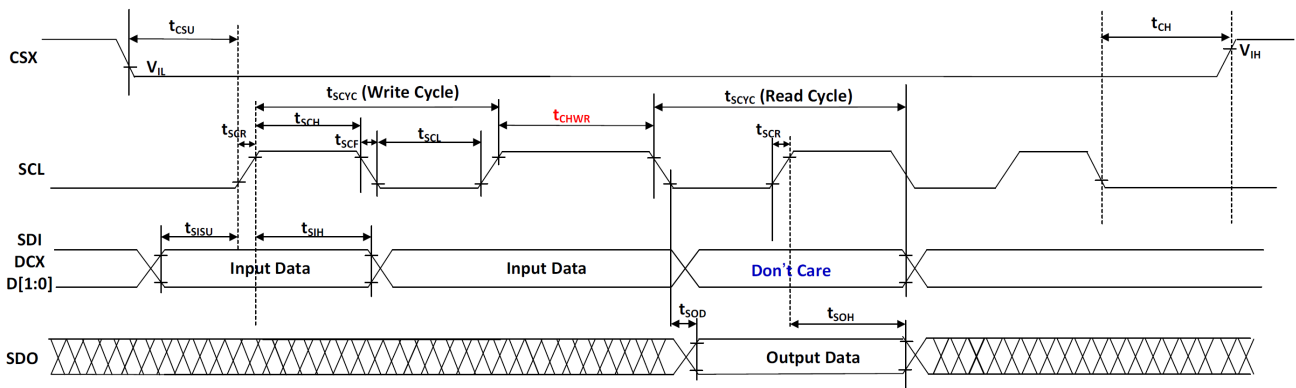
4-wire : Read 8-bit (UCS read command : 8-bit para)



4-wire : Read 24-bit (UCS read command 04h : 24-bit para)



8.3.3 QSPI Interface Characteristics



Note: The max SCL frequency for each pixel data format is specified as the below table.

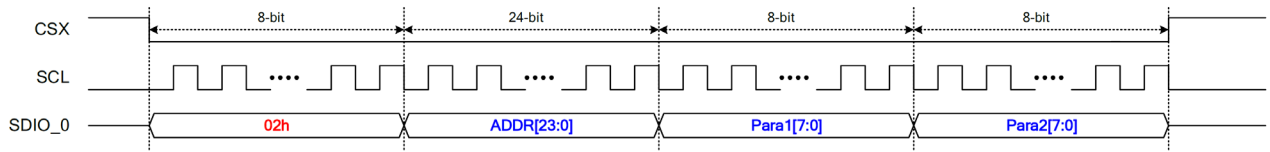
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V

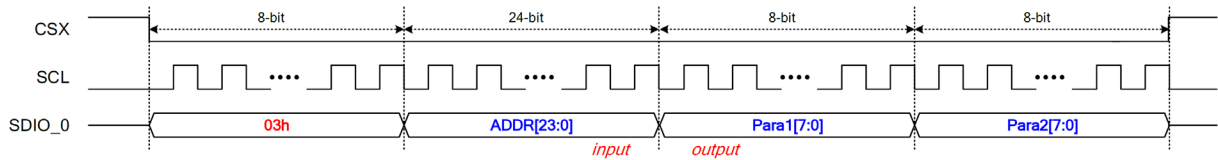
QSPI Timing

Quad SPI Interface Protocol – Register Read and Write

Command Write

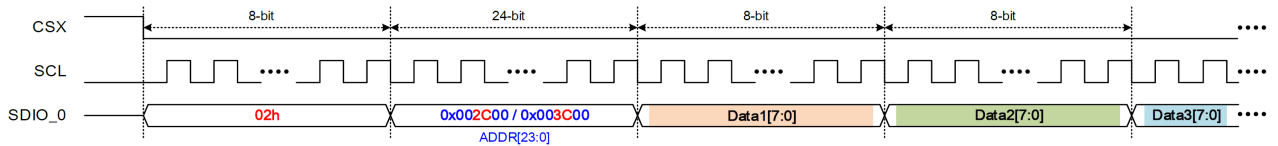


Command Read

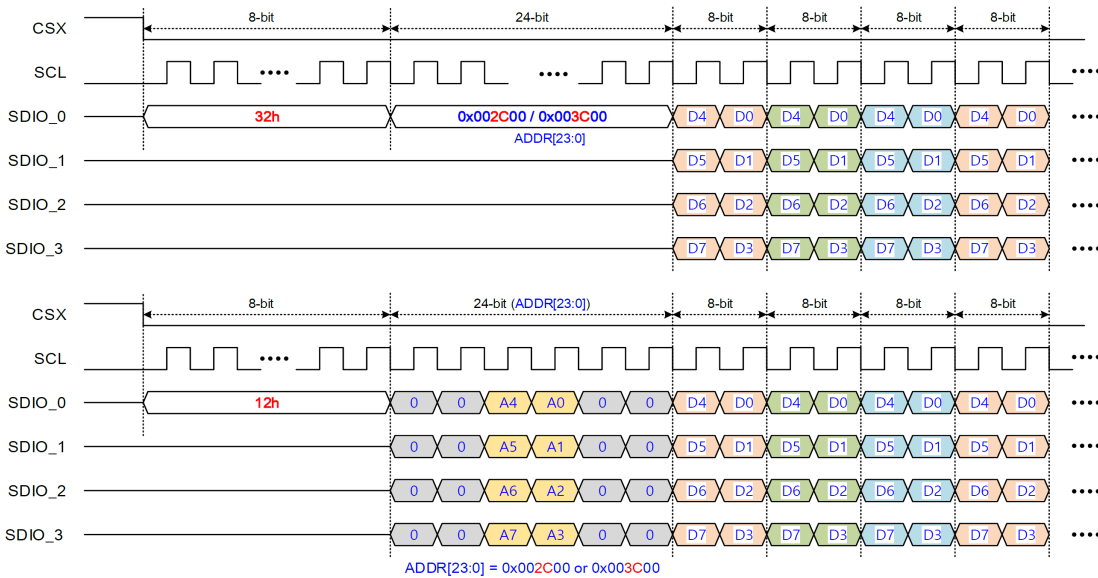


Quad SPI Interface Protocol – Pixel Interface

1-Wire Pixel Write

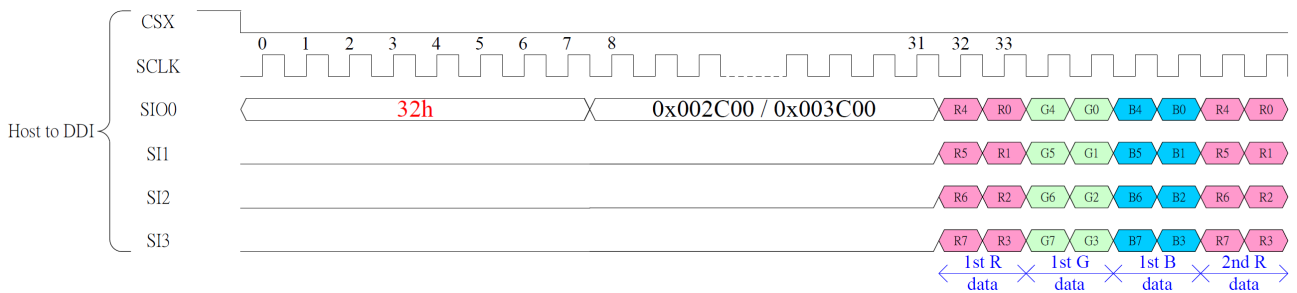


4-Wire Pixel Write

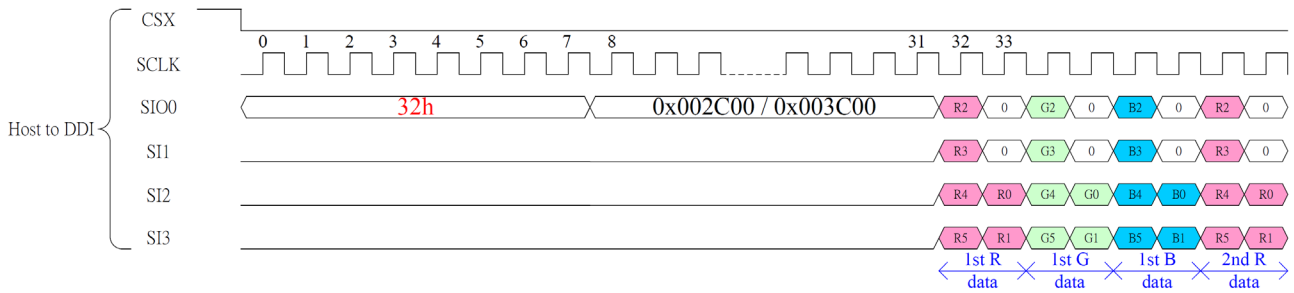


SPI-4Lanes Pixel Write Data Waveform

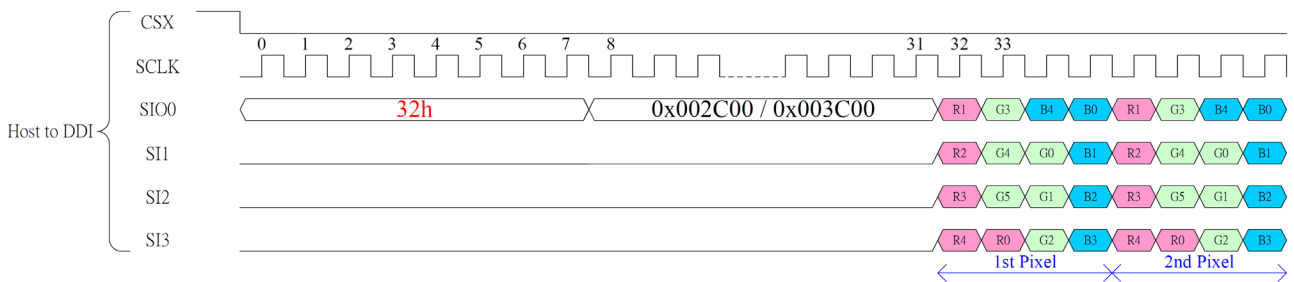
RGB888 – 4-Lanes



RGB666 – 4-Lanes

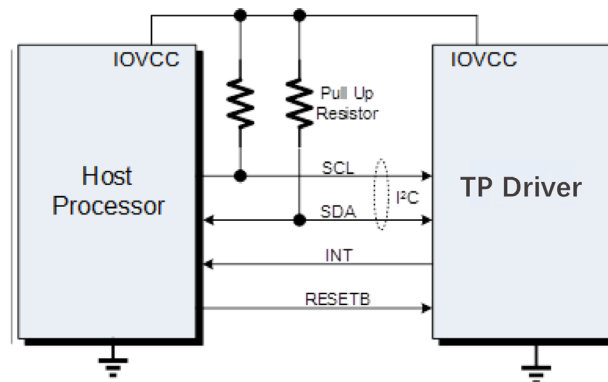


RGB565 – 4-Lanes

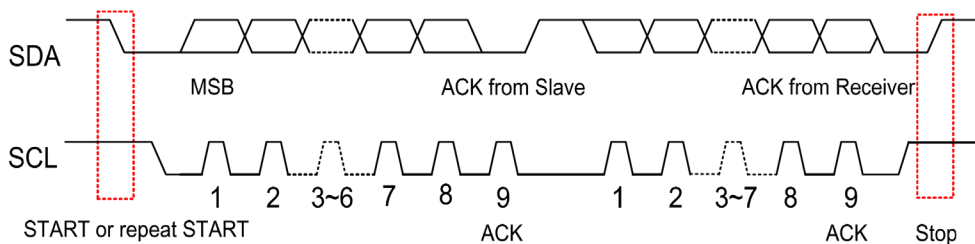


8-4 Touch Panel(TP) IIC Timing Characteristics

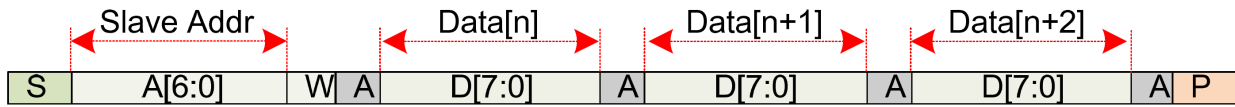
The TP driver communicates to the host through the IIC interface and follows the IIC protocol. IIC bus utilize the SCL and SDA, a two-wire synchronous communication interface and can operate at a maximum bit rate of 400kbps.



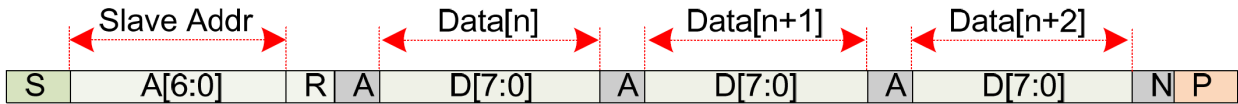
IIC Serial Data Transfer Format



IIC Interface Timing



IIC Master Write, Slave Read



IIC Master Read, Slave Write

TP Driver IC Slave Addr A[6:0]---0X38

Mnemonics	Description
S	I ² C Start or I ² C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

IIC Timing Characteristics

Parameter	Standard Mode		Fast Mode		Unit
	Min	Max	Min	Max	
SCL frequency (fast mode support)	0	100	0	400	KHz
Clock low period	4.7	-	1.3	-	us
Clock high period	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	4.7	-	1.3	-	us
Hold time (repeated) START condition	4.0	-	0.6	-	us
Data setup time	250	-	100	-	ns
Setup time for a repeated START condition	4.7	-	0.6	-	us
Setup Time for STOP condition	4.0	-	0.6	-	us

TP I/O Communication Voltage follow IOVCC

TP DC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		$0.7 \times IOVCC$	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	$0.3 \times IOVCC$	V	
Output high -level voltage	VOH	IOH= -0.1mA	$0.7 \times IOVCC$	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	$0.3 \times IOVCC$	V	
I/O leakage current	ILI	Vin=0~AVDD	-1	-	1	μA	
Current consumption (Normal operation mode)	Iopr	AVDD=2.8V Ta=25°C MCLK=15MHz	-	1.5	-	mA	
Current consumption (Monitor mode)	Imon	AVDD=2.8V Ta=25°C MCLK=15MHz	-	30	-	μA	
Current consumption (Sleep mode)	Islp	AVDD=2.8V Ta=25°C	-	10	-	μA	
Power Supply voltage	AVDD		2.8	-	3.6	V	

9. Standard Specification For Reliability

No	Item	Condition	Cycles	Judgment Criterion
1	High Temperature Operation	80°C/ 240hours	10	1. No clearly visible defects or remarkable deterioration of display quality.However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted. 2. No function-related abnormalities.
2	Low Temperature Operation	-30°C/ 240hours	10	
3	High Temperature Storage	85°C/ 240hours	5	
4	Low Temperature Storage	-40°C/ 240hours	5	
5	High Temperature Humidity Operation	60°C/90%RH/ 240hours	5	
6	Thermal Shock	-40°C~85°C / 100cycles	5	

Note: The results must be measured after 2 hours later under room temperature keeping.

- END -