FEATURES

- **Built-in Soft Start Function**
- **All Pins Floating Protection**
- **High Voltage CMOS Process with Excellent ESD Protection**
- **Very Low Start-up Current**
- **Proprietary "Smooth Frequency Foldback" and Burst Mode Operation for Green Mode Operation**
- **Proprietary "Hybrid Frequency Jittering"**
- **Current Mode Control**
- **Built-in Slope Compensation**
- **Leading Edge Blanking (LEB)**
- **Programmable Switching Frequency**
- **Proprietary "Constant Power Limiting"**
- **Audio Noise Free Operation**
- **OVP (Over Voltage Protection) on VDD**
- **OLP (Over Load Protection)**
- **Cycle-by-cycle Current Limiting (OCP)**

APPLICATIONS

Offline AC/DC flyback converter for

- **AC/DC Adaptors**
- **Set-Top Box Power Supplies**
- **ATX Standby Power**
- **Battery Charger**
- **Open-frame SMPS**

GENERAL DESCRIPTION

DP2263 is a high performance, low cost, highly integrated current mode PWM controller for offline flyback converter applications.

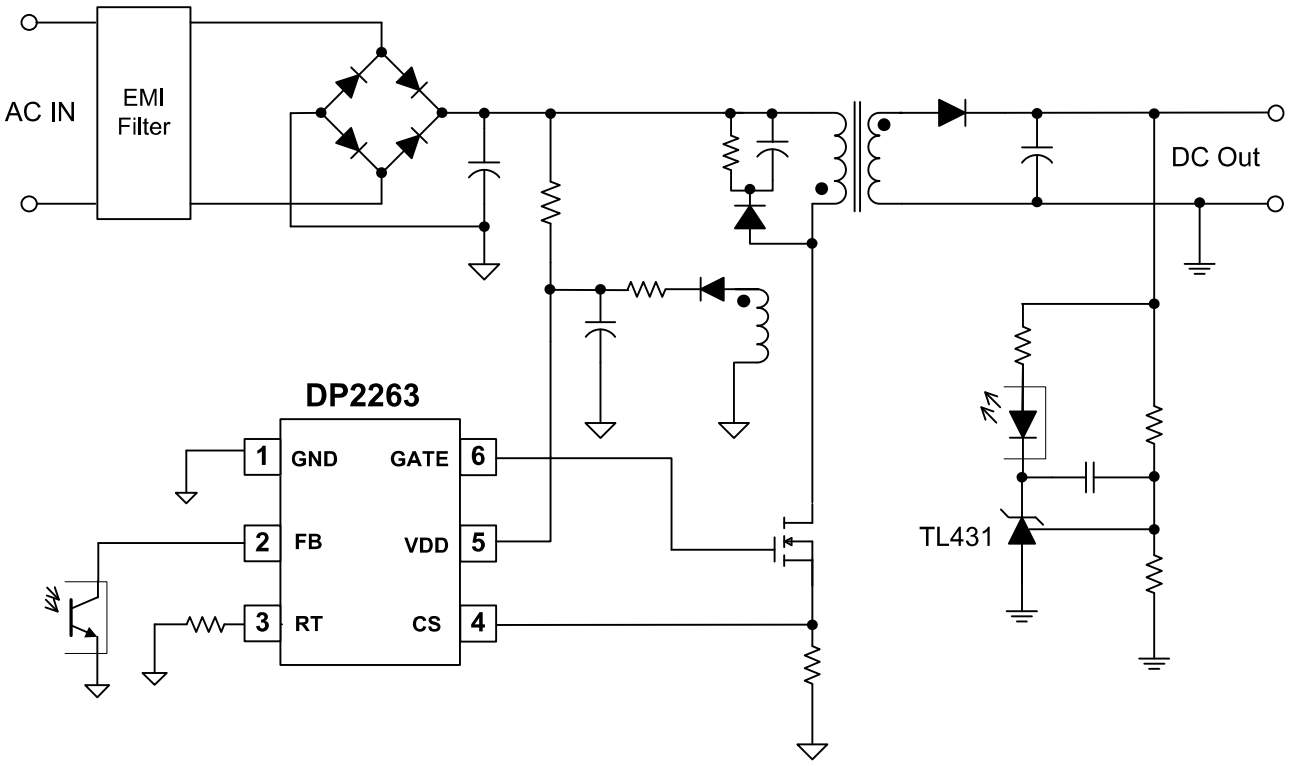
The IC integrates Depuw's Proprietary "Hybrid Frequency Jittering" for the oscillator to reduce conduction EMI emission of a power supply. When the output power demands decrease, the IC enters into Depuw's Proprietary "Smooth Frequency Foldback" for high power conversion efficiency without audio noise generated. When the current set-point falls below a given value, e.g. the output power demand diminishes, the IC automatically enters into burst mode and provides excellent efficiency without audio noise.

The IC has built-in synchronized slope compensation to prevent sub-harmonic oscillation at high PWM duty output. A Proprietary "Constant Power Limiting" block is integrated to achieve constant output power limit over universal AC input range. The IC also has built-in soft start function to soften the stress on the MOSFET during power on period.

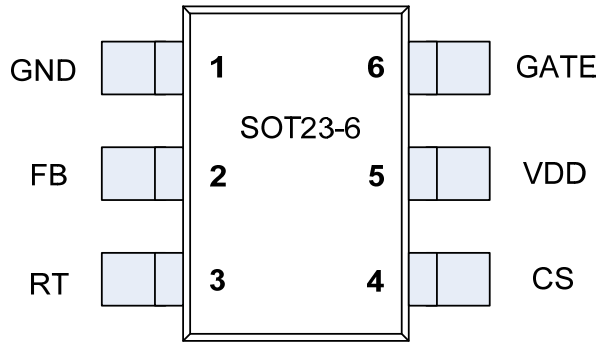
DP2263 integrates functions and protections of Under Voltage Lockout (UVLO), VCC Over Voltage Protection (OVP), Cycle-by-cycle Current Limiting (OCP), Over Load Protection (OLP), All Pins Floating Protection, RT Pin Short-to-GND Protection, Gate Clamping, VCC Clamping, Leading Edge Blanking (LEB).

DP2263 is available in SOT23-6, packages.

TYPICAL APPLICATION



Pin Configuration

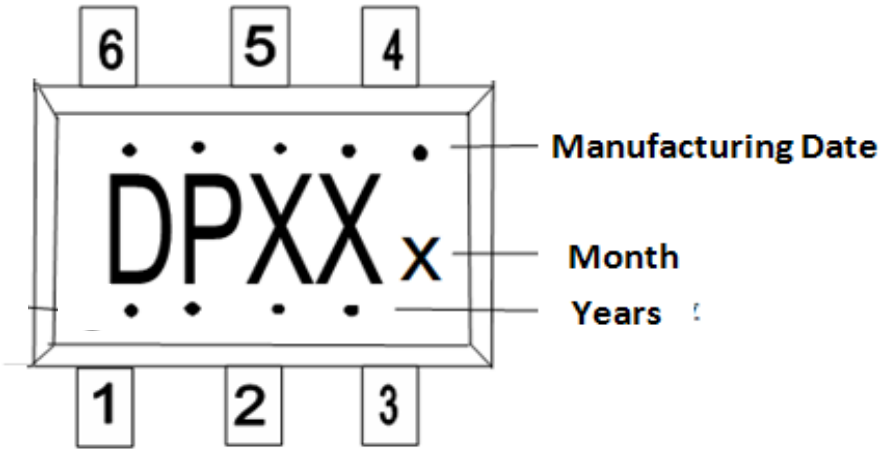


Ordering Information

Part Number	Description
DP2263	SOT23-6, Halogen free ,3000Pcs/Reel

Marking Information

SOT23-6



Description:

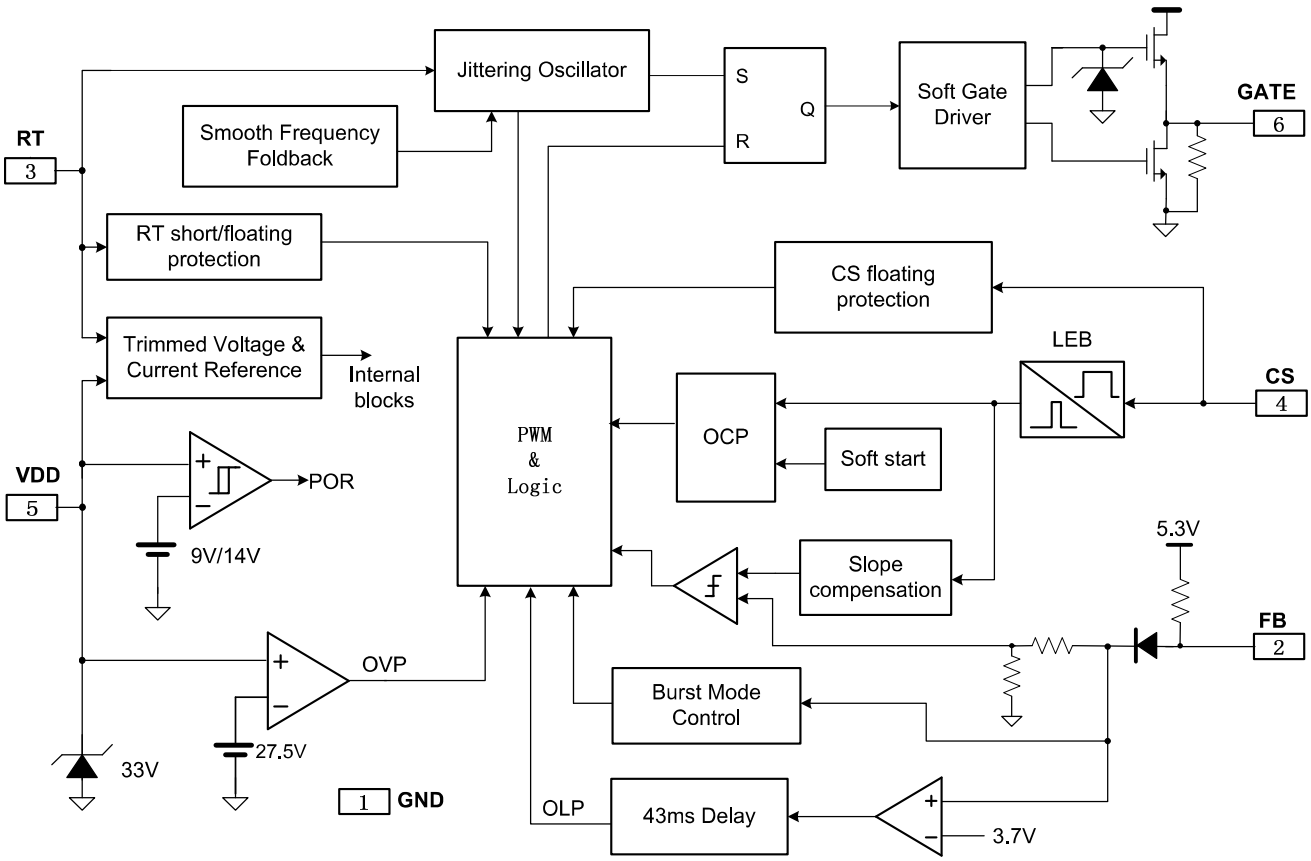
1.1. The first line of the five points represent the assembly house commissioning date, a total of 1-31.

1.2. DPXX for product name: D represent DP brand, P represents the power supply, XX on behalf of the commodity (63: DP2263)

1.3. After the product name, X on behalf of the month, 1-12 months.

1.4. The third row four point on behalf of the last year.

Block Diagram



Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 3.
3	RT	I	Set the switching frequency by connecting a resistor between RT and GND. This pin has floating/short-to-GND protection.
4	CS	I	Current sense input pin.
5	VDD	P	IC power supply pin.
6	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	33	V
VCC DC Clamp Current	10	mA
GATE pin	20	V
FB, RT, CS voltage range	-0.3 to 7	V
Package Thermal Resistance (SOT-26)	250	°C/W
Package Thermal Resistance (DIP-8)	90	°C/W
Package Thermal Resistance (SOP-8)	150	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 25	V
Operating Frequency	50 to 130	kHz
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS

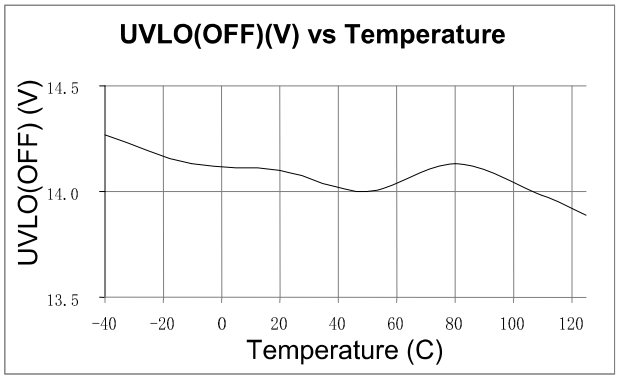
(T_A = 25°C, RT=100K ohm, VDD=18V, if not otherwise noted)

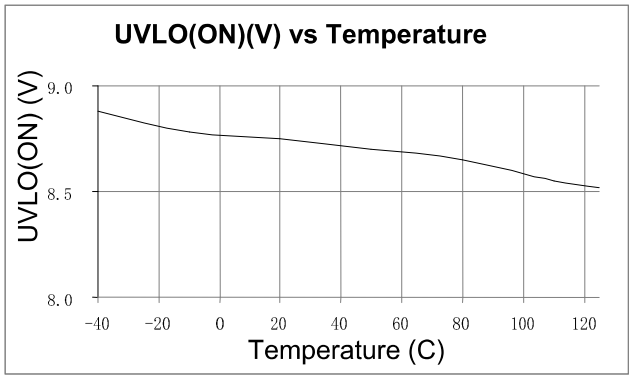
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
I_Startup	VDD Start up Current	VDD =12.5V, Measure current into VDD		5	20	uA
I_VDD_Op	Operation Current	V_{FB}=3V,CL=1nF		2.5	3.5	mA
UVLO(OFF)	VDD Under Voltage Lockout Exit (Startup)		13	14	15	V
UVLO(ON)	VDD Under Voltage Lockout Enter		8	9	10	V
VDD_OVP	VDD Over Voltage Protection trigger		25	27.5	30	V
V_{DD}_Clamp	VDD Zener Clamp Voltage	I(V_{DD}) = 15 mA		33		V
T_Softstart	Soft Start Time			3		mSec
Feedback Input Section(FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		2.0		V/V

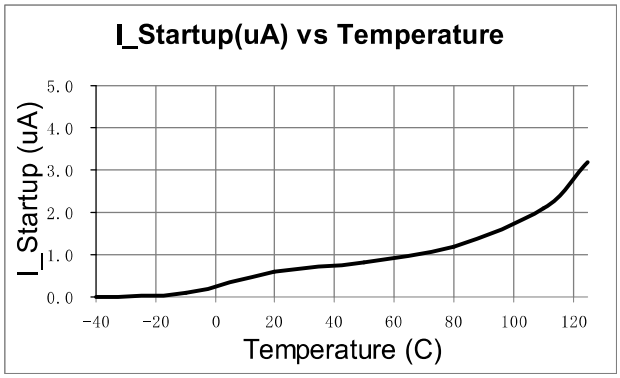
V_{FB}_Open	FB Open Voltage			5.3		V
I_{FB}_Short	FB short circuit current	Short FB pin to GND, measure current		1.1		mA
VFB_min_duty	FB under voltage gate clock is off.			1.0		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			3.7		V
T_D_PL	Power limiting Debounce Time	Note 3		43		mSec
Z_{FB}_IN	Input Impedance			5		Kohm
Current Sense Input Section (CS Pin)						
T_blanking	SENSE Input Leading Edge Blanking Time			250		nSec
Vth_OC_min	Internal current limiting threshold	Zero duty cycle	0.70	0.75	0.80	V
T_D_OC	Over Current Detection and Control Delay	CL=1nF at GATE,		70		nSec
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHZ
ΔF(shuffle)/Fosc	Frequency shuffling range	Note 4	-4		4	%
Δf_Temp	Frequency Temperature Stability	-20°C to 100°C (Note 4)		5		%
Δf_VDD	Frequency Voltage Stability	VDD = 12-25V,		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
RT_range	Operating RT Range		50	100	150	Kohm
V_RI_open	RI open voltage			2.0		V
F_BM	Burst Mode Base Frequency			22		KHZ
Gate Drive Output						
VOL	Output Low Level	Io = 20 mA (sink)			1	V
VOH	Output High Level	Io = 20 mA (source)	7.5			V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		17.5		V
T_r	Output Rising Time	CL = 1nF		200		nSec
T_f	Output Falling Time	CL = 1nF		60		nSec

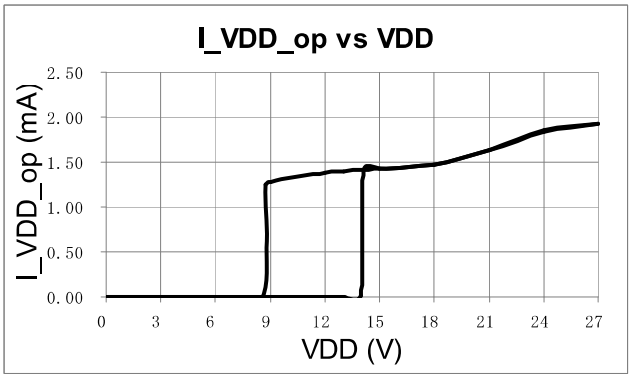
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2. The device is not guaranteed to function outside its operating conditions.
Note 3. The OLP debounce time is proportional to the period of switching cycle.
Note 4. Guaranteed by design.

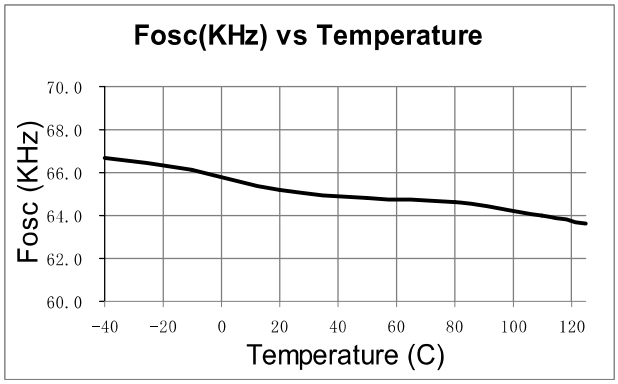
CHARACTERIZATION PLOTS

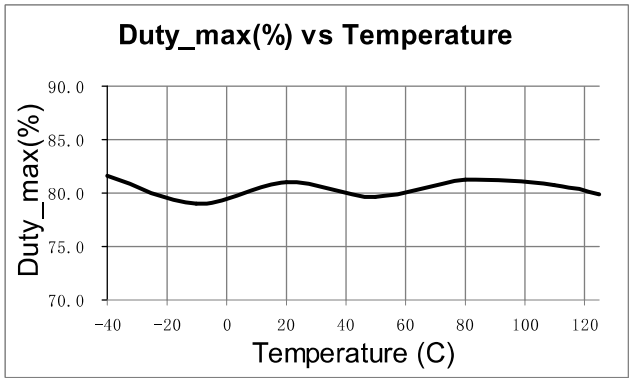


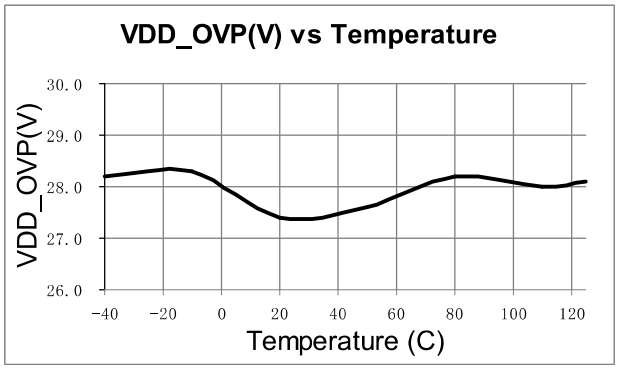


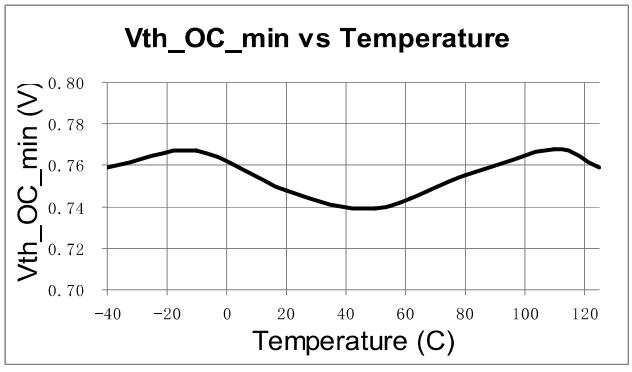


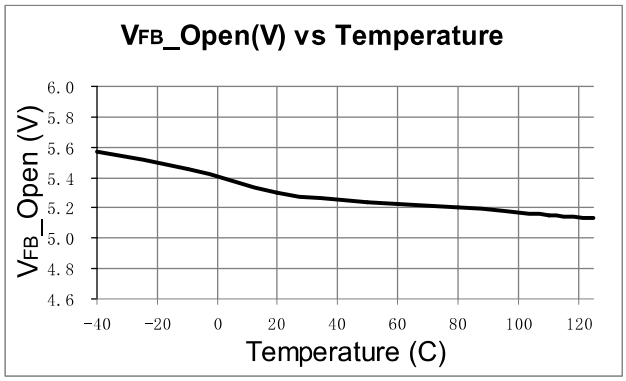


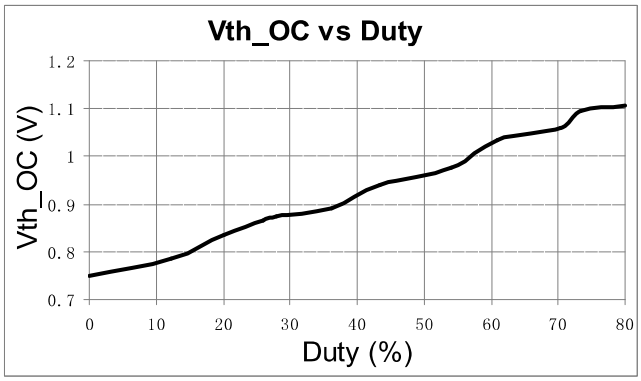


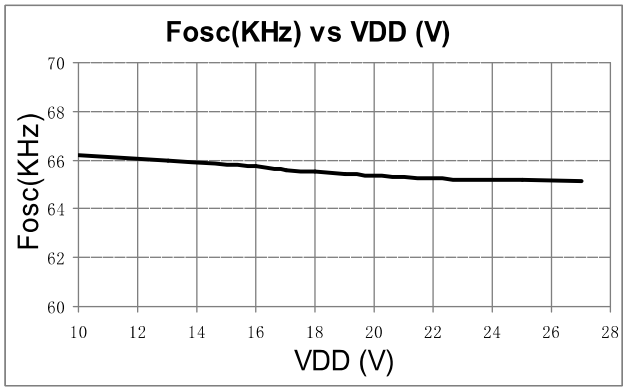


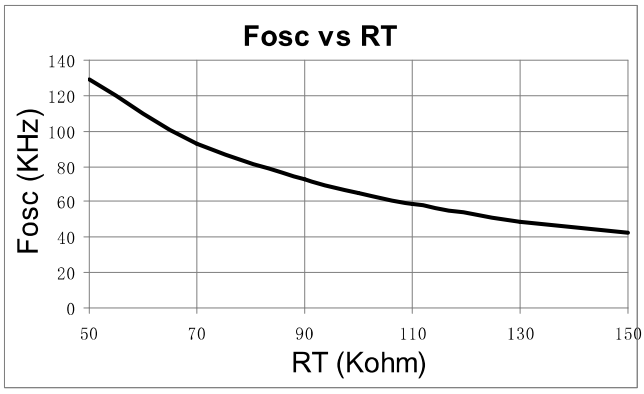





VFB_Open(V) vs Temperature
VFB_Open (V)
6.0
5.8
5.6
5.4
5.2
5.0
4.8
4.6
-40
-20
0
20
40
60
80
100
120
Temperature (C)


Vth_OC vs Duty
Vth_OC (V)
1.2
1.1
1
0.9
0.8
0.7
0
10
20
30
40
50
60
70
80
Duty (%)


Fosc(KHz) vs VDD (V)
Fosc(KHz)
70
68
66
64
62
60
10
12
14
16
18
20
22
24
26
28
VDD (V)


Fosc vs RT
Fosc (KHz)
140
120
100
80
60
40
20
0
50
70
90
110
130
150
RT (Kohm)

OPERATION DESCRIPTION

The DP2263 is a high performance, low cost, highly integrated current mode PWM controller for offline flyback converter applications. The built-in advanced energy saving with high level protection features improves the SMPS reliability and performance without increasing the system cost.

- **Under Voltage Lockout (UVLO) and Startup Operation**

Fig.1 shows a typical startup circuit for DP2263 application. Before the IC begins switching operation, it consumes only startup current (typically 5uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 14V(typical), DP2263 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The UVLO hysteresis window can provide adequate holdup time, which allows using small capacitor for VDD. The selection of Rst and Cdd should be a trade off between the power loss and startup time.

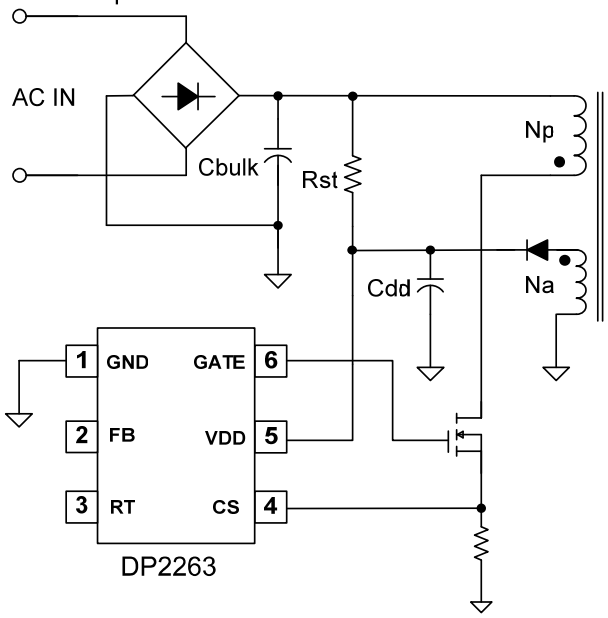


Fig.1

- **Soft Start**

DP2263 features an internal 3ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limit comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

- **Oscillator with "Hybrid Frequency Jittering"**

Connect a resistor from RT pin to GND according to the equation below to program the normal switching frequency:

$$F_{OSC}(KHz) = \frac{6500}{RT(K\Omega)}$$

It can typically operate between 50kHz to 130kHz. To improve system EMI performance, DP2263 integrates proprietary "Hybrid Frequency Jittering" to operate the system with ±4% frequency jittering around setting frequency.

- **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (350ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

- **Built-in Slope Compensation**

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In DP2263, the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Constant Power Limiting**

In DP2263, a Proprietary "Constant Power Limiting" block is integrated to achieve constant max. output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

- **Green Mode Operation**

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To fulfill green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

Smooth Frequency Folback

In DP2263, a Proprietary "Smooth Frequency Foldback" block is integrated to foldback the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, Depuw's proprietary "Smooth

frequency foldback" block can reduce the PWM frequency smoothly without audible noise.

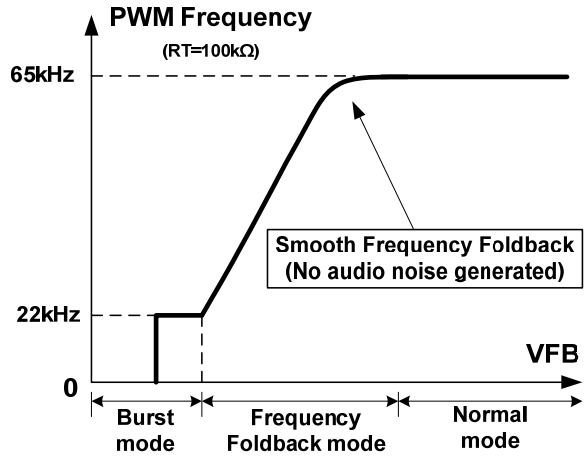


Fig.2

Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, DP2263 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

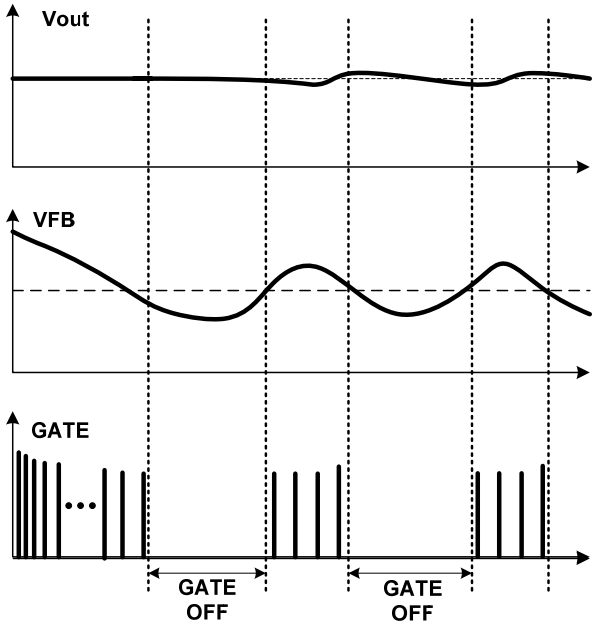


Fig.3

● Gate Drive

The output stage of DP2263 is a fast totem-pole gate driver with 300mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 17.5V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

● Protections

DP2263 provides many protections that can protect system from being damaged and enhance the system reliability. All the protections are listed as below:

Auto Recovery Mode Protection

As shown in Fig.4, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. The system begins switching when VDD reaches to UVLO(on) (typical 14V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

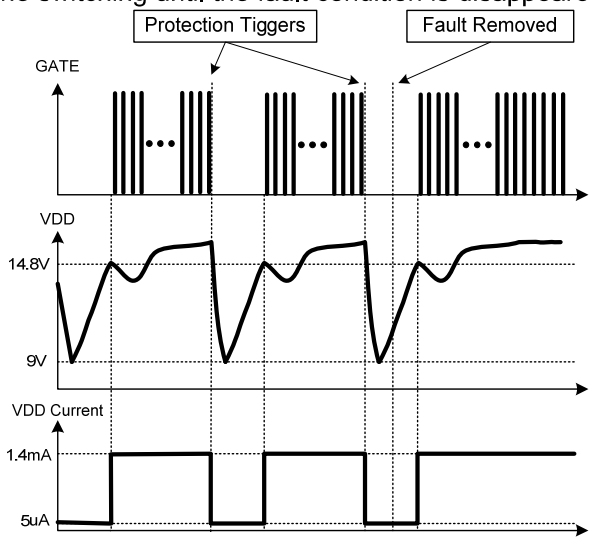


Fig.4

Over Load Protection (OLP)

When over load occurs, a fault is detected. If this fault is present for more than 43ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 43mS delay time is to prevent the false trigger from the power-on and turn-off transient

All Pins Floating and RT Pin Short-to-GND Protection

In DP2263, if CS and RT pin floating or RT pin short-to-GND occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

VDD OVP (Over Voltage Protection)

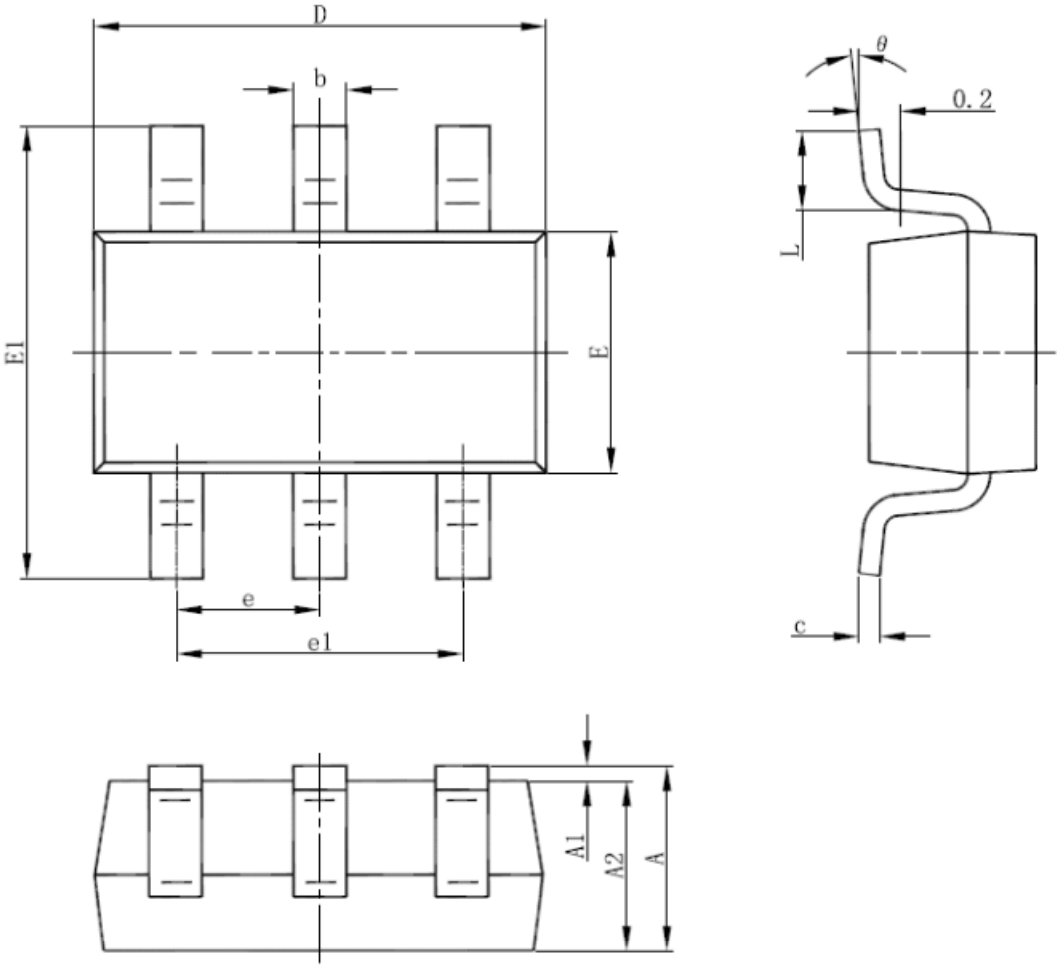
VDD OVP (Over Voltage Protection) is

implemented in DP2263 and it is a protection of auto-recovery mode.

Cycle-by-Cycle Current Limiting
It is a basic protection and can be implemented easily in current mode PWM controller.

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.047
A1	0.000	0.150	0.000	0.006
A2	0.900	1.100	0.035	0.043
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°