DP2283

High Performance Current Mode PWM Controller

FEATURES

- **Low Standby Power <80mW@230V**
- **Low Start-up Current <5uA for Fast Startup**
- **Proprietary "Smooth Frequency Fold-back" and Burst Mode Operation for Green Mode Operation**
- **Audio Noise Free Operation**
- **Proprietary "Hybrid Frequency Jittering"**
- **Programmable Switching Frequency**
- **Proprietary "Constant Power Limiting"**
- **Built-in Protections:**
  - **CS Pin Floating Protection**
  - **Over Voltage Protection (OVP) on VDD**
  - **Over Load Protection (OLP)**
  - **Cycle-by-cycle Current Limiting**
  - **Leading Edge Blanking**
  - **Soft Start Function**
  - **Slope Compensation**
- **RoHS Compliant and Halogen Free**
- **Available with SOT23-6 and DIP8 Package**

APPLICATIONS

- **AC/DC Adaptors**
- **Set-Top Box Power Supplies**
- **ATX Standby Power**
- **Battery Charger**
- **Open-frame SMPS**

GENERAL DESCRIPTION

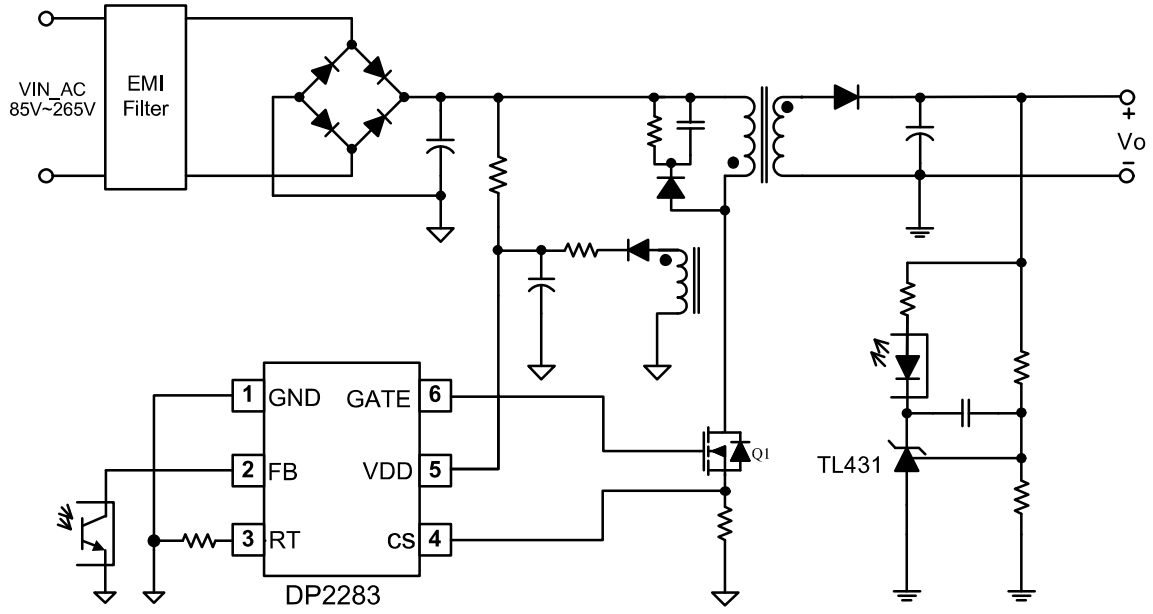
DP2283 is a high performance, low cost, highly integrated current mode PWM controller for offline adapter applications.

The DP2283 is integrated with Depuw's Proprietary "Hybrid Frequency Jittering" for the oscillator to reduce conduction EMI emission of the power supply. When the output power demands decrease, the IC enters into Depuw's Proprietary "Smooth Frequency Fold-back" for high power conversion efficiency without audio noise generated. When the current set-point falls below a given value; the IC automatically enters into burst mode and provides excellent efficiency without audio noise.

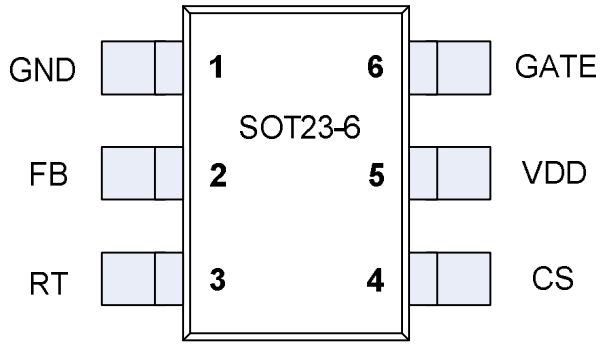
The DP2283 has built-in synchronized slope compensation to prevent sub-harmonic oscillation at high PWM duty output, a Proprietary "Constant Power Limiting" block to achieve constant output power limit over universal AC input range, and the soft start function to soften the stress on the MOSFET during power on period.

DP2283 integrates functions and protections of VDD UVLO, VDD OVP, Cycle-by-cycle Current Limiting (OCP), Over Load Protection (OLP), all Pins Floating Protection, RT Pin Short-to-GND Protection and Leading Edge Blanking (LEB).

TYPICAL APPLICATION



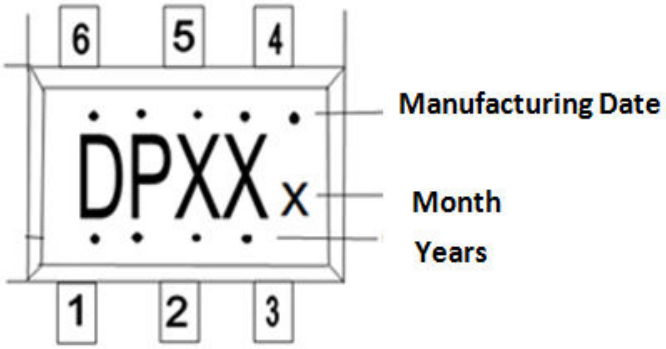
Pin Configuration



Ordering Information

Part Number	OVP	OLP	Description
DP2283	A/R	A/R	SOT23-6, Halogen free 3000/Reel

Marking Information



Description:

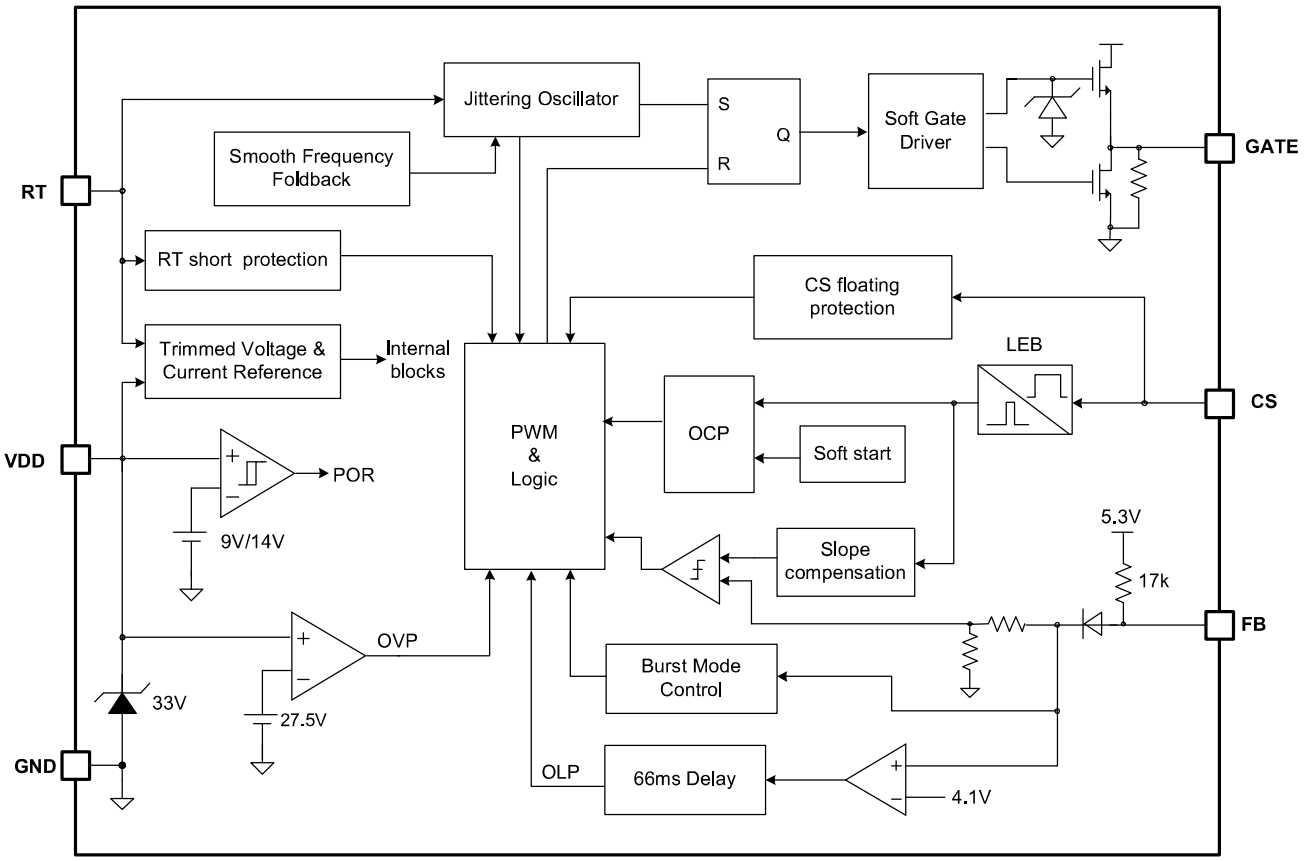
1.1. The first line of the five points represent the assembly house commissioning date, a total of 1-31.

1.2. DPXX for product name: D represent DP brand, P represents the power supply, XX on behalf of the commodity (83: DP2283)

1.3. After the product name on behalf of the month, 1-12 months.

1.4. The third row four point on behalf of the last year.

Block Diagram



Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground of the chip.
2	FB	I	Voltage feedback Pin. The loop regulation is achieved by connecting a photo-coupler to this Pin. PWM duty cycle is determined by this Pin voltage and the current sense signal at CS Pin.
3	RT	I	Set the switching frequency by connecting a resistor between RT Pin and GND Pin. This Pin has short-to-GND protection with auto-recovery mode. RT Pin is floated with nominal switching frequency at 50kHz.
4	CS	I	Current sense input Pin.
5	VDD	P	IC power supply Pin.
6	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	33	V
VCC DC Clamp Current	10	mA
GATE Pin	16	V
FB, RT, CS voltage range	-0.3 to 7	V
Package Thermal Resistance (SOT23-6)	250	°C/W

Package Thermal Resistance (DIP-8)	90	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3000	V
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 25	V
Operating Frequency	50 to 130	kHz
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, RT=100K ohm, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
I_Startup	VDD Start up Current	VDD =12.5V, Measure current into VDD		5		uA
I_VDD_Op	Operation Current	VDD=16V, V_{FB}=3.3V,CL=1nF			2.6	mA
UVLO(OFF)	VDD Under Voltage Lockout Exit (Startup)			14		V
UVLO(ON)	VDD Under Voltage Lockout Enter			9		V
VDD_OVP	VDD Over Voltage Protection trigger		25	27.5	30	V
V_{DD}_Clamp	VDD Zener Clamp Voltage	I(V_{DD}) = 8 mA		33		V
T_Softstart	Soft Start Time	Note 3		3		mSec
Feedback Input Section(FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		4.0		V/V
V_{FB}_Open	FB Open Voltage			5.3		V
I_{FB}_Short	FB short circuit current	Short FB Pin to GND, measure current		0.3		mA
VFB_ZDC	FB under voltage gate clock is off.			1.95		V

ZDC hysteresis	Zero duty cycle hysteresis			0.15		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.1		V
T_D_PL	Power limiting Debounce Time	Note 3		66		mSec
Z_{FB}_IN	Input Impedance			17		Kohm
Current Sense Input Section (CS Pin)						
T_blanking	SENSE Input Leading Edge Blanking Time			250		nSec
Vth_OC_min	Internal current limiting threshold	Zero duty cycle		0.36		V
Vth_OC_min	Internal current limiting threshold	55% duty cycle		0.6		V
T_D_OC	Over Current Detection and Control Delay	CL=1nF at GATE,		70		nSec
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency	RT=100k ohm (Note 4)		65		KHZ
ΔF(shuffle)/Fosc	Frequency shuffling range	Note 4	-4		4	%
Δf_Temp	Frequency Temperature Stability	-20°C to 100 °C (Note 4)		5		%
Δf_VDD	Frequency Voltage Stability	VDD = 12-25V,		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
RT_range	Operating RT Range		50	100	150	Kohm
V_RI_open	RI open voltage			2.0		V
F_BM	Burst Mode Base Frequency			22		KHZ
Gate Drive Output						
VOL	Output Low Level	Io = 20 mA (sink)			1	V

VOH	Output High Level	Io = 20 mA (source), VDD=9V		8.5		V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		13.5		V
T_r	Output Rising Time	CL = 1nF		150		nSec
T_f	Output Falling Time	CL = 1nF		75		nSec
OLP /OVP Latch up						
VDD_RL	Threshold voltage for Latch-up release	Optional for some part number		0.6		V
Over Temperature						
TSD	Over Temperature Shut Down			135		°C
TSD_RC	Over Temperature Recovery			80		°C

Note1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2. The device is not guaranteed to function outside its operating conditions.

Note3. The OLP debounce time is proportional to the period of switching cycle.

Note4. Guaranteed by design

OPERATION DESCRIPTION

The DP2283 is a high performance, low cost, highly integrated current mode PWM controller for offline flyback converter applications. The built-in advanced energy saving with high level protection features improves the SMPS reliability and performance without increasing the system cost.

- **Under Voltage Lockout (UVLO) and Startup Operation**

Fig.1 shows a typical startup circuit for DP2283 application. Before the IC begins switching, it consumes only startup current (typically 5uA) and the current flowing through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 14V (typical), DP2283 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The UVLO hysteresis window can provide adequate holdup time, which allows using small capacitor for VDD. The selection of Rst and Cdd should be a tradeoff between the power loss and startup time.

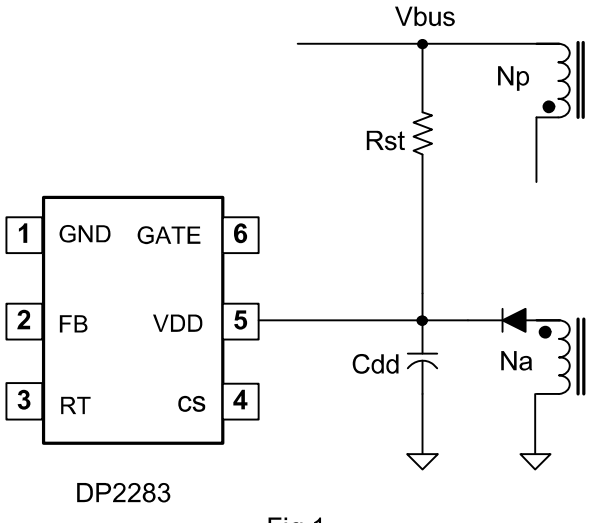


Fig.1

- **Soft Start**

DP2283 features an internal 3ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limit during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by the soft start activation.

- **Oscillator with "Hybrid Frequency Jittering"**

Connect a resistor from RT Pin to GND Pin according to the equation below to program the normal switching frequency:

$$F_{OSC}(KHz) = \frac{6500}{RT(K\Omega)}$$

It can typically operate between 50 kHz to 130 kHz. To improve system EMI performance, DP2283 integrates proprietary "Hybrid Frequency Jittering" to operate the system with ±4% frequency jittering around setting frequency.

- **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (350ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

- **Built-in Slope Compensation**

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In DP2283, the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Constant Power Limiting**

In DP2283, a Proprietary "Constant Power Limiting" block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

- **Green Mode Operation**

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

Smooth Frequency Fold-back

In DP2283, a Proprietary "Smooth Frequency Fold back" block is integrated to fold back the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, Depuw's proprietary "Smooth frequency fold back" block can reduce the PWM frequency smoothly without audible noise.

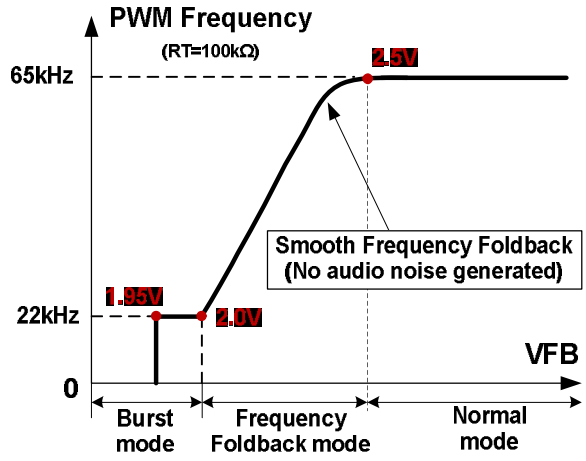


Fig.2

Burst Mode Control

When the loading is very small, the system enters burst mode. When VFB drops below VFB_ZDC, DP2283 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above VFB_ZDC, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

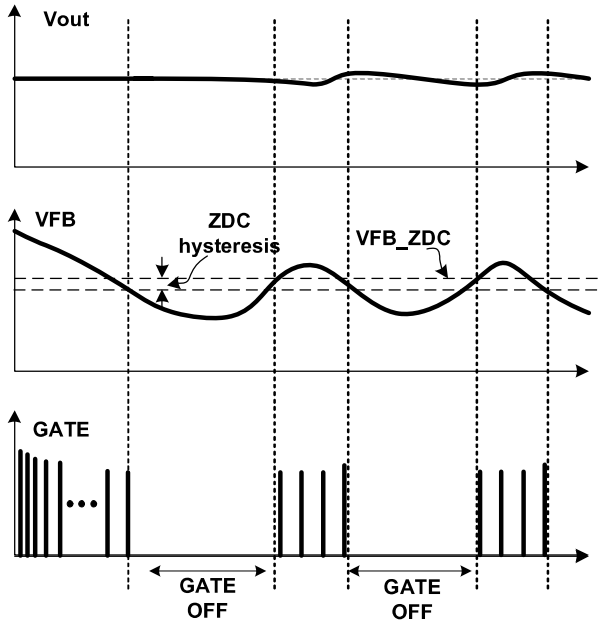


Fig.3

- **Gate Drive**

The output stage of DP2283 is a fast totem-pole gate driver with 300mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 13.5V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

- **Fault Protection**

DP2283 provides many protections that can protect system from being damaged and enhance the system reliability. All the protections are listed as below:

Auto Recovery Mode Protection

As shown in Fig.4, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO (off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. The system begins switching when VDD reaches to UVLO (on) (typical 14V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

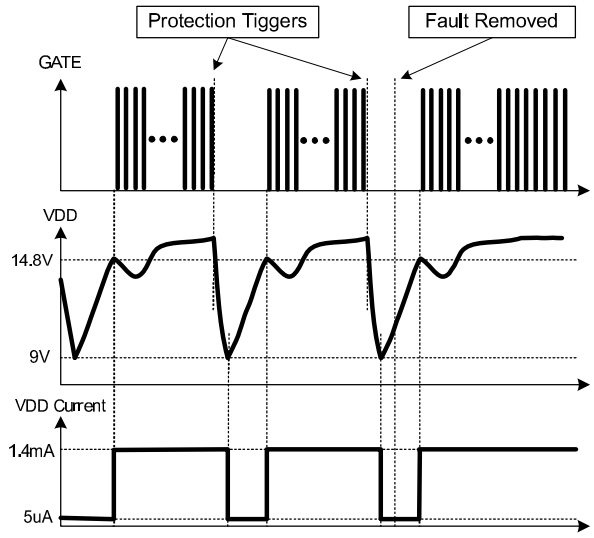


Fig.4

Latch-up Mode Protection

Once a fault condition is detected, it may enter the latch-up mode. In this mode, PWM switching will stop, and the system cannot restart until the VDD voltage drops below 4V. It means that the protection is not reset when VDD falls to UVLO (off) (typical 9V). Typically the input power source has to be shut down to let VDD drop below 4V in order to reset the protection. Below is the table for the operational mode under protections:

Part Number	OVP	OLP
DP2283	A/R	A/R

Over Load Protection (OLP)

When over load occurs, a fault is detected. If this fault is present for more than 66ms (typical), the protection will be triggered, DP2283 will experience an auto-recovery mode protection as mentioned above. The 66mS delay time is to prevent the false trigger from the power-on and turn-off transient. For DP2283B, OLP will trigger the latch-up, and the input power has to be disconnected in order to reset

VDD Over Voltage Protection (OVP)

VDD Over Voltage Protection (OVP) is implemented in DP2283 and it is a protection of auto-recovery mode. For DP2283 A/B, OVP will trigger the latch-up, and the input power has to be disconnected in order to reset

All Pins Floating and RT Pin Short-to-GND Protection

In DP2283, if CS and RT Pin floating or RT Pin short-to-GND occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

Cycle-by-Cycle Current Limiting

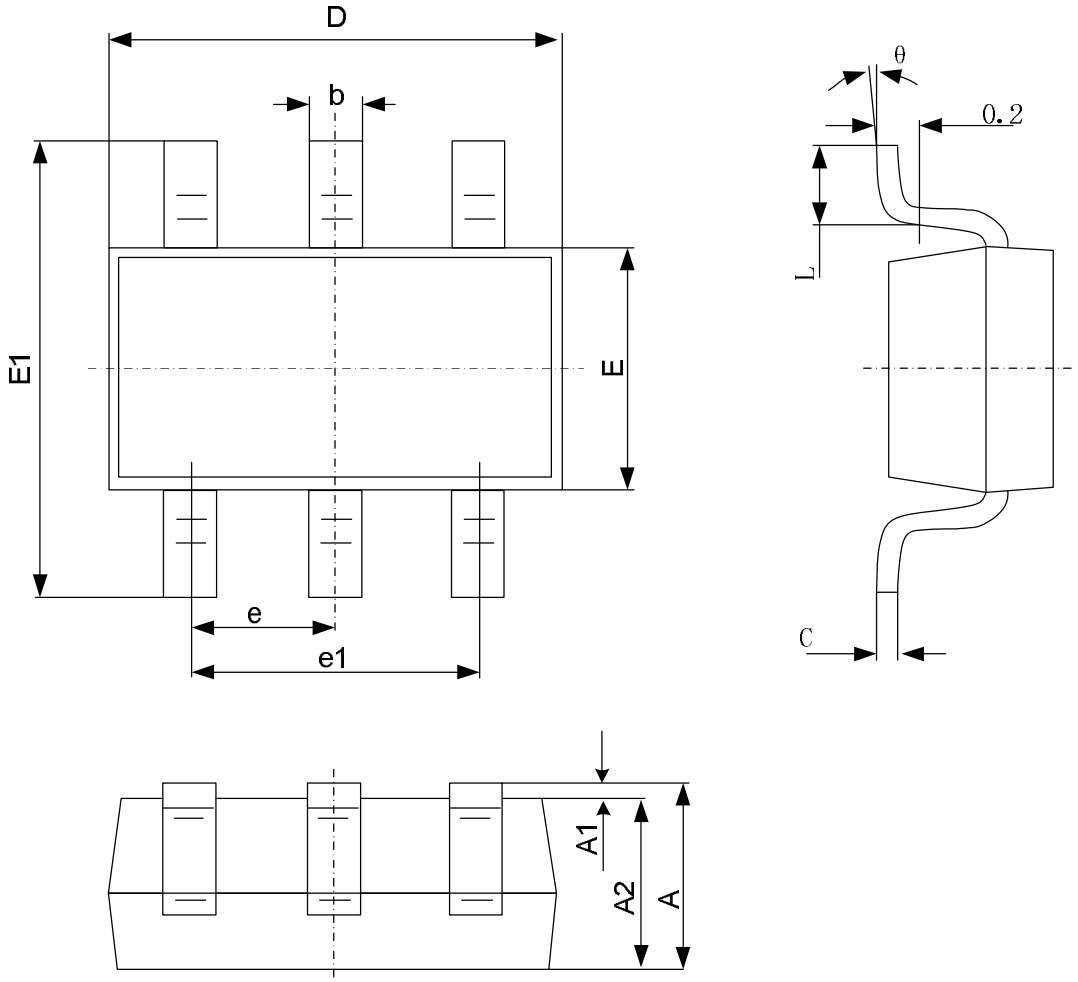
It is a basic protection and can be implemented easily in current mode PWM controller.

Over Temperature Protection

When the IC temperature is over 135 °C, the IC shuts down. Only when the IC temperature drops to 80 °C, IC will restart.

Package Dimension

SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.047
A1	0.000	0.150	0.000	0.006
A2	0.900	1.100	0.035	0.043
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°