GENERAL DESCRIPTION

DP2540A is a high performance offline PWM power switch for low power AC/DC charger and adapter applications.It operates in primary-side sensing and regulation.Consequently, opto-coupler and TL431 could be eliminated. High Precision Constant Voltage (CV) and Constant Current (CC) control are integrated as shown in the figure below. In CC control, the current and output power setting can be adjusted externally by the sense resistor Rs at CS pin. In CV control, multi-mode operations are utilized to achieve high performance and high efficiency. In addition, good load regulation is achieved by the built-in Cable Drop Compensation. Device operates in PFM in CC mode as well at large load condition and it operates in PWM with frequency reduction at light/medium load. The chip consumes very low operation current, it can achieve less than 75mW standby power.

DP2540A offers comprehensive protection coverage with auto-recovery features including Cycle-by-Cycle current limiting, VDD Over Voltage Protection (VDD OVP), short circuit protection, built-in leading edge blanking, VDD under voltage lockout (UVLO), OTP, etc.

High precision constant voltage (CV) and constant current (CC) can be achieved by DP2540A.

DP2540A is offered in DIP7/SOP7 package.

FEATURES

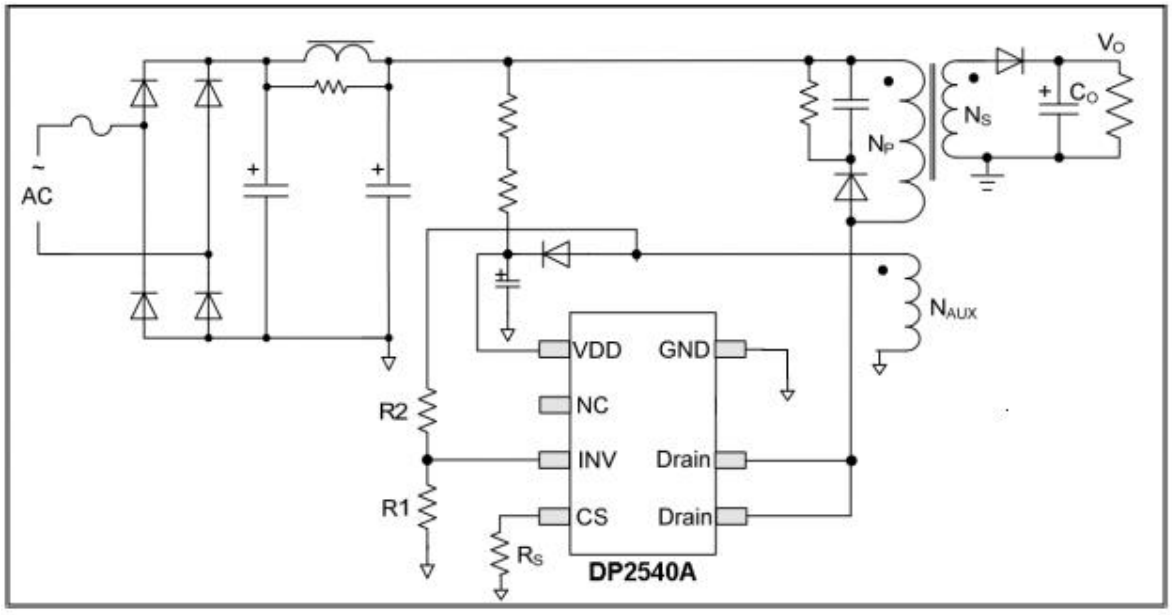
- ± 5% Constant Voltage Regulation and Current Regulation at Universal AC Input
- Primary Side Regulation (PSR) Without TL431 and Opto-coupler
- No Need for Control Loop Compensation
- Programmable CV and CC Regulation
- Multi-Mode PWM/PFM Operation
- Output Short Load Protection
- Less than 75mW Standby Power
- Built-in Line Voltage and Primary Winding Inductance Compensation
- Built-in Adaptive Current Peak Regulation
- Programmable Cable Drop Compensation
- Audio Noise Free Operation
- Built-in Over Temperature Protection (OTP)
- Soft Gate Driver for Good EMI Performance
- Built-in Leading Edge Blanking (LEB)
- Cycle-by-Cycle Current Limiting
- VDD Under Voltage Lockout with Hysteresis (UVLO)
- VDD OVP & Clamp

APPLICATIONS

Low Power AC/DC offline SMPS for

- Cell Phone Charger
- Digital Camera Charger
- Small Power Adapter
- Auxiliary Power for PC, TV etc.
- Linear Regulator/RCC Replacement

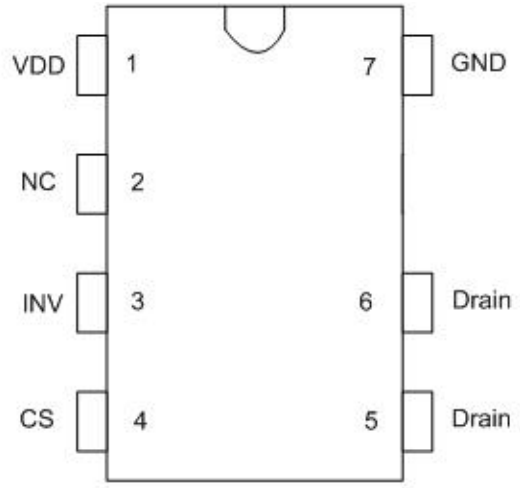
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of DIP7 /SOP7 package is shown as below.



Ordering Information

Part Number	Description
DP2540A	DIP7, Rohs, 50Pcs/Tube SOP7, Halogen free,3000PCS/Reel

Package Dissipation Rating

Package	RθJA (℃/W)
DIP7/SOP7	75/90

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (off state)	-0.3 to 650V
VDD Zener Clamp Voltage	V_{DD_Clamp}
VDD Clamp Continuous Current	10 mA
CS Input Voltage	-0.3 to 7V
INV Input Voltage	-0.3 to 7V
Maximum Operating Junction Temperature T_J	150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Marking Information

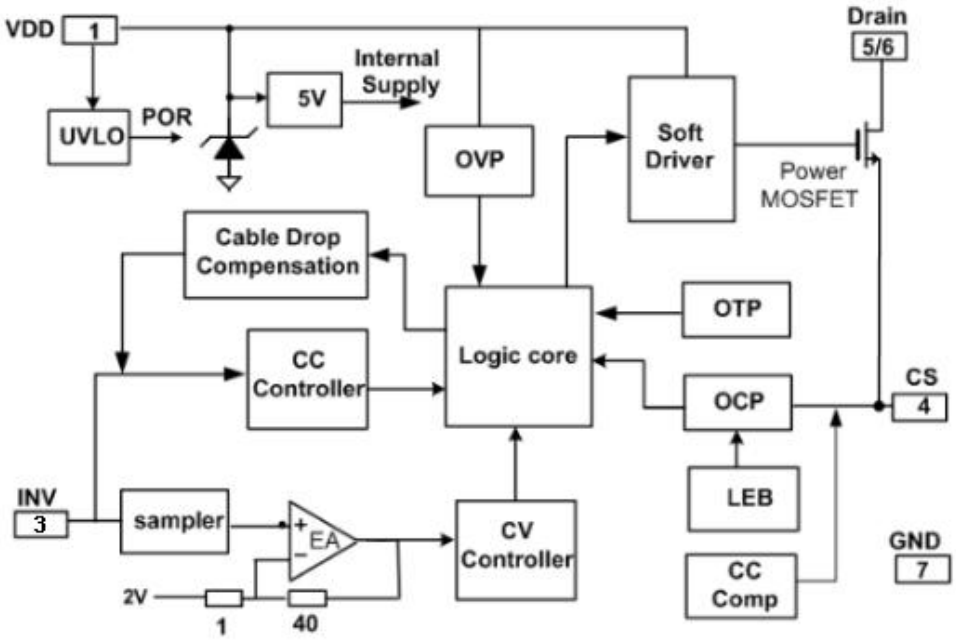
DP2540A for product name;

XXXXXX the first X reresents the last year,2016 is 6; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	VDD	P	Power supply.
2	NC	-	No connect.
3	INV	I	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
4	CS	I	Current sense input.
5/6	Drain	O	The Power MOSFET Drain
7	GND	P	Ground.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

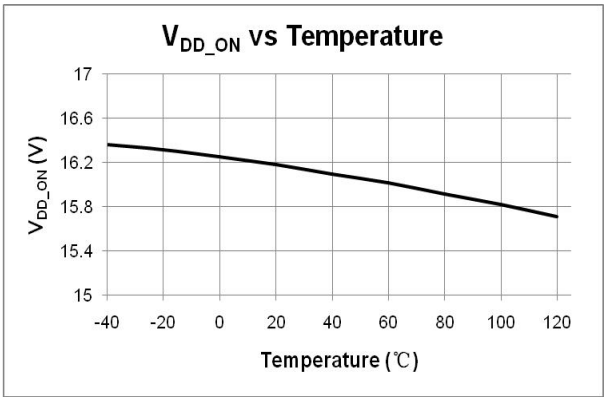
Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	11	27	V
T_A	Operating Ambient Temperature	-40	85	°C

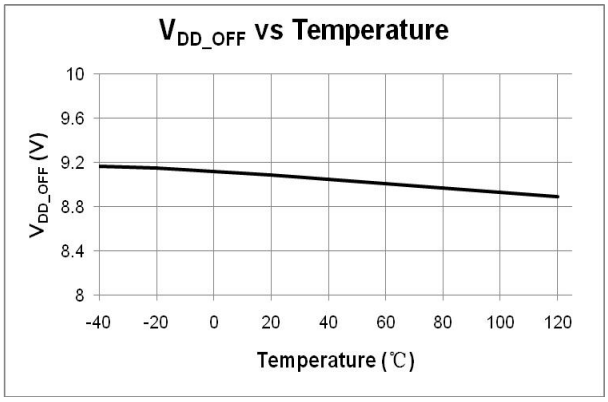
ELECTRICAL CHARACTERISTICS

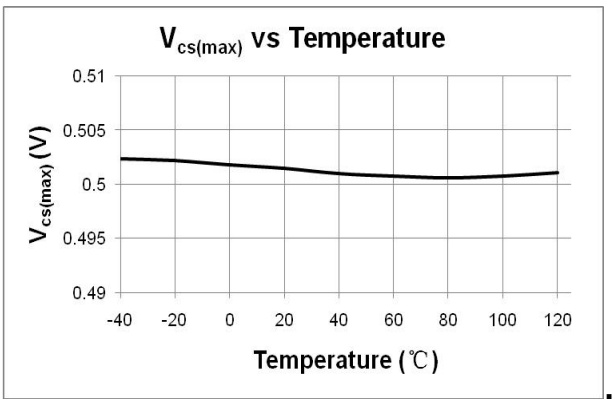
(T_A = 25°C, VDD=18V if not otherwise noted)

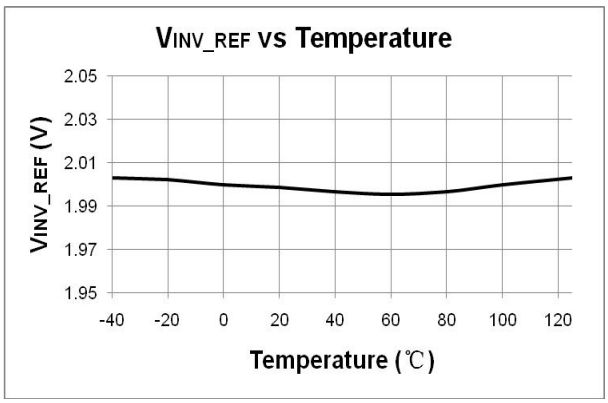
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			2	20	uA
I_{VDD_Op}	Operation Current	V_{INV}=3V, VDD=20V		1	1.5	mA
$I_{VDD\_standby}$	Standby Current			0.5	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		15	16.3	17.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8	9	10	V
V_{DD_OVP}	VDD OVP Threshold		28	30	32	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$ = 7 mA	32.5	34.5	36.5	V
Feedback Input Section (INV Pin)						
V_{INV_REF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{INV_SLP}	Short Load Protection (SLP) Threshold			0.7		V
T_{INV_Short}	Short Load Protection (SLP) Debounce Time			10		ms
V_{INV_DEM}	Demagnetization Comparator Threshold			25		mV
T_{off_min}	Minimum OFF time			2		us
T_{off_max}	Maximum OFF time			5		ms
I_{Cable_max}	Maximum Cable Drop compensation current			63		uA
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
T_{D_OCP}	Over Current Detection and Control Delay			100		ns
Over temperature Protection						
T_{SD}	Thermal Shutdown		---	165	--	°C
T_{RC}	Thermal Recovery			135	--	°C
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
R_{dson}	Static Drain-Source On Resistance				3	Ohm

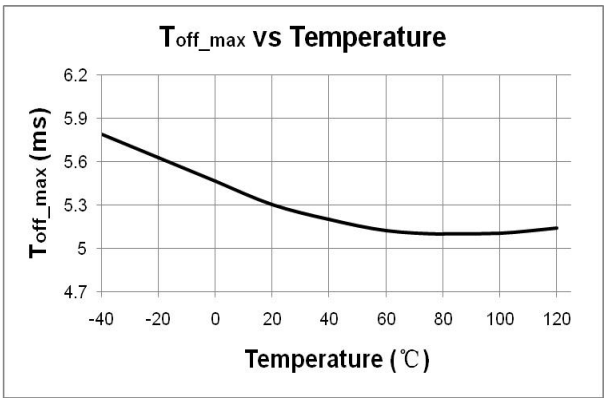
CHARACTERIZATION PLOTS

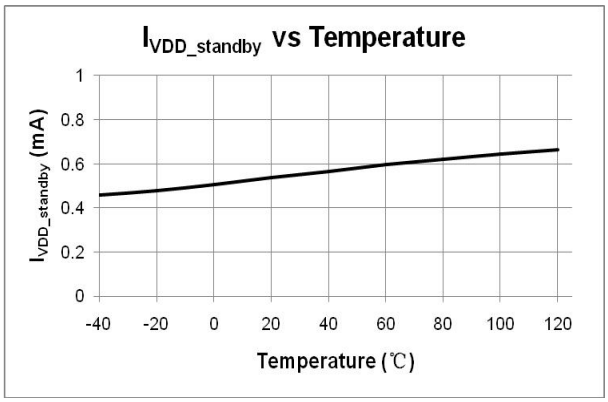












OPERATION DESCRIPTION

DP2540A is a cost effective PWM power switch optimized for off-line low power AC/DC applications including battery chargers and adapters. It operates in Primary Side Regulation (PSR), thus opto-coupler and TL431 are not required. High precision CV and CC control can be achieved to meet most small power charger and adapter applications requirements.

- **Startup Current and Start up Control**

Startup current of DP2540A is designed to be very low (typically 2uA) so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.

- **Operating Current**

The operating current of DP2540A is as low as 1mA. Good efficiency is achieved by the low operating current together with extended burst mode control schemes at No/light load conditions.

- **Primary Side CC/CV Control**

DP2540A is designed to produce good CC/CV control. In charger applications, a discharged battery charging starts in CC portion of the curve until it is nearly full charged and smoothly switched to operate in CV portion of the curve. In an AC/DC adapter, the normal operation occurs only on the CV portion of the curve. The CC portion provides output current limiting.

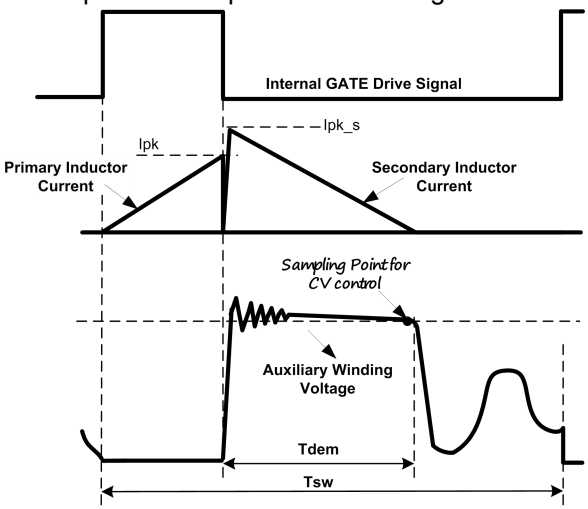


Fig.1

As shown by Fig 1, when the PWM switching is off the secondary side diode is conducted and the auxiliary winding voltage is proportion to the output voltage. Via a resistor divider connected between the auxiliary winding and INV (pin 3), the auxiliary voltage is sampled at the end of the demagnetization and it is hold until the next sampling. The sampled voltage is compared with V_{INV_REF} (2.0V) and the error is amplified by an internal Error Amplifier (EA). The internal EA output reflects the load condition and control the PWM switching frequency to regulate the output voltage, thus constant voltage (CV) can be achieved.

When system enters over load condition, the output voltage falls down and the INV sampled voltage should be lower than 2V internal reference which makes system enter CC Mode automatically.

- **Multi Mode CV Operation for High Efficiency**

DP2540A is a multi-mode PSR controller. In CV mode, the controller changes the mode of operation by sampling INV voltage. Under the medium to large load conditions, the IC operates in PWM mode, which improves the system audio noise performance. Under normal to light load conditions, the IC operates in PFM mode to achieve high efficiency. The IC can achieve less than 75mW standby power, as shown in Fig.2

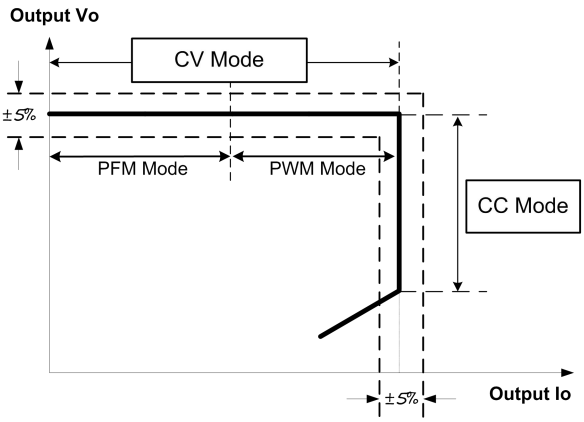


Fig.2

- **CC Operation Switching Frequency**

The switching frequency of DP2540A is adaptively controlled according to the load conditions and the operation modes.

For flyback operation in DCM, the maximum output power is given by

$$Po_{MAX} = \frac{1}{2} L_P F_{SW} I_P^2$$

Where Lp indicate the inductance of primary winding and Ip is the peak current of primary winding.

Refer to the equation above, the change of the primary winding inductance results in the change of the maximum output power and the constant output current in CC mode. To compensate the change from variations of primary winding inductance, the switching frequency is locked by and internal loop such that the switching frequency is

$$F_{SW} = \frac{1}{2T_{DEM}}$$

Since T_{DEM} is inversely proportional to the inductance, as a result, the product of Lp and Fsw is constant, thus the maximum output power and constant current in CC mode will not change as primary winding inductance changes. Up to ± 10% variation of the primary winding inductance can be compensated.

- **Adjustable CC Point and Output Power**

In DP2540A, the CC point and maximum output power can be externally adjusted by external current sense resistor Rs at CS pin as illustrated in typical application diagram. The larger Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.3.

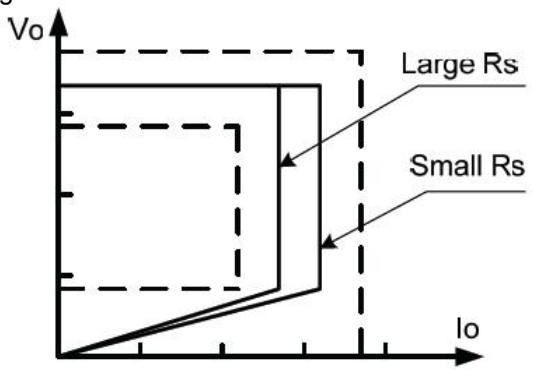


Fig.3

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in DP2540A. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

- **Audio Noise Free Operation**

DP2540A can provide audio noise free operation from full loading to zero loading.

- **Optimized Dynamic Response**

In DP2540A, an optimized dynamic response control is integrated to improve system dynamic response performance, which enables charger system to meet the USB charge requirements.

- **Programmable Cable Drop Compensation**

In DP2540A, cable drop compensation is implemented to achieve good load regulation. An offset voltage is generated at INV pin by an internal current flowing into the resistor divider. The current is proportional to the switching off time, as a result, it is inversely proportional to the output load current, thus the drop due to the cable loss can be compensated. As the load current decreases from full-load to no-load, the offset voltage at INV pin will increase. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used.

The percentage of maximum compensation is

$$\frac{\Delta V}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{INV\_REF}} \times 100\%$$

Δ V is load compensation voltage and Vout is output voltage;

For example: R1=3K Ω , R2=18K Ω , The percentage of maximum compensation is given by

$$\frac{\Delta V}{Vout} = \frac{63uA \times (3K//18K)}{2V} \times 100\% = 8.1\%$$

- **Over Temperature Protection (OTP)**

When the IC temperature is over 165 ^{O}C, the IC shuts down. Only when the IC temperature drops to 135 ^{O}C, IC will restart.

- **Output Short Load Protection**

In DP2540A, the output is sampled on INV pin and then compared with a threshold of UVP (0.7V typically) after an internal blanking time (10ms typical). When sensed INV voltage is below 0.7V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

- **VDD OVP and Zener Clamp**

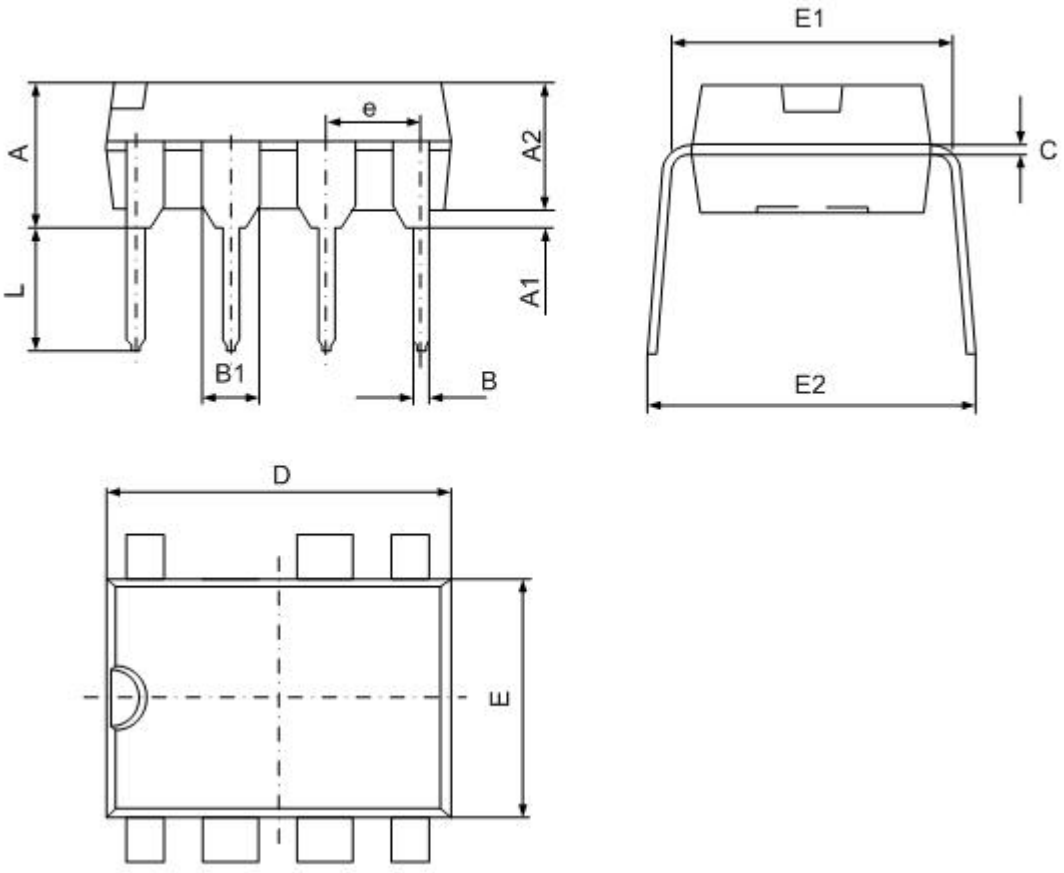
When VDD voltage is higher than 30V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 9V) and then the system will restart up again. An internal 34.5V (typical) zener clamp is integrated to prevent the IC from damage.

- **Soft Gate Drive**

DP2540A has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input.

Package Dimension

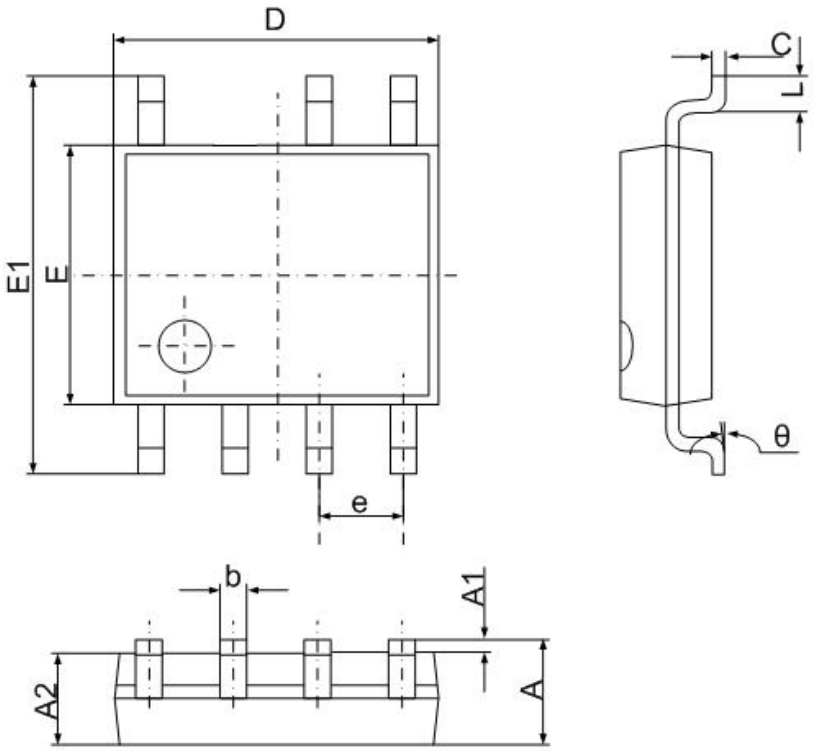
DIP7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	3.175	3.600	0.125	0.142
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	8.200	9.525	0.323	0.375

Package Dimension

SOP7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max		Min
A	1.350	1.750	A	1.350
A1	0.100	0.250	A1	0.100
A2	1.350	1.550	A2	1.350
b	0.330	0.510	b	0.330
c	0.170	0.250	c	0.170
D	4.700	5.100	D	4.700
e	1.270（BSC）	0.050（BSC）	e	1.270（BSC）
E1	5.800	6.200	E1	5.800
E	3.800		4.000	
L	0.400	1.270	L	0.400
θ	0°	8°	θ	0°