■ Description

TheDP3119 is a monolithic 36V, 2.1A step-down switch regulator. DP3119 integrates a high efficiency synchronous step-down switching regulator, which includes a 36V 108mΩ high side and a 36V, 102mΩ low side MOSFETs to provide 2.1A continuous load current over a 6.5V to 30V wide operating input voltage. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting. Programmable soft-start prevents inrush current at power-up. The supply current drops below 1μA in shutdown mode.

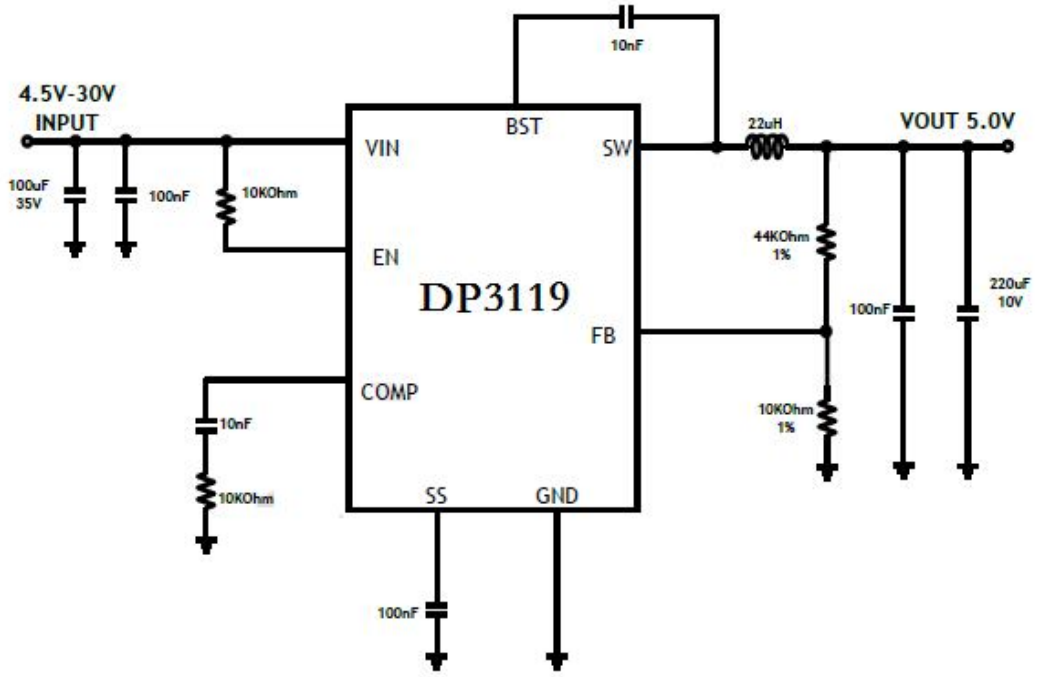
■ Applications

- USB car charger
- Portable charging device
- General purpose

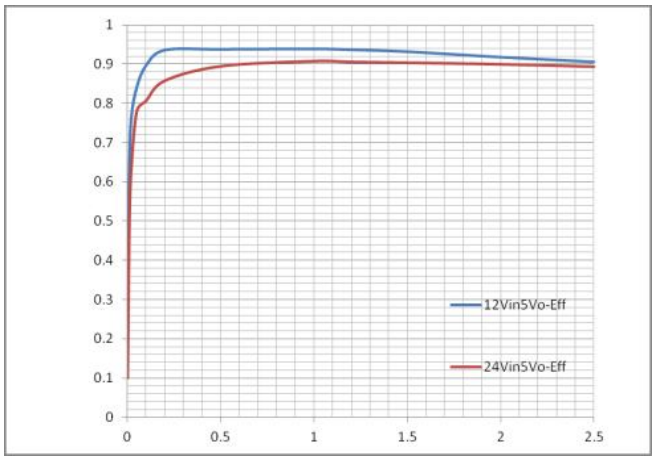
■ Features

- 2.1A continuous output current capability
- 6.5V to 36V wide operating input range with 33V input Over Voltage Protection
- Integrated 36V, 108mΩ high side and 36V, 102mΩ low side power MOSFET switches
- Up to 92% efficiency
- Programmable Soft-Start limits the inrush current at turn-on
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 100KHz Switching Frequency
- Input Under-Voltage Lockout. Output Over-Voltage Protection
- Over-Temperature Protection
- Thermally Enhanced ESOP-8 Package

■ Typical Application Schematic

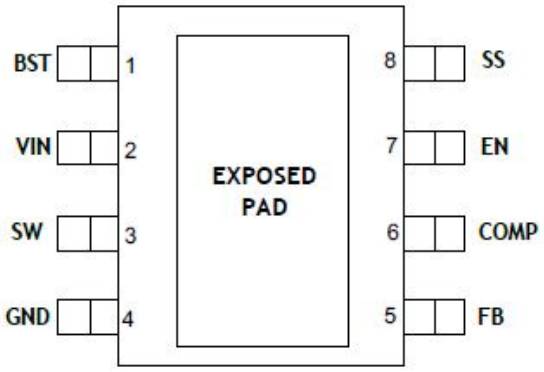


■ Efficiency



■ Pin Configuration and Functions

ESOP-8 Package (Top View)



Pin-Functions

Pin		Description
Number	Name	
1	BST	Boot-Strap pin. Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
2	VIN	Power Input. Vin supplies the power to the IC. Supply Vin with a 4.5V to 36V power source. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
3	SW	Power Switching pin. Connect this pin to the switching node of inductor.
4	GND	Ground
5	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin.
6	COMP	Connect compensation network to make the converter work stably.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN is pulled to VIN internally by a large resistor.
8	SS	Soft-start adjustment. Connect a cap to program soft-start time.
9	EPAD	EPAD is connected to GND internally. EPAD must be connected to GND on PCB board to get full power.

■ Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN to GND	-0.3	36	V
	VSS to GND	-0.3	6	V
	VEN to GND	-0.3	6	V
	VFB to GND	-0.3	6	V
Output Voltages	VCOMP to GND	-0.3	6	V
	VBST to VSW	-0.3	6	V
	VSW to GND	-1	VIN+0.3	V

■ Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	Unit
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		150	°C
T_L	Lead Temperature		260	°C
V_{ESD}	HBM Human body model		2	kV
	MM model		400	V

■ Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	6.5	30	V
	FB	-0.3	6	V
	EN	-0.3	6	V
Output Voltage	V_{OUT}	0.5	VIN*Dmax	V
Output Current	I_{OUT}	0	2.1	A
Temperature	Operating junction temperature range, T_J	-40	125	°C

■ Thermal Information (Note 3)

Symbol	Description	ESOP-8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

■ Electrical Characteristics(Typical at Vin = 12V, TJ=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	Unit
MOSFET						
I_{leak_sw}	High-Side Switch Leakage Current	V_{EN} = 0V, V_{SW} = 0V		0	10	uA
$R_{DS(ON)\_H}$	High-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 5V		108		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 5V		102		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup			6.375		V
V_{UVLO_down}				6.0		V
V_{UVLO_hys}				0.375		V
$I_{Q\text{-}NONSW}$	Operating quiescent current	VFB =1V		1		mA
$I_{Q\text{-}SW}$	Quiescent Supply Current	VFB =0.9V IOUT = 0A VOUT = 5V		1.5		mA
CONTROL LOOP						
Foscb	Buck oscillator frequency			100		kHz
V_{FB}	Feedback Voltage	4.5V ≤ VIN ≤ 30V		0.9		V
V_{FB_OVP}	Feedback Over-voltage Threshold			1		V
Dmax	Maximum Duty Cycle (Note 4)			96		%
Ton	Minimum On Time (Note 4)			100		nS
PROTECTION						
I_{ocl_hs}	Upper Switch Current Limit	Minimum Duty Cycle		4.5		A
I_{ocl_ls}	Lower Switch Current Limit	From Drain to Source		2.7		A
V_{inovp}	Input Over voltage protection			33		V
T_{ss}	Soft-Start Period			0.5		mS
Th_{sd}	Thermal Shutdown (Note 4)			155		°C
Th_{sdhys}	Thermal Shutdown Hysteresis(Note 4)			30		°C
V_{IH}	EN High Voltage		1.2			V
V_{IL}	EN Low Voltage				1	V
I_{EN}	EN Input Current			2.6		uA
I_{chg_ss}	Soft-Start Charge Current			4		uA
$V_{boot,refresh}$	Bootstrap refresh voltage			3.4		V
I_{cmp_src}	Comp Source Current	V_{FB} = 1.0 V		60		uA
I_{cmp_snk}	Comp Sink Current	V_{FB} = 0.8V		60		uA
G_{m_PS}	COMP to current sense transconuctance			5		A/V

Notes:

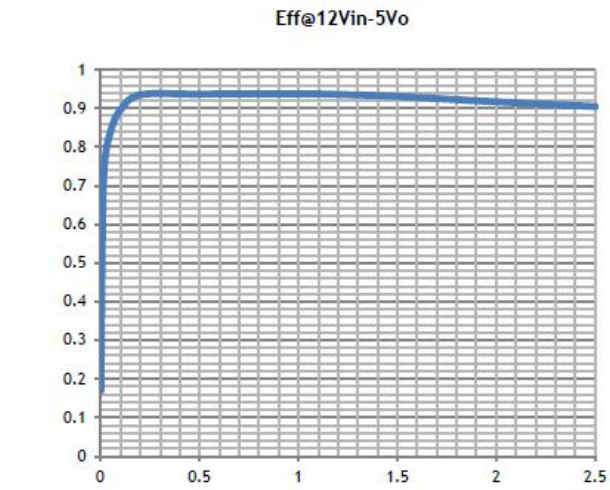
(1) Exceeding these ratings may damage the device.

(2) The device function is not guaranteed outside of the recommended operating conditions.

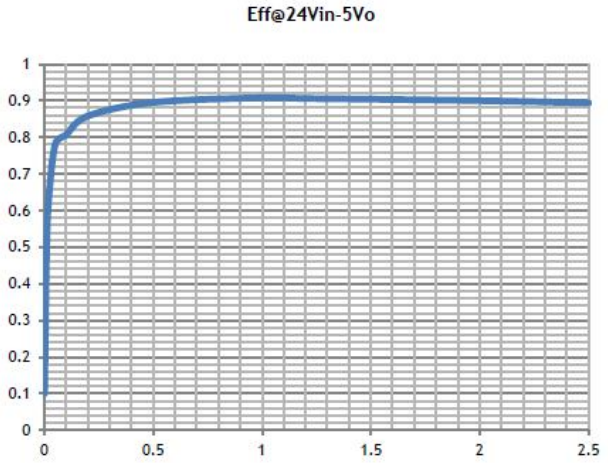
(3) Measured on approximately 1" square of 1 oz copper

(4) Guaranteed by design, not tested in production.

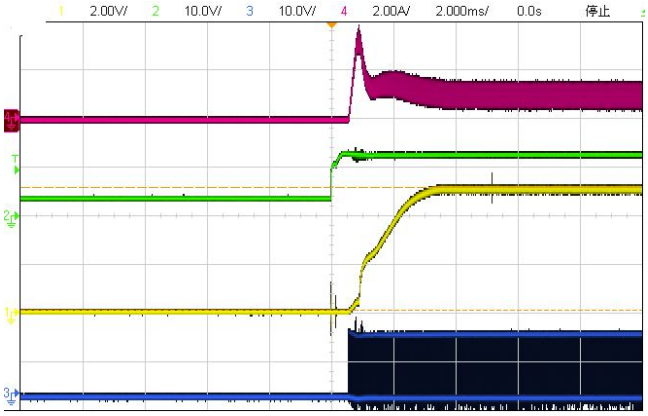
■ Typical Characteristics



Efficiency @ Vin = 12V, Vout = 5V

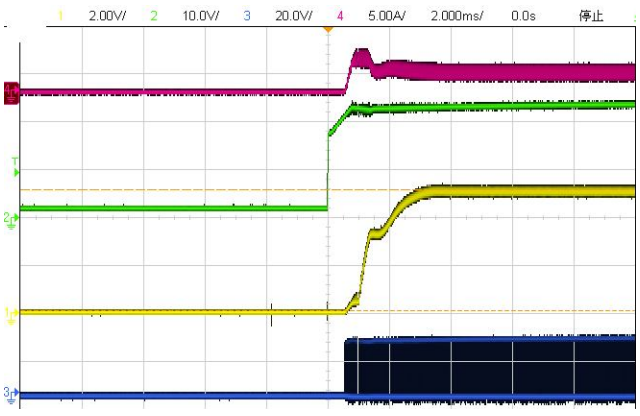


Efficiency @ Vin =24V, Vout = 5V



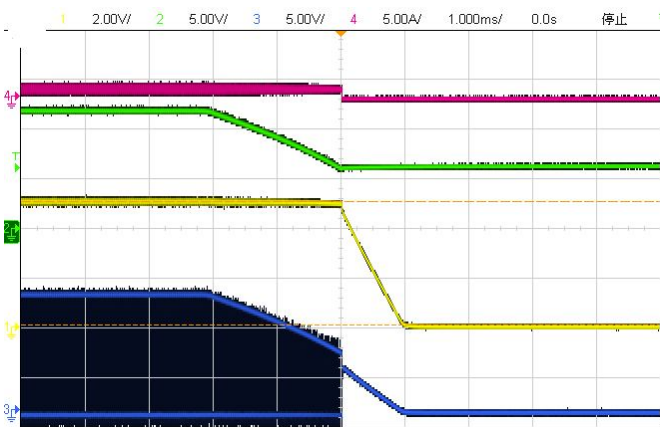
Ch1: Vout CH2: Vin CH3: SW CH4: IL

12V-5V-1A Power Up Waveform



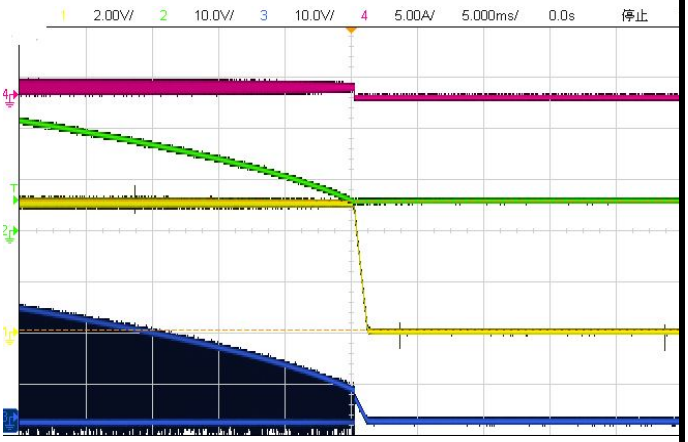
Ch1: Vout CH2: Vin CH3: SW CH4: IL

24V-5V-1A Power Up Waveform



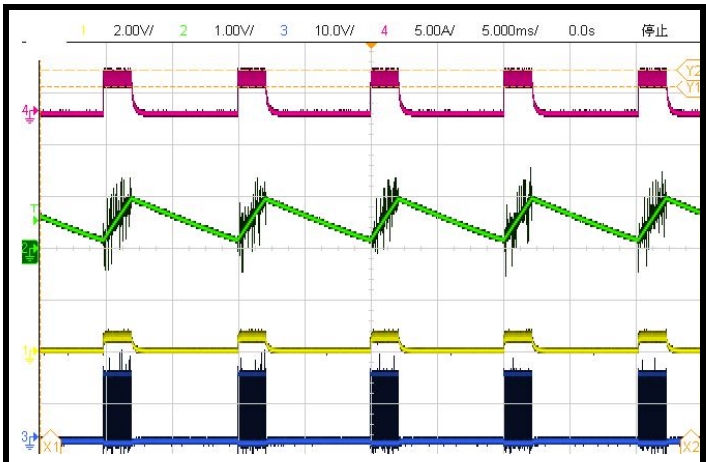
Ch1: Vout CH2: Vin CH3: SW CH4: IL

12V-5V-1A Power Down Waveform

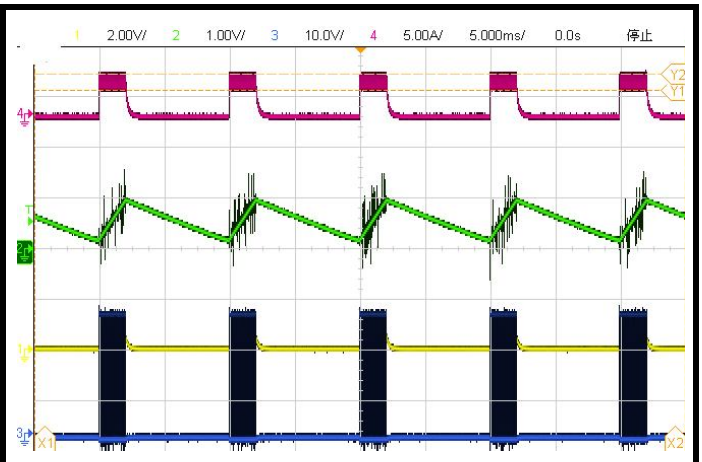


Ch1: Vout CH2: Vin CH3: SW CH4: IL

24V-5V-1A Power Up Waveform

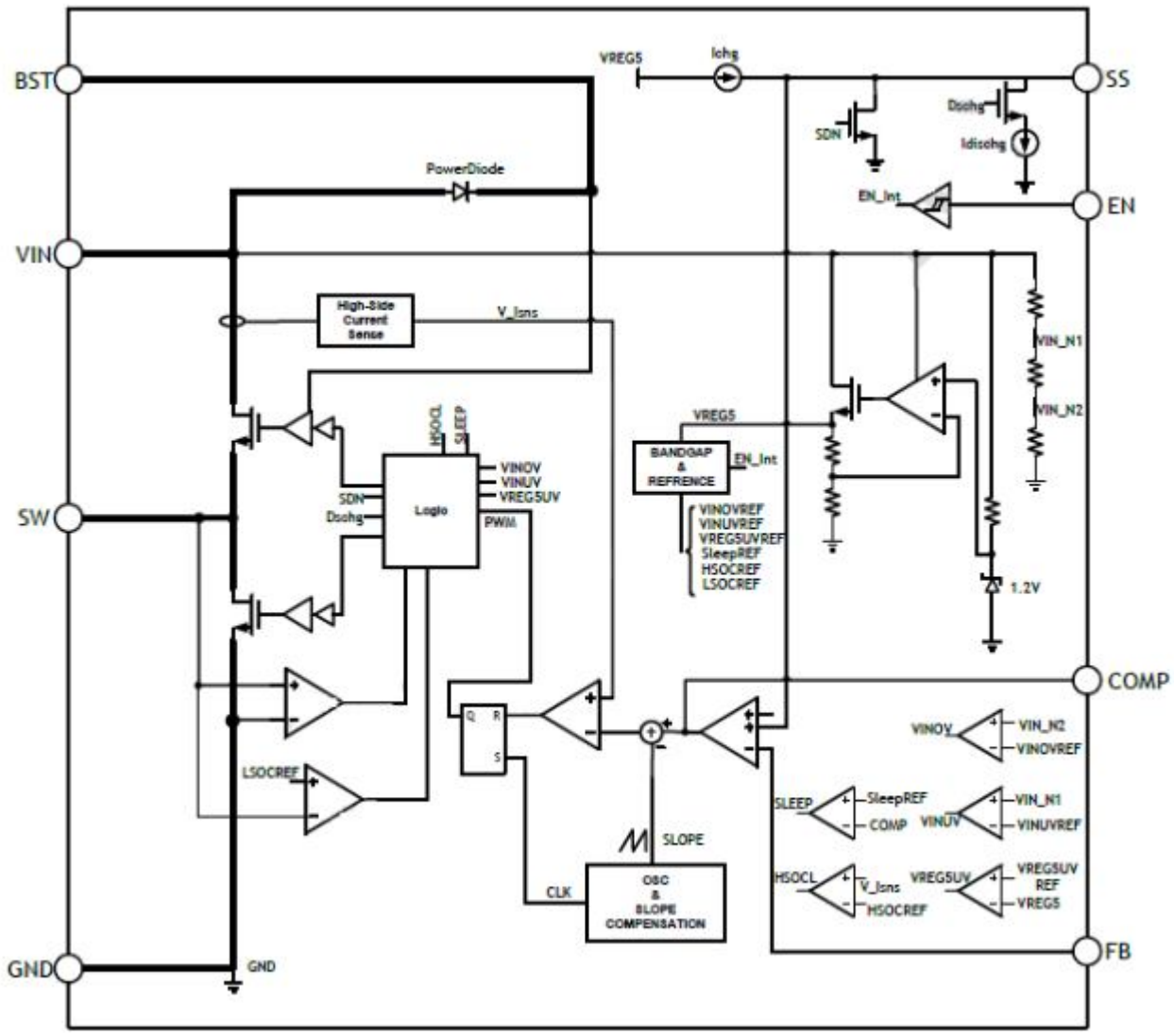


12Vin Short Protection Waveform



24Vin Short Protection Waveform

■ Functional Block Diagram



■ Overview

The DP3119 is a single channel, constant frequency, current mode step-down switching regulator for 30V, 2.1A application. It regulates 6.5V to 30V down an output voltage as low as 0.9V, and supplies up to 2.1A of load current.

The DP3119 uses current-mode control to regulate the output voltage. the output voltage is measured at FB through a resistive voltage divider and amplified through the internal error amplifier. The voltage at COMP pin is compared to the high-side switch current measured internally to control the output voltage.

The converter uses internal N-channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high-side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor is connected between SW and BST, charged by internal boost regulator during the period when low-side MOSFET is on.

When FB voltage exceeds 0.99V , the over-voltage comparator will generate a signal to shut High-side MOSFET to prevent FB voltage running away.

The DP3119 device has a fixed 100KHZ switching frequency. The device adjusts the soft-start time with the SS pin.

■ Peak Current Mode Control

The DP3119 employs a fixed 100kHz frequency, peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin to an internal error amplifier. The output of error amplifier will compare with the sensed signal of current flowing through high side switch by internal PWM comparator. PWM comparator will generate a turn-off signal to high side driver, which will turn off high side switch. The output voltage of error amplifier increases and decreases as the output current increases and decreases. The DP3119 has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

■ Sleep Operation for Light Load Efficiency

The DP3119 has an internal feature to help improve light load efficiency. when COMP voltage is less than a threshold, The DP3119 will judge and IC will go into sleep mode. Under sleep mode, typically, The peak current of high side switch will be about 400mA. when load current is smaller than this value, IC will switch in a very long period controlled by COMP voltage. With this work mode, The DP3119 will reach a very high efficiency under light load condition.

■ Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature supported by the DP3119.

■ Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. The 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation 1 below (R1 is the lower resistor, R2 is the upper resistor).

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2} \quad (1)$$

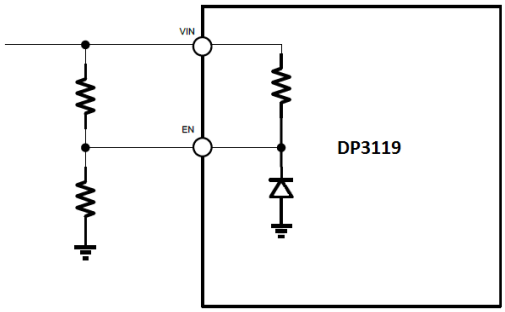
Vref is the internal reference voltage of DP3119, 0.9V.

■ Setting Enable Threshold

The DP3119 has a internal comparator to judge enable threshold at EN pin. When the EN pin voltage exceeds the threshold voltage, The DP3119 begins to work. When keeping EN low (below threshold), The DP3119 will stop working. The quiescent current of DP3119 is very low to maintain a good shut down operation for system.

The DP3119 has an internal pull up resistor to make sure IC work when EN is float. if an application requires control of EN pin, use open drain or open collector output logic to interface with this EN pin.

When system need a higher VIN UVLO threshold from the DP3119, then the EN pin can be configured as shown below:



Adjustable VIN Undervoltage Lockout

■ Error Amplifier

The DP3119 has a transconductance amplifier as the error amplifier. The error amplifier compares FB voltage with lower one between 0.9-V reference voltage and a Soft-start voltage appear at SS pin. The transconductance of the error amplifier is 600 uA/V. the frequency compensation components are placed between the COMP pin and ground.

■ Slope Compensation

The DP3119 adds a slope compensation ramp to the signal of COMP pin. this slope compensation will make sure IC not go into subharmonic oscillations as duty cycle increases.

■ Bootstrap Voltage provided by internal LDO

The DP3119 has an internal LDO to provide energy consumed by high side switch. At BST pin, The DP3119 needs a small ceramic capacitor like 100nF between BST and SW pin to provide gate-drive voltage for high side switch. The bootstrap capacitor is charged when high side is off. When IC works under CCM mode, the bootstrap capacitor will be charged when low side is on. The bootstrap capacitor will be maintained at about 5.3V. When IC works under sleep mode, what value the bootstrap capacitor is charged depends on the difference of Vin and output voltage. However, when the voltage on the bootstrap capacitor is below bootstrap voltage refresh threshold, The DP3119 will force low side on to charge bootstrap capacitor. Connecting an external diode from the output of regulator to the BST pin will also work and increase the efficiency of the regulator when output is high enough.

■ Soft-Start and Hiccup

The DP3119 needs a capacitor at SS pin to support soft-start function. system can adjust soft-start time by setting difference soft-start capacitor at SS pin. Inside DP3119, there is one 4uA current to charge SS pin when IC starts to work.

The DP3119 also uses SS pin to configure its hiccup rest time. when the output voltage is lower than 0.4V and high side peak current reaches current limit threshold, the DP3119 will stop working and discharge SS capacitor in an internal 1uA current.

When the voltage at SS pin is lower than 0.1V, IC will starts to work again and charge SS capacitor till SS voltage reaches 1.2V. if still, the output voltage is lower than 0.4V and high side peak current reaches current limit threshold, the DP3119 will stop working and discharge SS capacitor again.

■ High Side Over-Current Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the voltage of COMP and the voltage generated by high side current are compared. When the voltage generated by high side current reaches COMP voltage, high-side turns off.

■ Low Side Over-Current Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the SW voltage is sensed to generate a internal signal to compare with GND voltage. when GND voltage is larger than this internal signal, it means low side current limit reached. As long as inductor current is larger than low side current limit, high side switch won't be turned on.

The DP3119 provides zero current detection too. When the source current of low side switch reaches zero, low side switch will be immediately turned off.

■ Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 125°C typically, IC will starts to work again.

■ Inductor selection

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher DC resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{L\_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where Iload is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Optional schottky diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.

Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2} \quad (5)$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Where C_{IN} is the input capacitance value.

Output capacitors selection

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

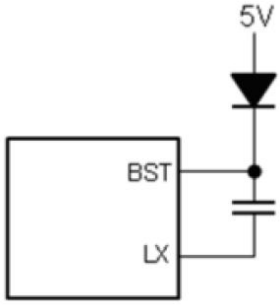
In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP3119 can be optimized for a wide range of capacitance and ESR values.

External bootstrap diode

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.



External Boostrap Diode

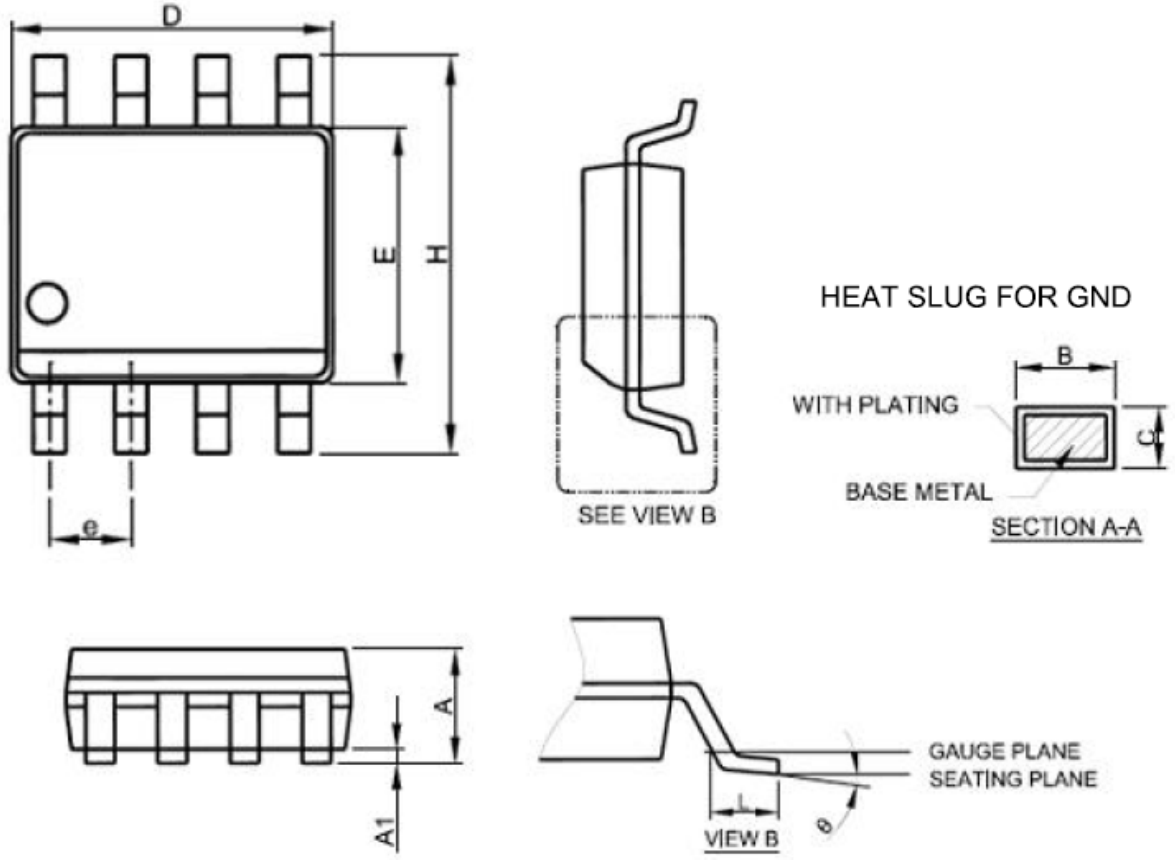
This diode is also recommended for high duty cycle operation (when (V_{OUT} / V_{IN}) > 65%) and high output voltage (V_{OUT}>12V) applications.

PCB Layout

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sense path should stay away from noisy nodes, such as SW and BST signals and preferably through a layer on the other side of shielding layer.
2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for C_1, C_2 and C_3, C_4 should be as small as possible and connect to system ground plane at only one spot (preferably at the C_{OUT} ground point) to minimize injecting noise into system ground plane.
6. Place current sense resister R3 as near as possible to the chip and stay away from noisy nodes such as SW, BST.

■ **Packaging Information** **ESOP-8**



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.17	0.25
D	4.70	5.10
E	3.70	4.10
e	1.27BSC	
H	5.80	6.20
L	0.40	1.27
θ	0	8°

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