DP3119B

36V, 3.1A Monolithic Buck Converter with CC/CV Control

Rev1.0

■ Description

DP3119B integrates a high efficiency synchronous step-down switching regulator, which includes a 36V, 76mΩ high side and a 36V, 52mΩ low side MOSFETs to provide 3.1A continuous load current over 6.5V to 36V wide operating input voltage with 33V input over voltage protection. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting.

DP3119B has configurable line drop compensation, configurable charging current limit. CC/CV mode control provides a smooth transition between constant current charging and constant voltage charging stages. Built-in soft-start prevents inrush current at power-up.

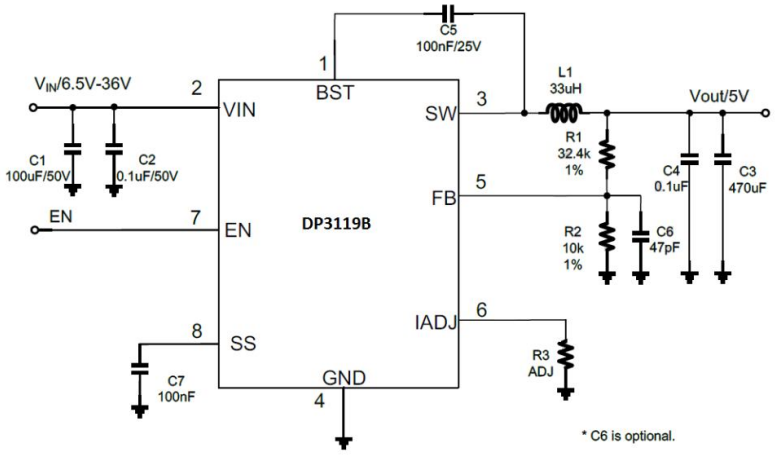
■ Applications

- USB car charger
- Portable charging device
- General purpose USB charger
- General purpose DC-DC conversion

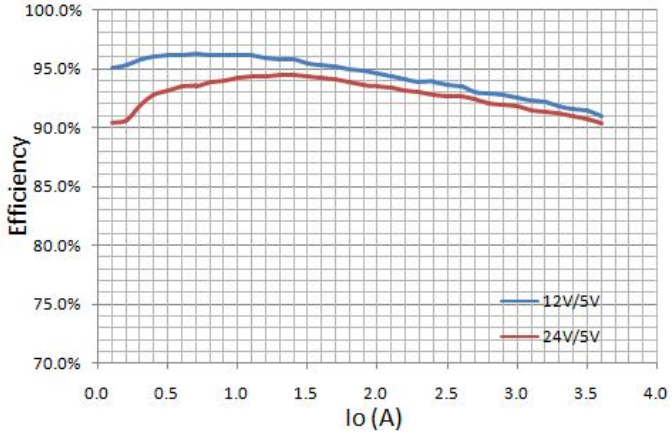
■ Features

- 3.1A continuous output current capability
- 6.5V to 36V wide operating input range with input Over Voltage Protection
- Integrated 36V, 76mΩ high side and 36V, 52mΩ low side power MOSFET switches
- Up to 95% efficiency
- CV/CC Mode control (Constant voltage and constant current). Cycle-by-Cycle Current Limiting
- Configurable Line Drop Compensation with resistor
- Internal Soft-Start limits the inrush current at turn-on
- Internal compensation to save external components
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 100KHz Switching Frequency
- Over-Temperature Protection
- 33V input voltage protection to protect power MOSFETs from working at high current ,high input voltage condition
- Soft start time is programmable using external capacitor
- Input Under-Voltage Lockout. Output Over-Voltage Protection
- Over-Temperature Protection
- Pulse skip mode at light load to improve light load efficiency
- Thermally Enhanced ESOP-8 Package

■ Typical Application Schematic

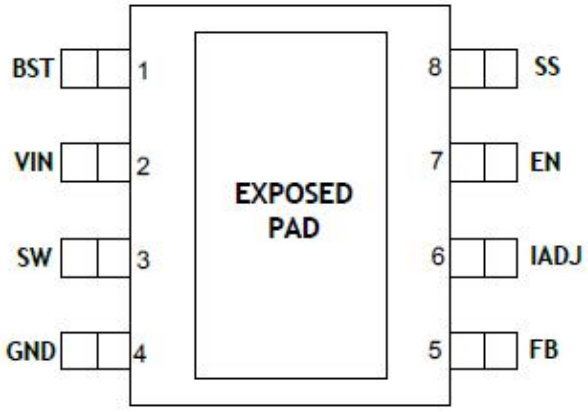


■ Efficiency



■ Pin Configuration and Functions

ESOP-8 Package (Top View)



Pin		Description
Number	Name	
1	BST	Boot-Strap pin. Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
2	VIN	Power Input. Vin supplies the power to the IC. Supply Vin with a 4.5V to 36V power source. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
3	SW	Power Switching pin. Connect this pin to the switching node of inductor.
4	GND	Ground
5	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin. It is better to connect a 47pF ceramic capacitor between FB pin and GND pin.
6	IADJ	Connect a resistor between IADJ and GND to configure load current limit and line drop compensation.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN is pulled to VIN internally by a large resistor.
8	SS	This pin is used to program soft-start time, connect a cap to program soft-start time.
9	EPAD	EPAD is connected to GND internally. EPAD must be connected to GND on PCB board to get full power.

■ Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	36	V
	V_{SS} to GND	-0.3	6	V
	V_{EN} to GND	-0.3	6	V
	V_{FB} to GND	-0.3	6	V
Output Voltages	VI_{ADJ} to GND	-0.3	6	V
	V_{BST} to VSW	-0.3	6	V
	V_{SW} to GND	-1	VIN+0.3	V

■ Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	Unit
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		150	°C
T_L	Lead Temperature		260	°C
V_{ESD}	HBM Human body model		2	kV
	MM model		500	V

■ Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	6.5	30	V
	FB	-0.3	6	V
	EN	-0.3	6	V
Output Voltage	V_{OUT}	0.5	VIN*Dmax	V
Output Current	I_{OUT}	0	3.1	A
Temperature	Operating junction temperature range, T_J	-40	125	°C

■ Thermal Information (Note 3)

Symbol	Description	ESOP-8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

■ Electrical Characteristics(Typical at Vin = 12V, TJ=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	Unit
MOSFET						
$R_{DS(ON)\_H}$	High-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} =3.3V		76		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 3.3V		52		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup				6.5	V
V_{UVLO_down}				6.0		V
V_{UVLO_hys}				0.5		V
$I_{Q\text{-}NONSW}$	Operating quiescent current	VFB =1.2V		1		mA
CONTROL LOOP						
Foscb	Buck oscillator frequency			100		kHz
V_{FB}	Feedback Voltage			1.2		V
V_{FB_OVP}	Feedback Over-voltage Threshold			1.1*VFB		V
Dmax	Maximum Duty Cycle (Note 4)			95		%
Ton	Minimum On Time (Note 4)			200		nS
PROTECTION						
I_{ocl_hs}	Upper Switch Current Limit	Minimum Duty Cycle		5.5		A
I_{ocl_ls}	Lower Switch Current Limit	From Drain to Source		4.5		A
V_{inovp}	Input Over voltage protection			33		V
Th_{sd}	Thermal Shutdown (Note 4)			155		°C
Th_{sdhys}	Thermal Shutdown Hysteresis(Note 4)			15		°C
D_{hiccup}	Hiccup duty cycle (Note 4)			10		%

Notes:

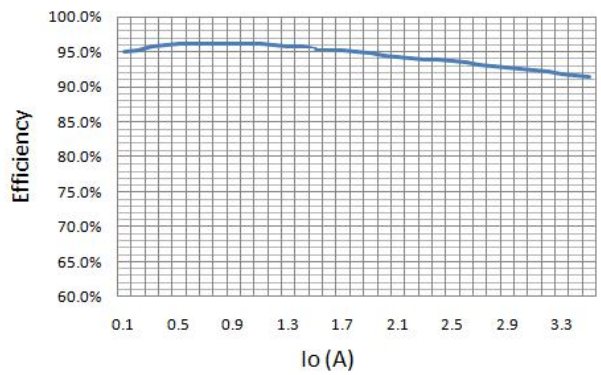
(1) Exceeding these ratings may damage the device.

(2) The device function is not guaranteed outside of the recommended operating conditions.

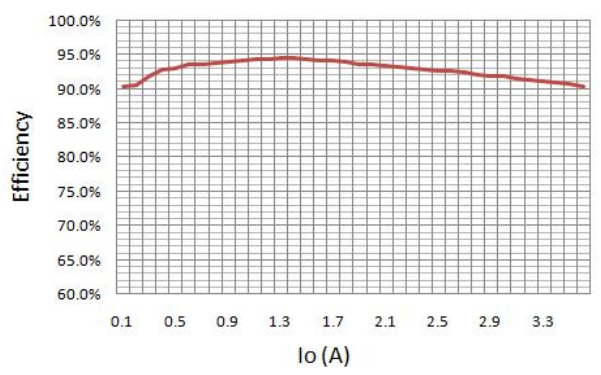
(3) Measured on approximately 1" square of 1 oz copper

(4) Guaranteed by design, not tested in production.

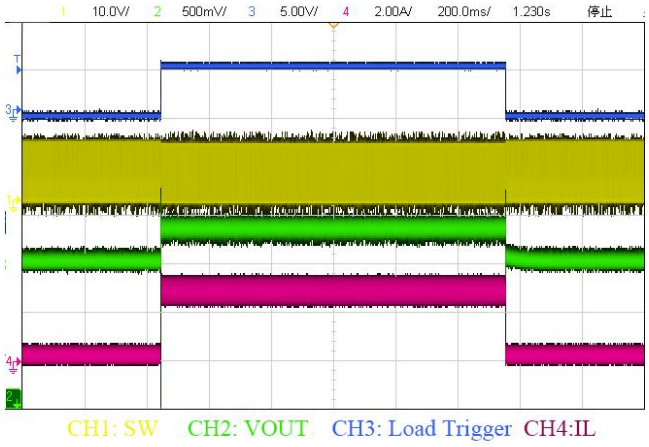
■ Typical Characteristics



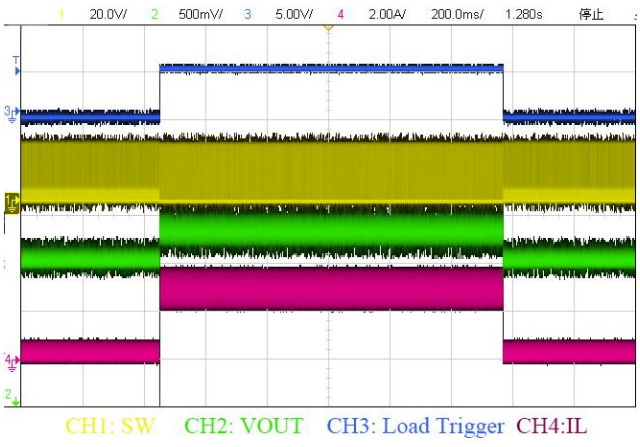
Efficiency @ Vin = 12V, Vout = 5V



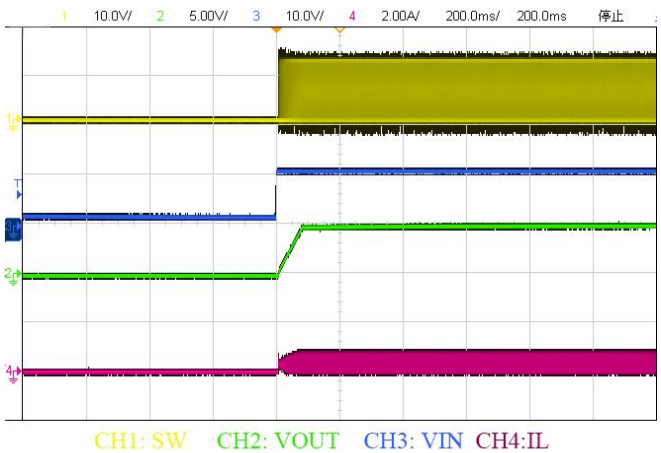
Efficiency @ Vin =24V, Vout = 5V



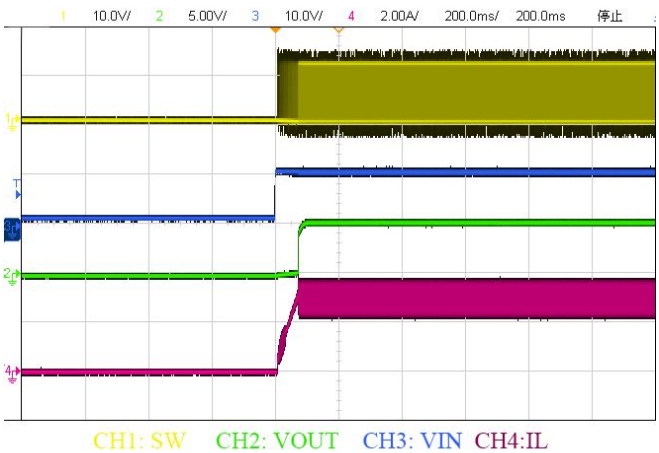
Vin = 12V, Vout = 5V
Load transient 0.3A to 3A



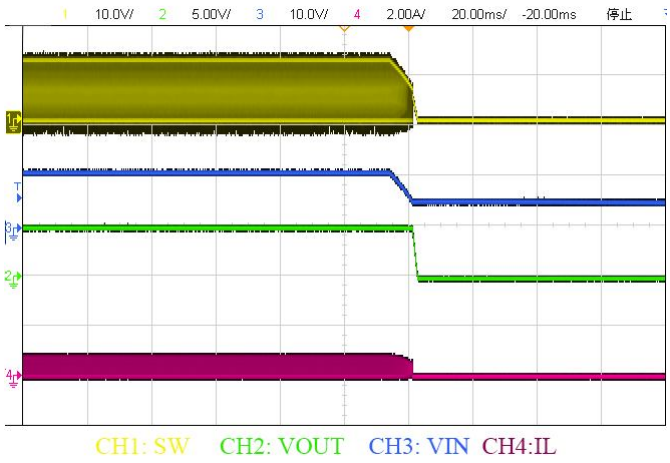
Vin = 24V, Vout = 5V
Load transient 0.3A to 3A



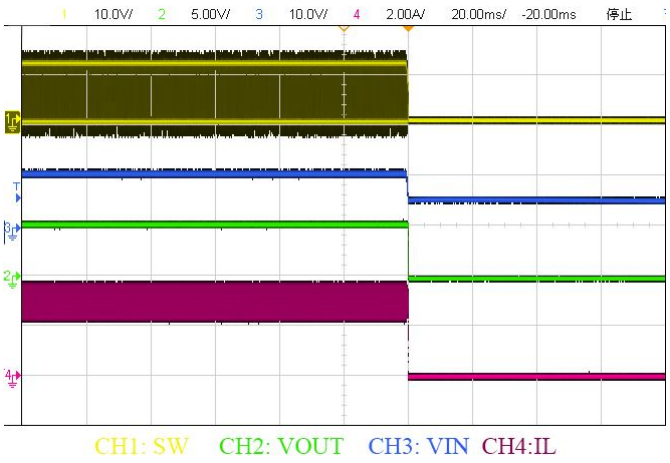
Vin = 12V, Vout = 5V
Startup waveform, Iout = 0.3A



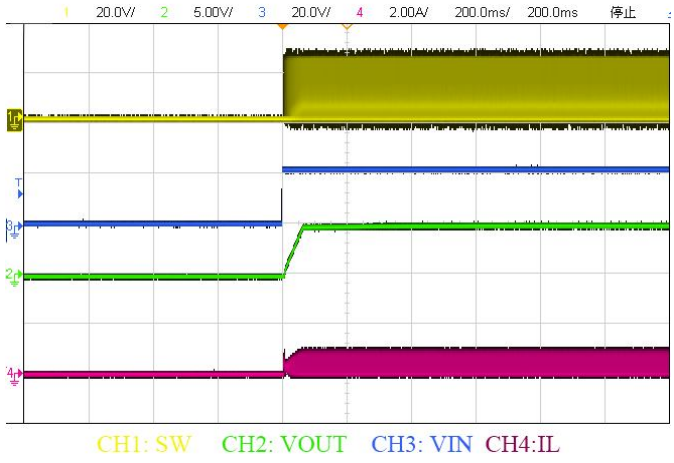
Vin = 12V, Vout = 5V
Startup waveform, Iout = 3A



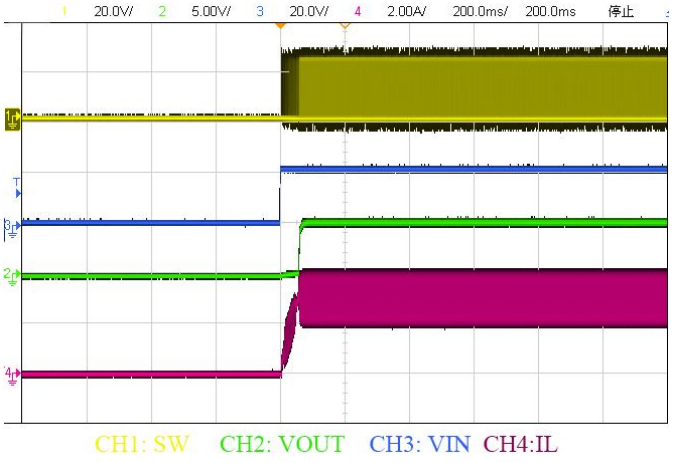
Vin = 12V, Vout = 5V
Shutdown waveform, Iout = 0.3A



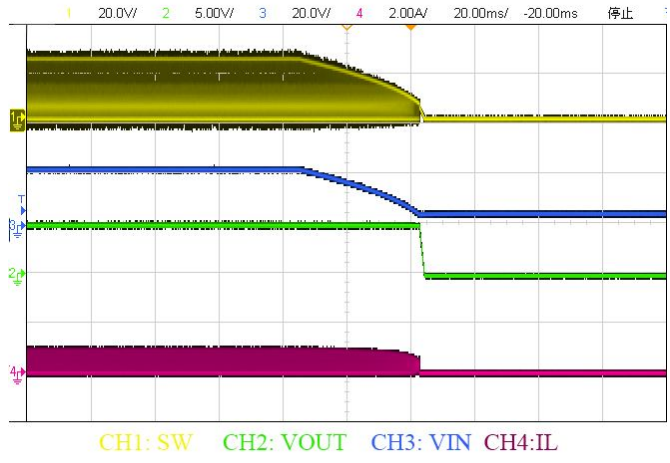
Vin = 12V, Vout = 5V
Shutdown waveform, Iout =3A



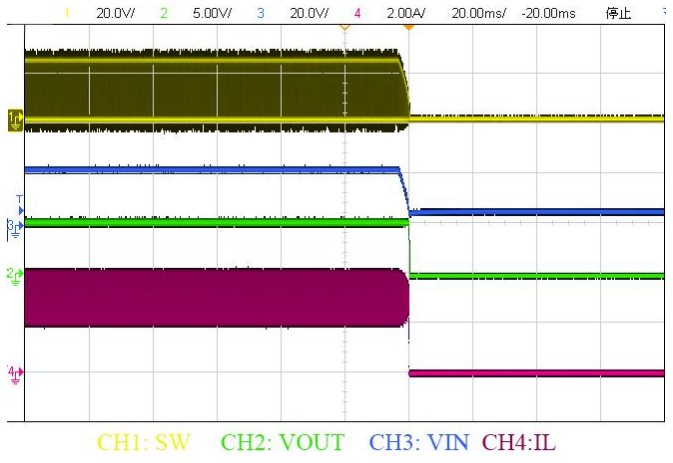
Vin = 24V, Vout = 5V
Startup waveform, Iout = 0.3A



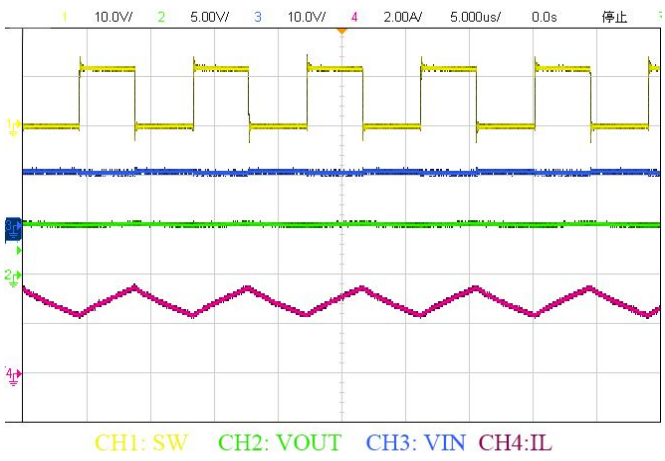
Vin = 24V, Vout = 5V
Startup waveform, Iout = 3A



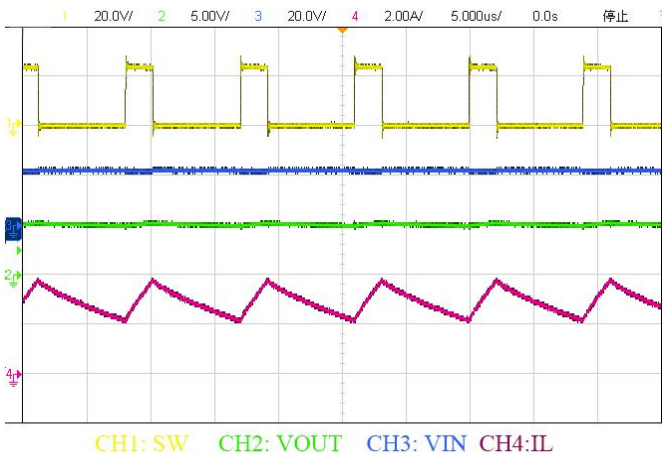
Vin = 24V, Vout = 5V
Shutdown waveform, Iout = 0.3A



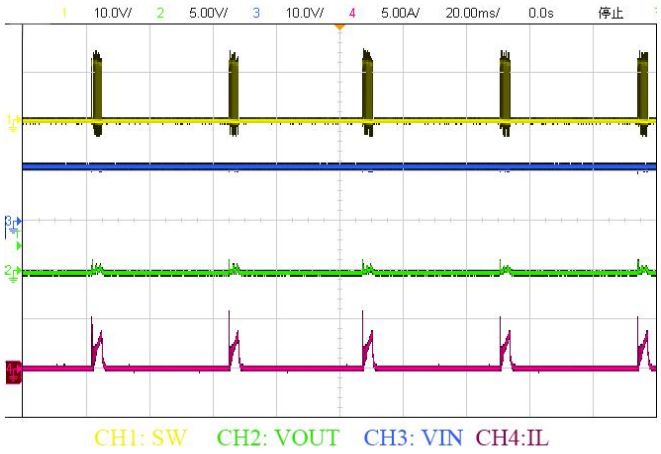
Vin = 24V, Vout = 5V
Shutdown waveform, Iout = 3A



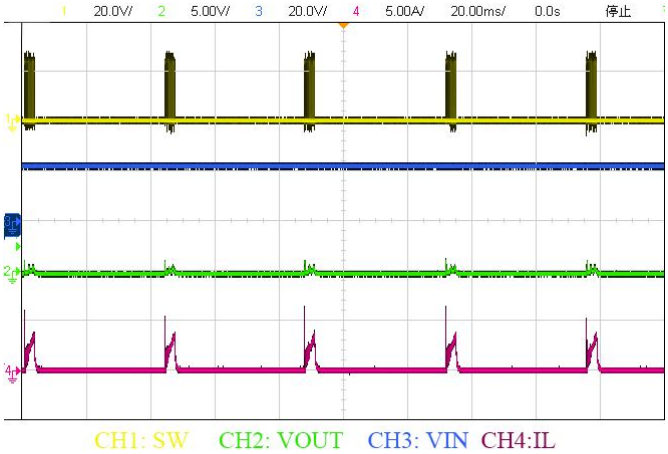
Vin = 12V, Vout = 5V
Steady State waveform, Iout = 3A



Vin = 24V, Vout = 5V
Steady State waveform, Iout = 3A

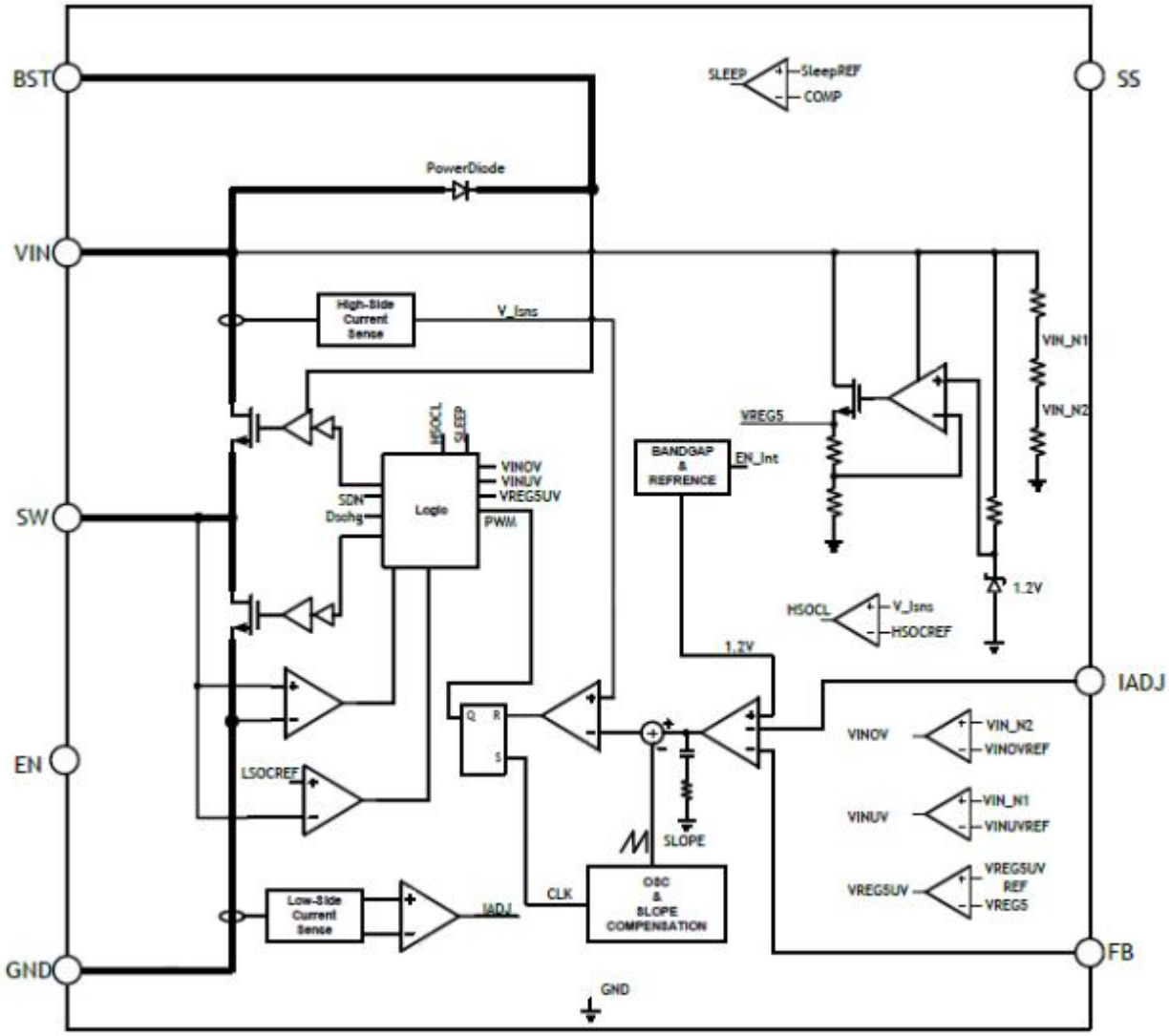


Vin = 12V, Vout = 5V
Short Circuit waveform



Vin = 24V, Vout = 5V
Short Circuit waveform

■ Functional Block Diagram



■ Overview

DP3119B is an easy to use synchronous step-down DC-DC converter that operates from 6.5V to 36V supply voltage. It is capable of delivering up to 3.1A continuous load current with high efficiency and thermal performance in a very small solution size.

DP3119B employs fixed frequency peak current mode control to regulate the output voltage. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is fixed at 100 kHz to minimize inductor size and improve EMI performance.

■ Peak Current Mode Control

DP3119B employs a fixed 100 kHz frequency peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. DP3119B has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

■ CC/CV control mode and average load current limiting

DP3119B has a CC/CV control mode. The load current is sensed and averaged. When average load current is high enough, constant-current loop will be dominant and limit the average load current to a value configured by resistor on IADJ pin. For decided average load current limit Iload, the resistor R3 can be calculated as equation (1):

$$R_3 = \frac{1.5}{\frac{I_{load}}{23.6} - 0.016} \quad k\Omega \qquad (1)$$

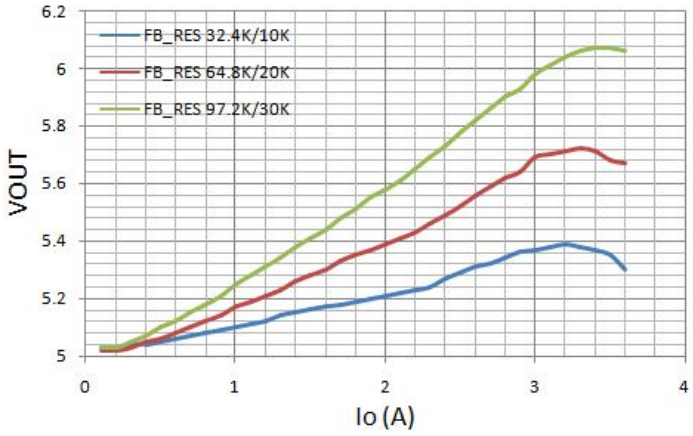
R3 is the programming resistor on IADJ pin. The typical range is 10k-50k.

■ Line drop compensation

When USB charging cable line is long and resistance is high, there will be some significant voltage drop on the cable. Portable device will see much lower input voltage. If the voltage across the load input terminals is too low, it will affect the charge time for the load. It is recommended to adjust the output voltage of charger to compensate this voltage drop. DP3119B has an excellent configurable line drop compensation feature. The line drop compensation value can be programmed by the top feedback resistor R1 in Fig 1. The value can be roughly calculated as equation (2):

$$V_{lineDrop} = \frac{I_{load} * G_{ls} * R_3 * R_1}{100k} \qquad (2)$$

Iload is the load current. Gls is the load current sense gain from load current to sourcing current on IADJ pin. R3 is the programming resistor on IADJ pin. R1 is the top output sensing resistor. For 5V/3.1A application, the values can be set as: R3=10k; R2=10k; R1=31.6k. Fig. 20 shows line drop compensation with different R1/R2 combinations.



Line drop compensation

■ Sleep Operation for light load efficiency

DP3119B has an internal feature to help improving light load efficiency. When output current is low, DP3119B will go into pulse skip mode to save power.

■ Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. The 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation (3) below. It is recommended to make R2/R1=3.16:

$$V_{out} = V_{ref} \times \frac{R_1 + R_2}{R_2} \qquad (3)$$

Vref is the internal reference voltage of DP3119B, 1.2V.

■ Error Amplifier

The error amplifier compares the FB voltage against the internal reference (Vref) and outputs a current proportional to the difference between these two signals. This output current charges or discharges the internal compensation network to generate the error amplifier output voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control-loop design.

■ Slope Compensation

In order to avoid sub-harmonic oscillation at high duty cycle, DP3119B adds a slope compensation ramp to the sensed signal of current flowing through high side switch.

■ Bootstrap Voltage provided by internal LDO

DP3119B has an internal LDO to provide energy consumed by high side switch. At BST pin, DP3119B needs a small ceramic capacitor like 100nF between BST and SW pin to provide gate-drive voltage for high side switch. The bootstrap capacitor is charged when high side is off. In Continuous-Current-Mode, the bootstrap capacitor will be charged when low side is on. The bootstrap capacitor voltage will be maintained at about 5.3V. When IC works under sleep mode, what value the bootstrap capacitor is charged depends on the difference of Vin and output voltage. However, when the voltage on the bootstrap capacitor is below bootstrap voltage refresh threshold, DP3119B will force low side on to charge bootstrap capacitor. Connecting an external diode from the output of regulator to the BST pin will also work and increase the efficiency of the regulator when output is high enough.

■ Soft-Start and Hiccup

Connect a capacitor on SS pin to program soft-start time. DP3119B has a soft-start function to control the ramp up speed of output voltage and limit the input current surge during IC start-up.

■ Over-Current Protection and Hiccup

DP3119B has cycle-by-cycle peak current limit for both high side and low side switch. When high side switch current is higher than high side current limit, high side switch will be turned off. DP3119B will not turn on high side switch again until low side switch current is lower than low side switch current limit. DP3119B has a CC/CV control structure. When load current is smaller than load current limit programmed by resistor on IADJ pin, CV (constant voltage) loop is dominant. FB voltage will be regulated to internal reference point. When load current is close to load current limit point, CC (constant current) loop will be dominant and regulate load current to be constant by lower down output voltage. If IADJ is connected to GND and output is shorted to GND, DP3119B will go into hiccup mode to limit average load current. DP3119B will exit hiccup mode once the over current condition is removed.

■ Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 140°C, IC will start to work again.

■ Enable

DP3119B can be enabled by EN pin. EN pin internal threshold is set at 1V. Customer can adjust the startup voltage at input pin by this EN pin through resistor divider.

■ Application and Implementation

■ Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{L\_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Where Iload is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

■ Optional schottky diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled with low side MOSFET to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Part Number	Voltage/Current Rating	Vendor
SS25FA	50V/2A	Fairchild
B240A	40V/2A	Vishay

■ Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2} \quad (7)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{load}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

CIN is the input capacitance.

■ Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right) \quad (9)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

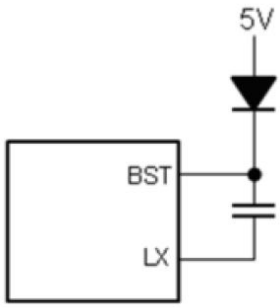
In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP3119B can be optimized for a wide range of capacitance and ESR values.

■ External bootstrap diode

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.



External Boostrap Diode

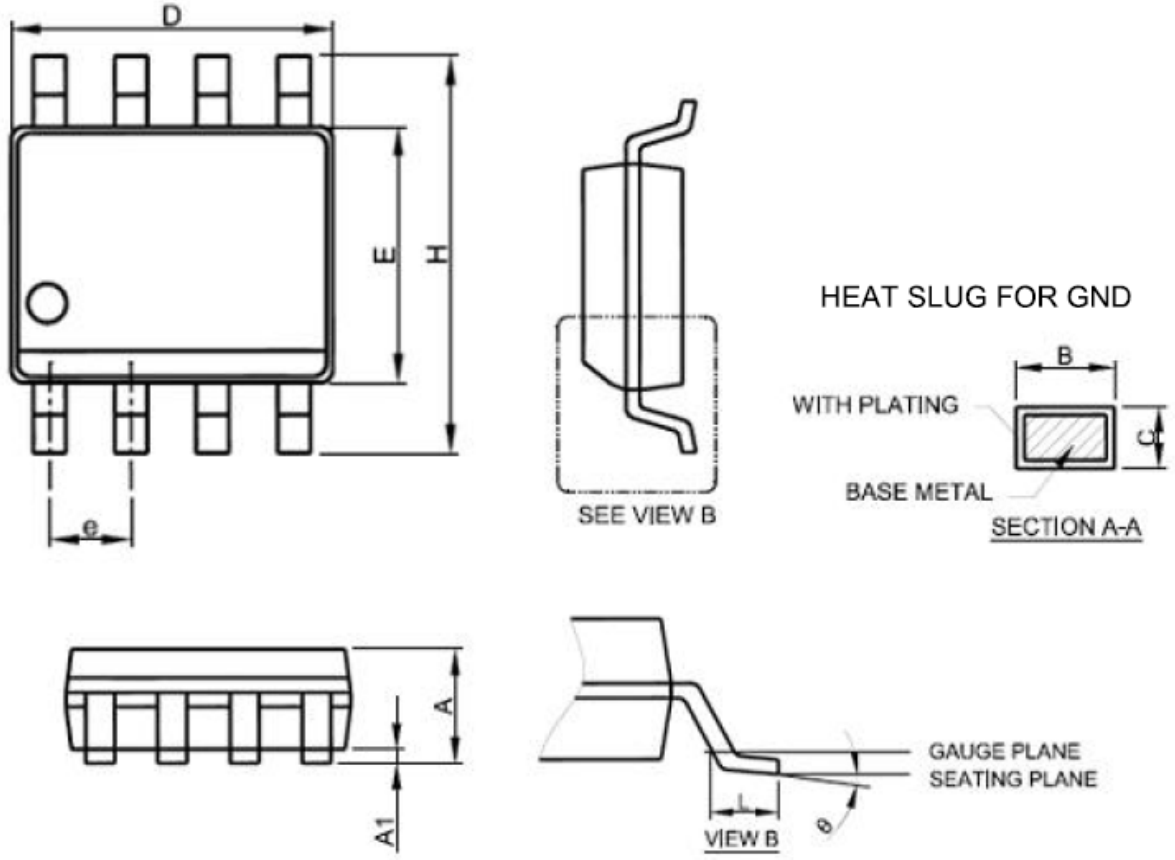
This diode is also recommended for high duty cycle operation (when (VOUT / VIN) > 65%) and high output voltage (VOUT>12V) applications.

■ PCB Layout

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sense path should stay away from noisy nodes, such as SW and BST signals and preferably through a layer on the other side of shielding layer.
2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for C_1, C_2 and C_3, C_4 should be as small as possible and connect to system ground plane at only one spot (preferably at the C_{OUT} ground point) to minimize injecting noise into system ground plane.
6. Place current sense resister R3 as near as possible to the chip and stay away from noisy nodes such as SW, BST.

■ **Packaging Information** **ESOP-8**



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.17	0.25
D	4.70	5.10
E	3.70	4.10
e	1.27BSC	
H	5.80	6.20
L	0.40	1.27
θ	0	8°

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