M-Densus High Density Memory Device

256 Megabit CMOS 3.3V EDO DRAM DP3ED32MX8RY5

DESCRIPTION:

The M-Densus series is a family of interchangeable memory modules. The 64 Megabit DRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The module is constructed with four 8 Meg x 8 EDO, 3.3 Volt DRAM's available in a 128 Megabit compatible pin-out.

The 64 Megabit based M-Densus modules have been designed to fit in the same footprint as the 32 Meg x 4 DRAM TSOP monolithic. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

Configurations Available:

256 Megabit: 32 Meg x 8

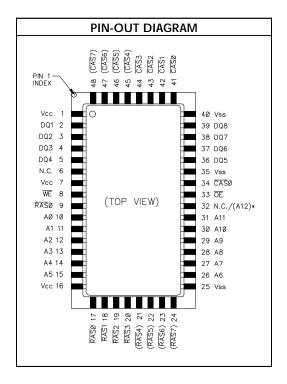
Access Times: 50, 60ns (max.)

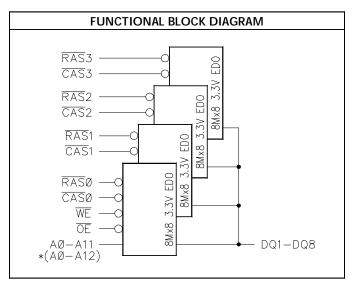
• 3.3 Volt Supply

- Common Data Inputs and Outputs
- Extended Data Out Capability (EDO)
- 4K/8K 64ms Refresh
- 3 Variations of Refresh:
 - RAS only Refresh
 - CAS before RAS Refresh
 - Hidden Refresh
- Package: Leadless TSOP Module

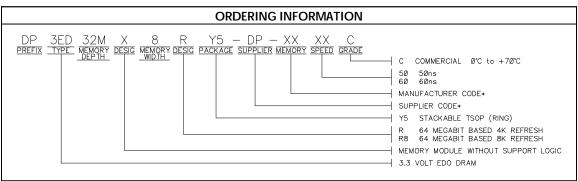
| PIN NAMES | |
|-----------------|--|
| A0 - A11 | Row Address: A0 - A11 Column Address: A0 - A11 Refresh Address: A0 - A11 |
| A0 - A12* | Row Address: A0 - A12 Column Address: A0 - A10 Refresh Address: A0 - A12 |
| DQ0 - DQ4 | Data In / Data Out |
| CAS0 - CAS4 | Column Address Strobe |
| RAS0 - RAS4 | Row Address Enables |
| WE | Data Write Enable |
| ŌĒ | Data Output Enable |
| V _{CC} | Power Supply (+3.3V) |
| V _{SS} | Ground |
| N.C. | No Connect |

^{*} A12 for 8K refresh device.

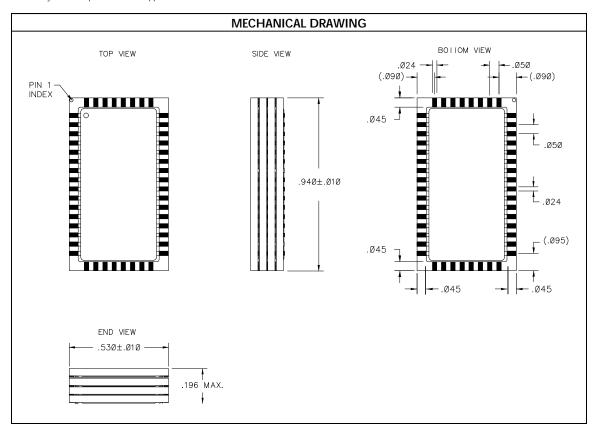




PRELIMINARY



Contact your sales representative for supplier and manufacturer codes.



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