# DP5020

CMOS 16BIT LED DRIVER CIRCUIT

## Features

DP5020 is a driver IC designed for LED display panels. It has a built-in CMOS shift register and latch function, which can convert the serial input

The DP5020 has 16 current sources that can provide a constant current of 2~60mA at each output port.

The flow rate is used to drive the LED. Each OUT driving channel output can be short-circuited to obtain a larger current output. When the environment changes, the output

The output current is affected very little. At the same time, external resistors with different resistance values (REXT) can be used to adjust the current size of each output port of DP5020.

Therefore, the brightness of the LED can be precisely controlled, which is suitable for high-quality white balance display drive modules. This product has excellent performance and reliable quality.

## Features

ÿ 16 constant current source output channelsÿ

The current output does not change with the load voltage at the outputÿ Constant current

range: 2~60mA@VDD=5V; 2~45mA@VDD=3.3Vÿ Extremely accurate current output value (channel to channel) maximum

error: ÿ±1.5ÿ (chip to chip) maximum error:

ÿ±2.0ÿÿ Precision current output value can be set by adjusting

external resistorÿ Up to 25MHz clock frequencyÿ Operating

voltage: 3.0Vÿ5.5ÿÿ Package: SSOP24, QSOP24

External Application Block Diagram

Application areas:

ÿ Indoor and outdoor, single, double, full-color (dynamic, static) LED display screens ÿ Lighting, energy-

saving lighting

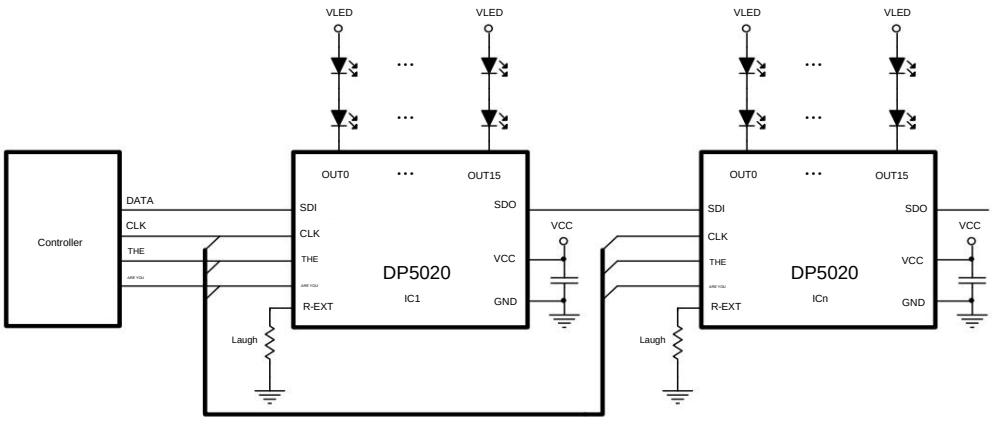



Figure 1

Internal structure diagram

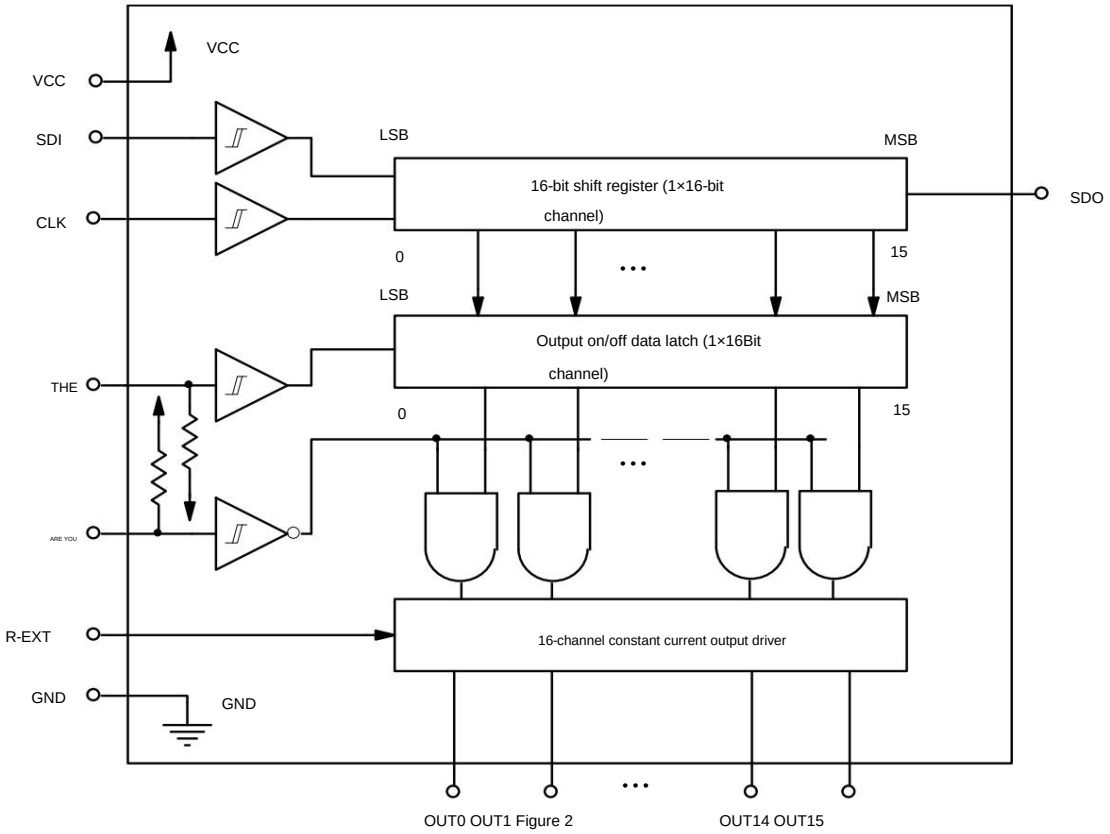
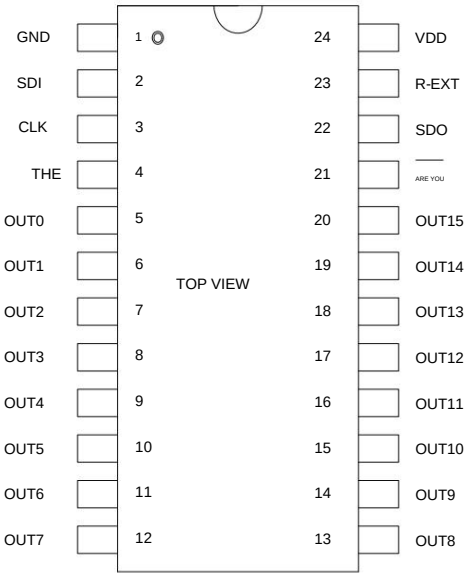



Figure 2

Pin information




DP5020

Figure 3

## Pin Function

| Pin Name | Pin Number | I/O | Functional Description |
|---|---|---|---|
| SDI | 2 | I | Serial data input, Schmitt buffer input |
| CLK | 3 | I | Serial data shift clock input, Schmitt buffer input, shift data when the clock rises |
| THE | 4 | | Data latch control terminal, Schmitt buffer input, when LE is high, serial data will be transmitted to Input latch; when LE is low, the data will be latched Output enable control |
| ARE YOU | 21 | | terminal, when OE is low, OUT0~OUT15 output will be started; when OE is high, OUT0~OUT15 output will be turned off, this pin has a pull-up resistor to VCC |
| R-EXT | 23 | I/O | Constant current value setting terminal; set the current of OUT0~OUT15 output terminals, connect an external resistor to GND |
| SDO | 22 | O | Serial data output terminal, output on the rising edge of CLK, can be connected to the SDI port of the next chip O Constant current |
| OUT0 | 5 | | source output terminal. Each output terminal can be short-circuited to increase the constant current |
| OUT1 | 6 | O | Constant current source output |
| OUT2 | 7 | O | Constant current source output |
| OUT3 | 8 | O | Constant current source output |
| OUT4 | 9 | O | Constant current source output |
| OUT5 | 10 | O | Constant current source output |
| OUT6 | 11 | O | Constant current source output |
| OUT7 | 12 | O | Constant current source output |
| OUT8 | 13 | O | Constant current source output |
| OUT9 | 14 | O | Constant current source output |
| OUT10 | 15 | O | Constant current source output |
| OUT11 | 16 | O | Constant current source output |
| OUT12 | 17 | O | Constant current source output |
| OUT13 | 18 | O | Constant current source output |
| OUT14 | 19 | O | Constant current source output |
| OUT15 | 20 | O | Constant current source output |
| VCC | 24 | | termina - Chip power |
| GND | 1 | | supply - Control logic and drive current loop ground |

## Output and input equivalent circuit

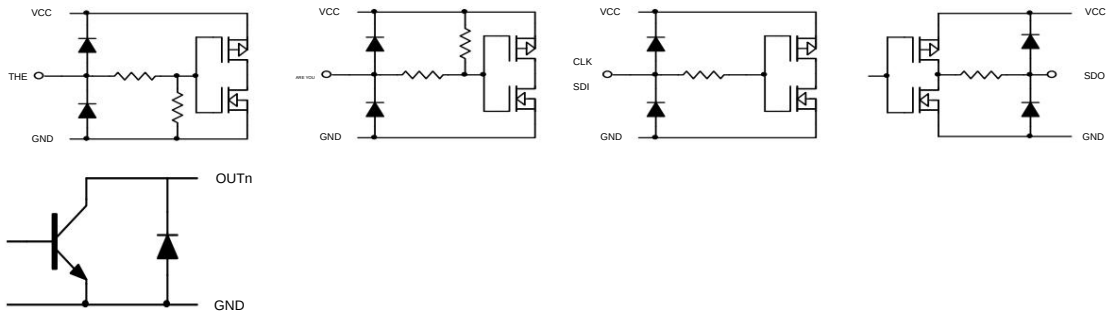



Figure 4

Integrated circuits are electrostatically sensitive devices. When used in dry seasons or dry environments, they are prone to generate a large amount of static electricity. Static electricity discharge may

It is recommended to take all appropriate precautions to prevent the IC from being damaged.

If the chip is not properly connected, it may cause ESD damage or performance degradation, and the chip may not work properly.

Logic diagram

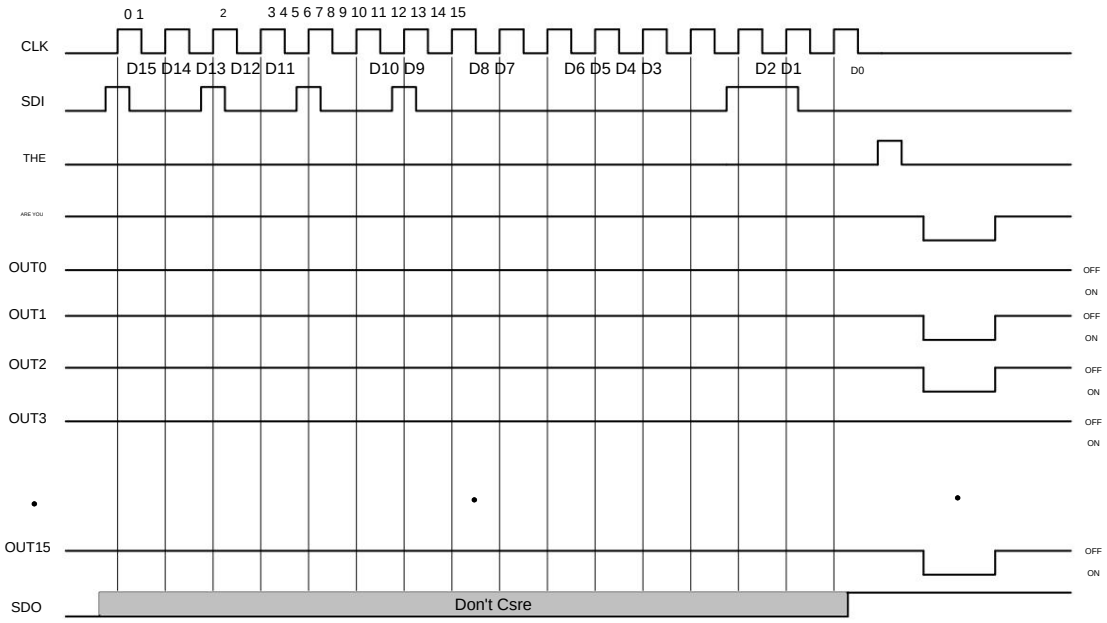



Figure 5

Limit parameters (1) (2)

| Parameter name | | Parameter Symbols | Limit value unit | |
|---|---|---|---|---|
| Supply | | VCC | -0.4ÿ6.0 | V |
| voltage Input voltage | SDI,CLK,LE,OE | COME | -0.4ÿVCC+0.4V | V |
| range Output current | OUT0~OUT15 | IOUT | 65 | mA |
| (DC) Output voltage | OUT0~OUT15,SDO | VOUT | -0.4ÿ+6.0 | V |
| range Clock | CLK, SDI, LE, OE | FCLK | 25 | MHZ |
| frequency Operating temperature range | | Torp | -20ÿ+85 | ÿ |
| Storage temperature | | Ttsg | -55ÿ+150 | ÿ |
| range Human body model | | ESD | 4000 | V |
| (HBM) Machine model (MM) | | | 300 | V |

(1) The levels in the above table may cause permanent damage to the device and reduce the reliability of the device under long-term use conditions.

It is not recommended that the chip operate beyond these limit parameters under any other

conditions. (2) All voltage values are tested relative to the network ground.

Recommended operating conditions

| Tested at -45ÿ~+85ÿ unless otherwise specified | | | DP5020 | | | unit |
|---|---|---|---|---|---|---|
| Parameter Symbol | Parameter Symbol | Test Conditions DC | Minimum | Typical | Maximum | |
| Parameter Specifications: VCC=3V~5.5V | | | | | | |
| Power supply voltage VCC | | | 3 | 5.0 | 5.5 | V |
| Output voltage range VO High | | OUT0~OUT15 | | | 5.5 | V |
| level input voltage VIH Low | | | 0.7×VCC | | VCC | V |
| level input voltage VIL High | | | GND | | 0.3×VCC V | |
| level output current IOH Low | | VCC=5V,SDO=4.5V | | | -8 | mA |
| level output current IOL | | VCC=5V,SDO=0.5V | | | 16 | mA |
| Constant output sink current IOLC | | OUT0~OUT15 3VÿVCCÿ3.6V | 2 | | 45 | mA |
| | | OUT0~OUT15 3.6VÿVCCÿ5.5V | 2 | | 60 | mA |
| Operating temperature range TA | | | -20 | | +85 ÿ | |
| Operating junction temperature range | | | -40 | | +125 ÿ | |
| TJ AC parameter specification table: VCC = 3V ~ | | | | | | |
| 5.5V Data shift clock frequency Rate | FCLK | CLK | | | 25 | MHZ |
| Pulse duration | TWH0 | CLK | 15 | | | ns |
| | TWH1 | THE | 25 | | | ns |
| | TWH2 | ARE YOU | 60 | | | ns |
| | TWL2 | ARE YOU | 30 | | | ns |
| Time Establishment | TSU0 | SDI – CLKÿ | 5 | | | ns |
| | TSU1 | LEÿ– CLKÿ | 12 | | | ns |
| Time keeping | TH0 | SDI – CLKÿ | 5 | | | ns |
| | TH1 | LEÿ– CLKÿ | 12 | | | ns |

Electrical Characteristics

| Tested under VDD=3.0V~5.5V and operating temperature -40ÿ~+85ÿ, Unless otherwise | | | DP5020 | | | unit |
|---|---|---|---|---|---|---|
| specified, parameter name | parameter symbol | Test conditions | Minimum | Typical | Maximum | |
| High level output voltage | VOH | IOH=-6mA: SDO | VCC-0.4 | VCC | V | |
| Low level output voltage | VOL | IOL=10mAÿSDO | | | 0.4 | V |
| Input Current | IIN | VIN=connect to VCC or GND SDI,CLK,LE,OE | -1 | | 1 | uA |
| Supply Current ÿVCCÿ | ICC0 | SDI/CLK/LE=0,OE=1 ,Riref=open SDI/ | | 11 | 12 mA | |
| | ICC1 | CLK/LE=0,OE=1 ,Riref=1.2K | | 12 | 13 mA | |
| | I CC2 | OUT0~OUT15 On, SDI, CLK, LE, OE = 0, Riref = 470ÿ | | 15 | 16 mA | |
| | I CC3 | OUT0~OUT15 On, SDI, CLK, LE, OE = 0, Riref = 1.2K | | 13 | 14 mA | |
| Constant output current | IOLO | OUT0~OUT15 open, VOUTn= 1V=VOUTfix=1V, Riref=470 ÿ,VCC=5VÿTA=25ÿ | 36.3 | 37 | 37.7 mA | |
| Output leakage current | LOLKG | OUTn=OFF,VOUTn=VOUTfix=5.5 V,OE=1,Riref=1.5K, | | | 0.1 | uA |
| Constant current error (channel to channel) | ÿIOLC0 | OUT0~OUT15 open, VOUTn =1V=VOUTfix=1V,Riref=470ÿ | | ±1 | ±1.5 % | |
| Constant current error (chip to chip) | ÿIOLC1 | OUT0~OUT15 open, VOUTn= 1V=VOUTfix=1V, Riref=1.5K, VCC =3V~5VÿTA=25ÿ | | ±1.5 | ±2 % | |
| Linear adjustment | ÿIOLC2 | OUT0~OUT15 ÿ,VOUTn= 1V=VOUTfix=1V,Riref=470 ÿ,VCC=3V~5 V | | ±0.5 | ±1 | %/V |
| Load Regulation | ÿIOLC3 | OUT0~OUT15 ÿ,VOUTn= 1V~3V,VOUTfix=1V,Riref=470ÿ | | ±1 | ±3%/V | |
| Reference voltage output | VIREF | Riref=470ÿ,TA=25ÿ OE | 1.10 | 1.16 | 1.22 | V |
| Pull-up | RPUP | | 32 | 40 | 48 | kÿ |
| resistor Pull-down resistor | RPDWN | THE | 32 | 40 | 48 | kÿ |

Switching Characteristics

| Tested under VDD=3.0V~5.5V and operating temperature -40ÿ~+85ÿ, Unless otherwise specified | Parameter Name | Parameter Symbol | Test Condition TR0 SDO | DP5020 Minimum | Typical | Maximum | unit |
|---|---|---|---|---|---|---|---|
| Rise time | | | | | 50 | 100 | nS |
| | TR1 | | OUTn | | 80 | 160 | nS |
| Fall time | TF0 | | SDO | | 50 | 100 | nS |
| | TF1 | | OUTn | | 80 | 160 | nS |
| Transmission delay time | TD0 | | CLKÿ to SDOÿÿ | | 60 | 120 | nS |
| | TD1 | | LEÿ or OEÿÿ to OUT0/OUT7/OUT8 /OUT15 On/Off | | 100 | 150 | nS |
| | TD2 | | LEÿ or OEÿÿ to OUT1/OUT6/OUT9 /OUT14 On/Off | | 120 | 170 | nS |
| | TD3 | | LEÿ or OEÿÿ to OUT2/OUT5/ OUT10/OUT13 On/Off | | 140 | 190 | nS |
| | TD4 | | LEÿ or OEÿÿ to OUT3/OUT4/ OUT11/OUT12 On/Off | | 160 | 210 | nS |
| Output Error time | TON_ERR | | | -50 | | 50 | nS |

Timing characteristics

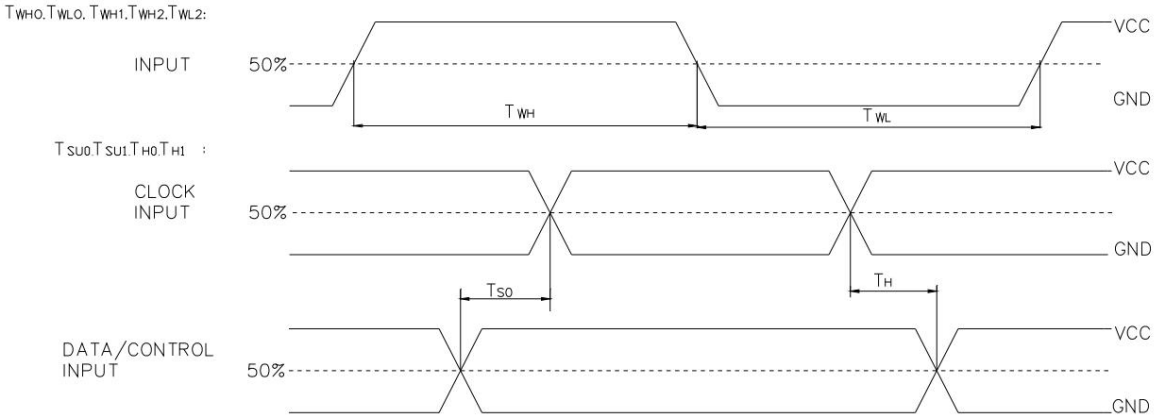



Figure 6- Input time

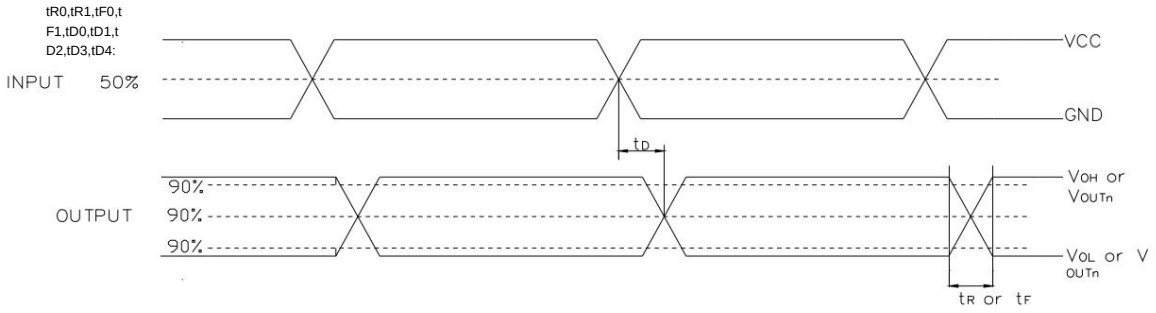



Figure 7- Output time

Application Information

As shown in the figure below, an external resistor (Rext) is used to adjust the output current (IOUT). The output current value can be calculated by applying the following formula:

$$Iout = \frac{1.16V}{Laugh} \times 15$$

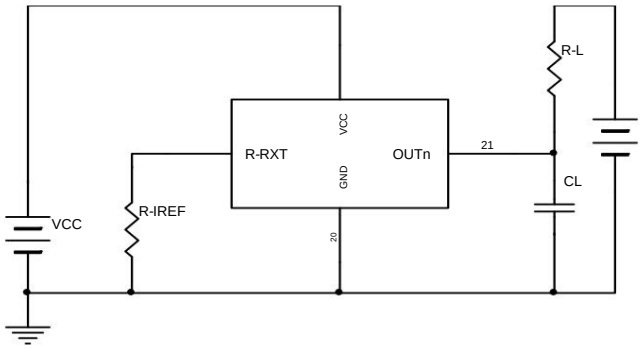



Figure 8

The Riref in the formula refers to the voltage value at the R-EXT terminal. When the resistance value is 470ÿ, the output current value can be calculated by the formula to be 37mA; when When the resistance value is 1200ÿ, the output current is 14.5mA.

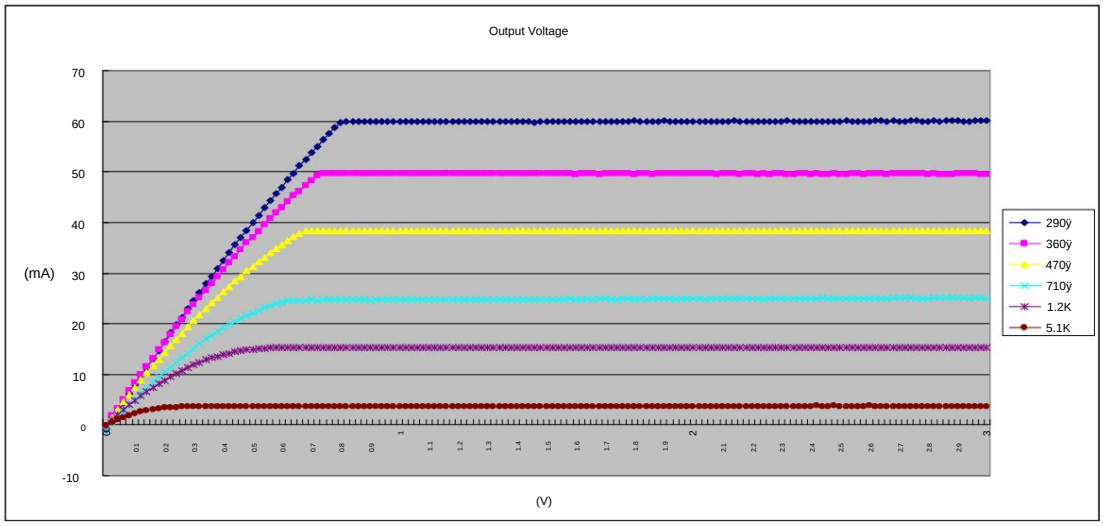



Fig. 9

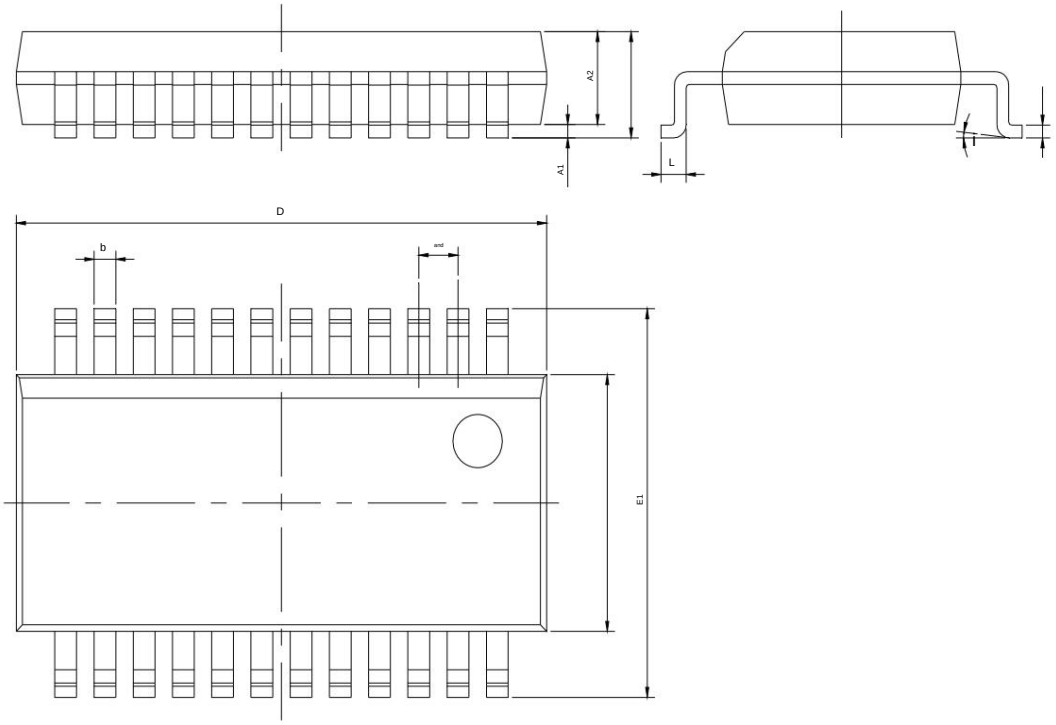
Connecting different resistance values of the R-EXT pin to GND can obtain different constant currents at the output end of the OUT pin, but the voltage at the constant current turning point is different under different constant currents. As can be seen in the figure, the constant current voltage point is ÿ0.8V at 60mA, and the constant current voltage point drops to ÿ0.5V at 15mA. When designing the circuit, the voltage drop at the OUTx end should be fully considered to avoid the driving current failing to reach the preset value.

In addition, the OUTx terminal is not suitable for working at a high voltage drop for a long time when it is turned on, which will increase the power loss of the chip, causing serious heating of the chip and affecting the stability of the system. In actual application,

electromagnetic interference may be generated by signal routing or other factors. To avoid such failures, it is recommended to use DP5020 The shorter the distance to the LED display module, the better.

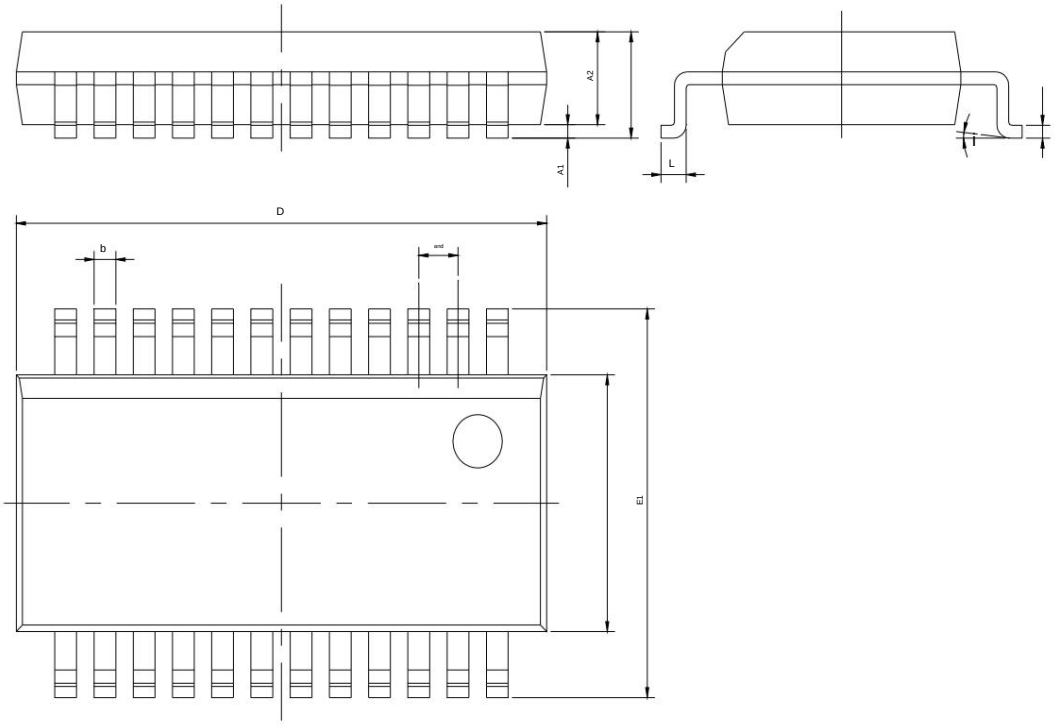
Packaging diagram

SSOP24




| Symbol | Dimensions In Millimeters | | | Dimensions In Inches | | |
|---|---|---|---|---|---|---|
| | Min | Name | Max | Min | Name | Max |
| A | 1.75 | · | 2.10 | 0.069 | · | 0.083 |
| A1 | 0.05 | · | 0.20 | 0.002 | · | 0.008 |
| A2 | 1.70 | · | 1.90 | 0.067 | · | 0.075 |
| b | 0.40TYP | | | 0.016TYPE | | |
| c | 0.09 | · | 0.20 | 0.004 | · | 0.008 |
| D | 12.9 | · | 13.1 | 0.508 | · | 0.516 |
| AND | 5.90 | · | 6.10 | 0.232 | · | 0.240 |
| E1 | 7.6 | · | 8.2 | 0.300 | · | 0.323 |
| and | 1.00TYPE | | | 0.039TYP | | |
| L | 0.33 | · | 0.73 | 0.013 | · | 0.029 |
| i | 0° | · | 8° | 0° | · | 8° |

QSOP24




| Symbol | Dimensions In Millimeters | | | Dimensions In Inches | | |
|---|---|---|---|---|---|---|
| | Min | Name | Max | Min | Name | Max |
| A | 1.35 | 1.60 | 1.75 | 0.0531 | 0.063 | 0.069 |
| A1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| A2 | 1.25 | 1.45 | 1.65 | 0.049 | 0.057 | 0.065 |
| b | 0.21 | | 0.31 | 0.008 | | 0.012 |
| c | 0.25BSC | | | 0.010BSC | | |
| D | 8.53 | 8.63 | 8.73 | 0.336 | 0.340 | 0.344 |
| AND | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| E1 | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| and | 0.535 | 0.635 | 0.735 | 0.021 | 0.025 | 0.029 |
| L | 0.45 | 0.60 | 0.80 | 0.018 | 0.024 | 0.031 |
| i | 0° | | 8° | 0° | | 8° |