National *Semiconductor*

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DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

The DP73048B/DP8304B are high speed Schottky 8-bit TRI-STATE bidirectional transceivers designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic.

Features

■ 8-bit bidirectional data flow reduces system package count
■ Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
■ PNP inputs reduce input loading
■ Output high voltage interfaces with TTL, MOS, and CMOS
■ 48 mA/300 pF bus drive capability
■ Pinouts simplify system interconnections
■ Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
■ Compact 20-pin dual-in-line package
■ Bus port glitch free power up/down

Logic and Connection Diagrams

TL/F/8793–1

Dual-In-Line Package
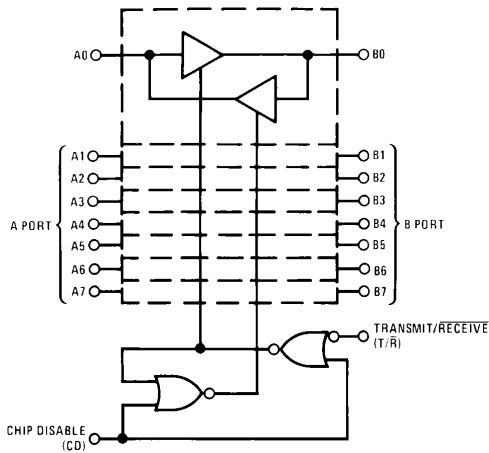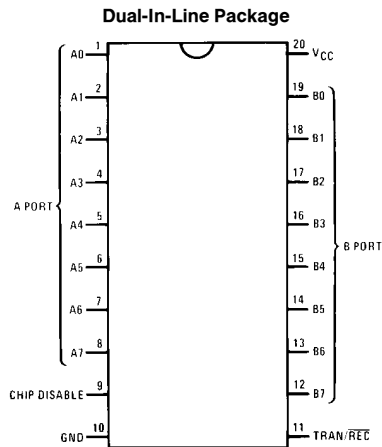
TL/F/8793–2

Top View
Order Number DP7304BJ, DP8304BJ,
DP8304BN or DP8304BWM
See NS Package Number J20A, N20A or M20B

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7304B	4.5	5.5	V
DP8304B	4.75	5.25	V
Temperature (T_A)			
DP7304B	−55	125	°C
DP8304B	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL} I_{OL} = 16 mA (8304B)			0.35	0.5	V
		I_{OL} = 8 mA (both)			0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max (Note 4)		−25	−50	−150	mA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
B PORT (B0–B7) (Continued)							
I_{IH}	Logical "1" Input Current	$CD = V_{IL}$, $T/\overline{R} = V_{IL}$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$CD = 2.0V$, $V_{CC} = Max$, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$CD = V_{IL}$, $T/\overline{R} = V_{IL}$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$CD = 2.0V$, $I_{IN} = -12\ mA$			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$CD = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8304B			0.8	V
			DP7304B			0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$			0.5	20	μA
I_I	Maximum Input Current	$V_{CC} = Max$, $V_{IH} = 5.25V$				1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$	$T/\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12\ mA$			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$CD = 2.0V$, $V_{IN} = 0.4V$, $V_{CC} = Max$			70	100	mA
		$CD = V_{INA} = 0.4V$, $T/\overline{R} = 2V$, $V_{CC} = Max$			90	140	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4V$, $T/\overline{R} = 0.4V$ *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4V$, $T/\overline{R} = 0.4V$ *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 1k, CR = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 30 pF		27	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 5k, C4 = 30 pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4V$, $T/\overline{R} = 2.4V$ *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF		18	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45 pF		11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4V$, $T/\overline{R} = 2.4V$ *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF		16	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45 pF		11	18	ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATIONS (Continued)						
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 16	40 22	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		26 14	35 22	ns ns
TRANSMIT/$\overline{RECEIVE}$ MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to $\overline{Receive}$ a Logical "0", $T/\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to $\overline{Receive}$ a Logical "1", $T/\overline{R}$ to A Port	CD = 0.4V, *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		28	40	ns
t_{RTH}	Propagation Delay from $\overline{Receive}$ Mode to Transmit a Logical "1", $T/\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 1k, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		28	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.
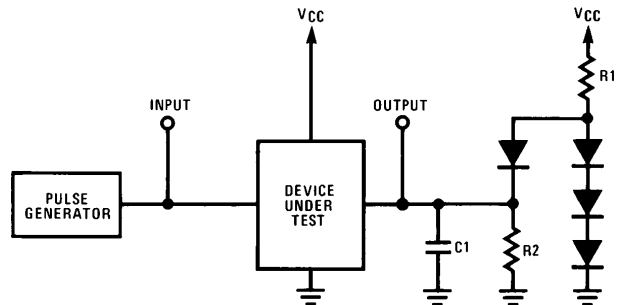
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

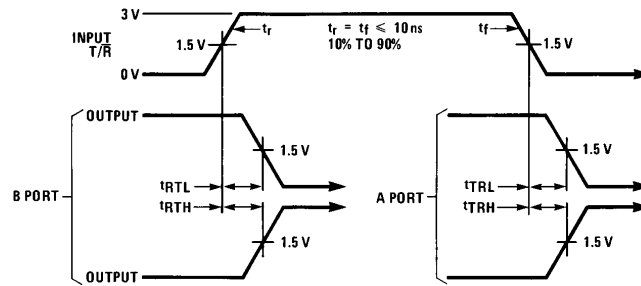## Switching Time Waveforms and AC Test Circuits
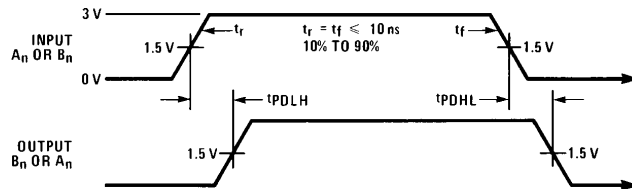
TL/F/8793–3
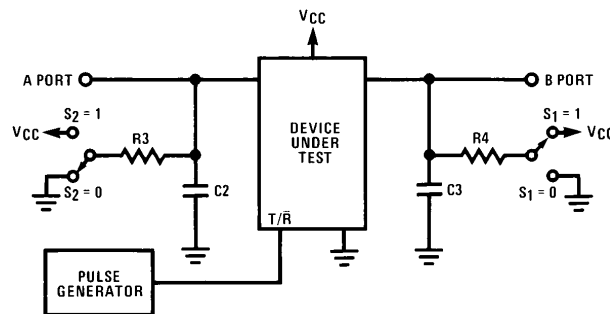

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Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

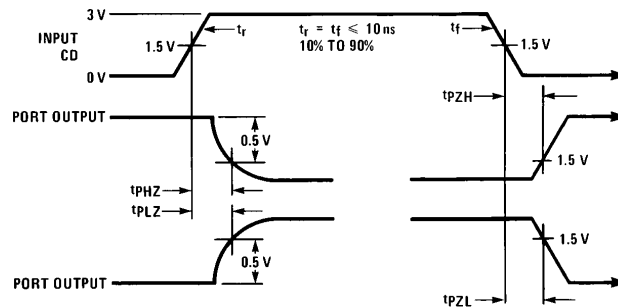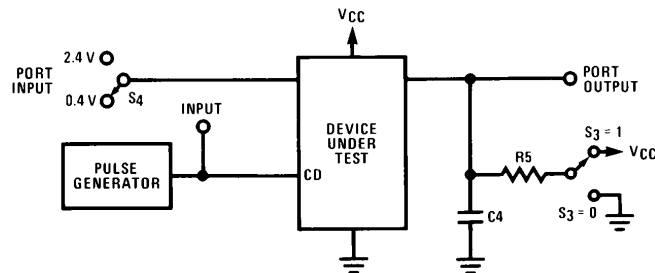# Switching Time Waveforms and AC Test Circuits (Continued)

TL/F/8793–5

Note: C2 and C3 include test fixture capacitance.

TL/F/8793–6

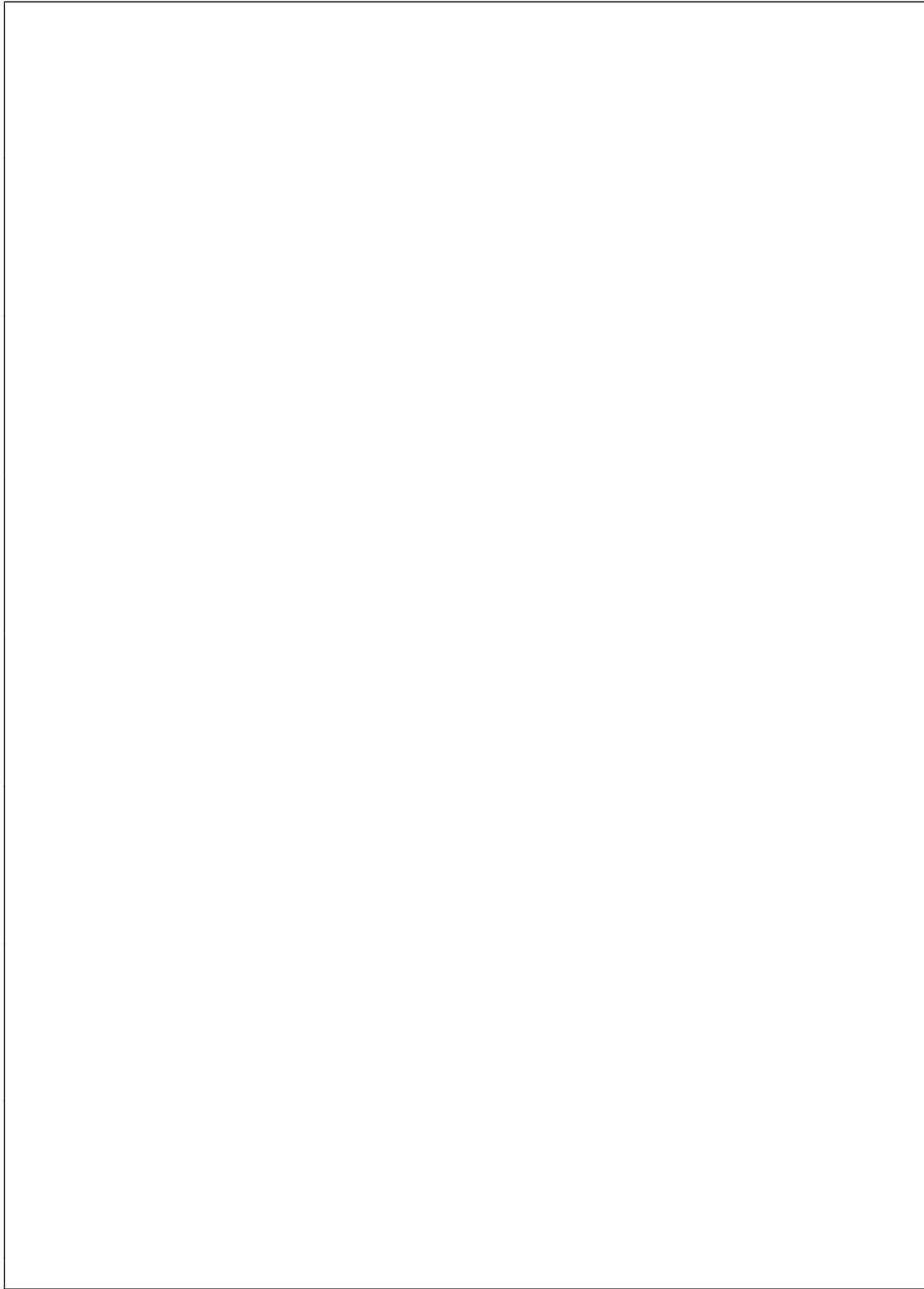**FIGURE B. Propagation Delay from T/R̄ to A Port or B Port**

TL/F/8793–7

TL/F/8793–8

Note: C4 includes test fixture capacitance.
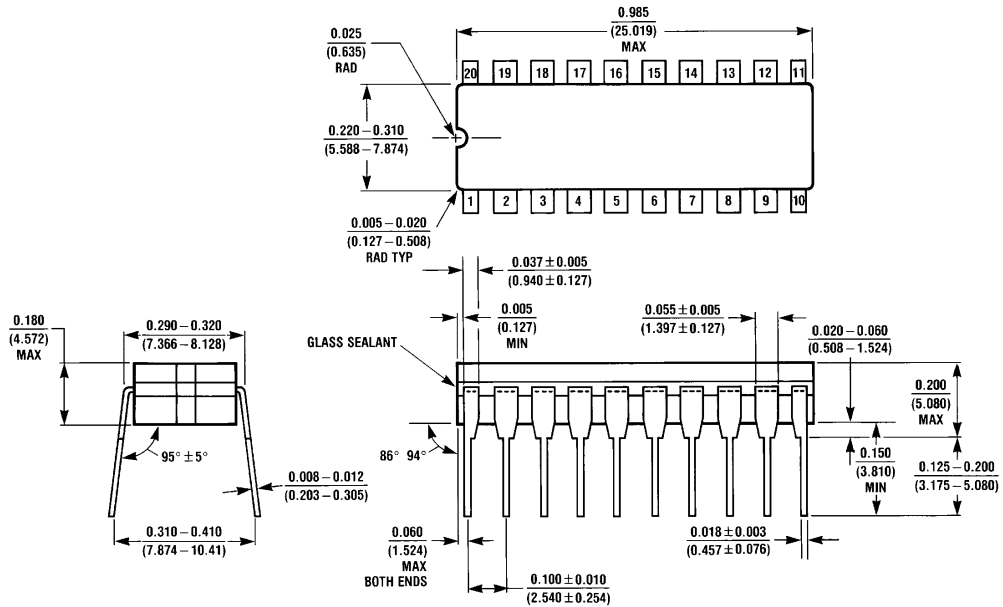
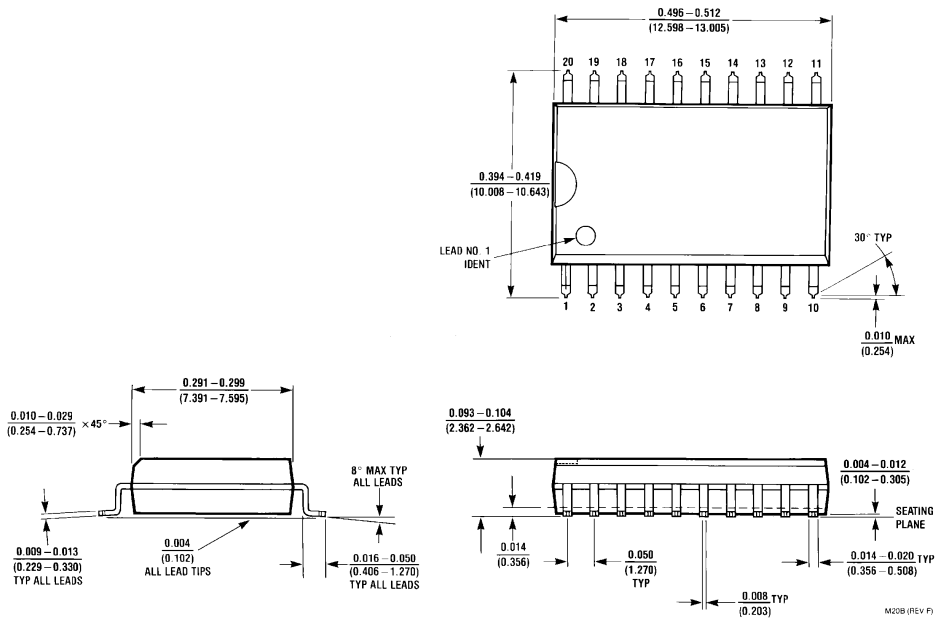Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

http://www.national.com

Physical Dimensions inches (millimeters)

0.025
(0.635)
RAD

0.220 − 0.310
(5.588 − 7.874)

0.005 − 0.020
(0.127 − 0.508)
RAD TYP

0.985
(25.019)
MAX

0.037 ± 0.005
(0.940 ± 0.127)

0.005
(0.127)
MIN

0.055 ± 0.005
(1.397 ± 0.127)

0.020 − 0.060
(0.508 − 1.524)

GLASS SEALANT

0.200
(5.080)
MAX

0.150
(3.810)
MIN

0.125 − 0.200
(3.175 − 5.080)

0.180
(4.572)
MAX

0.290 − 0.320
(7.366 − 8.128)

95° ± 5°

0.008 − 0.012
(0.203 − 0.305)

86° 94°

0.310 − 0.410
(7.874 − 10.41)

0.060
(1.524)
MAX
BOTH ENDS

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ± 0.003
(0.457 ± 0.076)

J20A (REV M)

Ceramic Dual-In-Line Package (J)
Order Number DP7304BJ or DP8304BJ
NS Package Number J20A

0.496 − 0.512
(12.598 − 13.005)

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

30° TYP

0.010
(0.254) MAX

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M20B (REV F)

SO Package (M)
Order Number DP8304BWM
NS Package Number M20B

http://www.national.com

Physical Dimensions inches (millimeters) (Continued)

1.013–1.040
(25.73–26.42)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

PIN NO. 1 IDENT

OPTION 1

0.260 ±0.005
(6.604 ±0.127)

0.280
(7.112)
MIN

0.300–0.320
(7.620–8.128)

0.065
(1.651)

0.090
(2.286)

0.060
(1.524)
NOM
TYP

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.130 0.005
(3.302 0.127)

0.145–0.200
(3.683–5.080)

0.032 ±0.005
(0.813 ±0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

95°± 5°

0.009–0.015
(0.229–0.381)
TYP

0.100 ±0.010
(2.540 ±0.254)

90°±0.004°

0.018 ±0.003
(0.457 ±0.076)

0.020
(0.508)
MIN

0.125–0.140
(3.175–3.556)

0.060 ±0.005
(1.524 ±0.127)

0.325 +0.040
       −0.015

(8.255 +1.016
        −0.381)

N20A (REV G)

Molded Dual-In-Line Package (N)
Order Number DP8304BN
NS Package Number N20A

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.