



DP80390XP

Pipelined High Performance

8-bit Microcontroller

ver 3.10

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OVERVIEW

DP80390XP is an **ultra high performance, speed optimized** soft core of a single-chip 8-bit embedded controller dedicated for operation with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern about **performance to power consumption** ratio. This ratio is extended by an advanced power management unit **PMU**.

DP80390XP soft core is 100% binary-compatible with the industry standard 80390 & 8051 8-bit microcontroller. There are two configurations of DP80390XP: **Harward** where internal data and program buses are separated, and **von Neumann** with common program and external data bus. DP80390XP has Pipelined RISC architecture **10 times faster** compared to standard architecture and executes **85-200 million instructions** per second. This performance can also be exploited to great advantage in **low power** applications where the core can be clocked over ten times more slowly than the original implementation for no performance penalty.

DP80390XP is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

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CPU FEATURES

- 100% software compatible with industry standard 80390 & 8051
 - *LARGE mode – 8051 instruction set*
 - *FLAT mode – 80390 instruction set*
- Pipelined RISC architecture enables to execute instructions 10 times faster compared to standard 8051
- 24 times faster multiplication
- 12 times faster addition
- 2 Data Pointers (DPTR) for faster memory blocks copying
 - *Advanced INC & DEC modes*
 - *Auto-switch of current DPTR*
- Up to 256 bytes of internal (on-chip) Data Memory
- **Up to 16M bytes of linear Program Memory**
 - *64 kB of internal (on-chip) Program Memory*
 - *16 MB external (off-chip) Program Memory*
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed

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- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory
- Dedicated signal for Program Memory writes.
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready
- **2.0 GHz virtual** clock frequency in a 0.35u technological process

PERIPHERALS

- DoCD™ debug unit
 - Processor execution control
 - Run
 - Halt
 - Step into instruction
 - Skip instruction
 - Read-write all processor contents
 - Program Counter (PC)
 - Program Memory
 - Internal (direct) Data Memory
 - Special Function Registers (SFRs)
 - External Data Memory
 - Hardware execution breakpoints
 - Program Memory
 - Internal (direct) Data Memory
 - Special Function Registers (SFRs)
 - External Data Memory
 - Hardware breakpoints activated at a certain
 - Program address (PC)
 - Address by any write into memory
 - Address by any read from memory
 - Address by write into memory a required data
 - Address by read from memory a required data
 - Three wire communication interface
- Power Management Unit
 - Power management mode
 - Switchback feature
- Stop mode
- Extended Interrupt Controller
 - 2 priority levels
 - Up to 7 external interrupt sources
 - Up to 8 interrupt sources from peripherals
- Four 8-bit I/O Ports
 - Bit addressable data direction for each line
 - Read/write of single line and 8-bit group
- Three 16-bit timer/counters
 - Timers clocked by internal source
 - Auto reload 8/16-bit timers
 - Externally gated event counters
- Full-duplex serial port
 - Synchronous mode, fixed baud rate
 - 8-bit asynchronous mode, fixed baud rate
 - 9-bit asynchronous mode, fixed baud rate
 - 9-bit asynchronous mode, variable baud rate
- I2C bus controller - Master
 - 7-bit and 10-bit addressing modes
 - NORMAL, FAST, HIGH speeds
 - Multi-master systems supported
 - Clock arbitration and synchronization
 - User defined timings on I2C lines
 - Wide range of system clock frequencies
 - Interrupt generation
- I2C bus controller - Slave
 - NORMAL speed 100 kbs
 - FAST speed 400 kbs
 - HIGH speed 3400 kbs
 - Wide range of system clock frequencies
 - User defined data setup time on I2C lines
 - Interrupt generation
- SPI – Master and Slave Serial Peripheral Interface
 - Supports speeds up ¼ of system clock
 - Mode fault error
 - Write collision error
 - Four transfer formats supported
 - System errors detection
 - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)

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- *Interrupt generation*
- Programmable Watchdog Timer
- 16-bit Compare/Capture Unit
 - *Events capturing*
 - *Pulses generation*
 - *Digital signals generation*
 - *Gated timers*
 - *Sophisticated comparator*
 - *Pulse width modulation*
 - *Pulse width measuring*
- Fixed-Point arithmetic coprocessor
 - *Multiplication - 16bit * 16bit*
 - *Division - 32bit / 16bit*
 - *Division - 16bit / 16bit*
 - *Left and right shifting - 1 to 31 bits*
 - *Normalization*
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
 - *FADD, FSUB - addition, subtraction*
 - *FMUL, FDIV- multiplication, division*
 - *FSQRT- square root*
 - *FUCOM - compare*
 - *FCHS - change sign*
 - *FABS - absolute value*
- Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers
 - *FADD, FSUB- addition, subtraction*
 - *FMUL, FDIV- multiplication, division*
 - *FSQRT- square root*
 - *FUCOM- compare*
 - *FCHS - change sign*
 - *FABS - absolute value*
 - *FSIN, FCOS- sine, cosine*
 - *FTAN, FATAN- tangent, arcs tangent*

CONFIGURATION

The following parameters of the DP80390XP core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortlessly changing appropriate constants in package file.

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There is no need to change any parts of the code.

- Internal Program Memory - synchronous
- asynchronous
- Internal Program ROM Memory size - 0 - 64kB
- Internal Program RAM Memory size - 0 - 64kB
- Internal Program Memory fixed size - true
- false
- Second Data Pointer (DPTR1) - used
- unused
- DPTR0 decrement - used
- unused
- DPTR1 decrement - used
- unused
- Data Pointers auto-switch - used
- unused
- Interrupts - subroutines
- location
- Timing access protection - used
- unused
- Power Management Mode - used
- unused
- Stop mode - used
- unused
- DoCD™ debug unit - used
- unused

Besides mentioned above parameters all available peripherals and external interrupts can be excluded from the core by changing appropriate constants in package file.

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application

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- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, One Year licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except One Year license where time of use is limited to 12 months.

- Single Design license for
 - VHDL, Verilog source code called HDL Source
 - Encrypted, or plain text EDIF called Netlist
- One Year license for
 - Encrypted Netlist only
- Unlimited Designs license for
 - HDL Source
 - Netlist
- Upgrade from
 - HDL Source to Netlist
 - Single Design to Unlimited Designs

DESIGN FEATURES

◆ PROGRAM MEMORY:

The DP80390 soft core is dedicated for operation with Internal and External Program Memory. Its maximal linear size is equal to 16 MB. Internal Program Memory can be implemented as:

- ROM located in address range between $0000h \div (ROM_{size}-1)$
- RAM located in address range between $(64kB-RAM_{size}) \div FFFFh$

External Program Memory can be implemented as ROM or RAM located in address range between $ROM_{size} \div 16 MB$ excluding area occupied by RAM_{size} .

◆ INTERNAL DATA MEMORY:

The DP80390XP can address Internal Data Memory of up to 256 bytes. The Internal Data Memory can be implemented as Single-Port synchronous RAM.

◆ EXTERNAL DATA MEMORY:

The DP80390XP soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

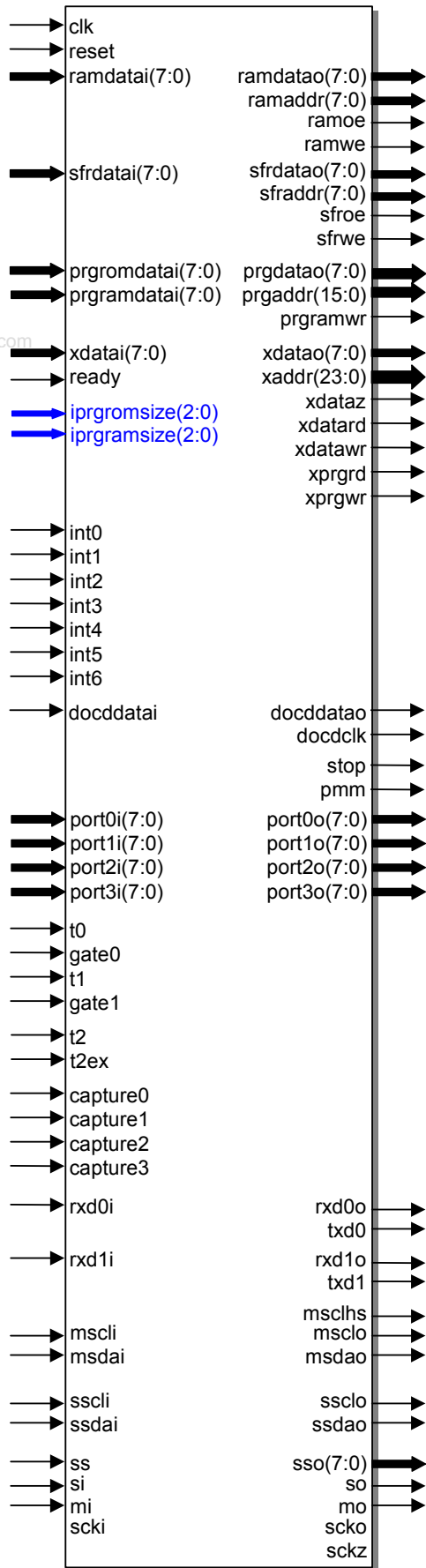
◆ USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DP80390XP design. ESFRs are memory mapped into Direct Memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

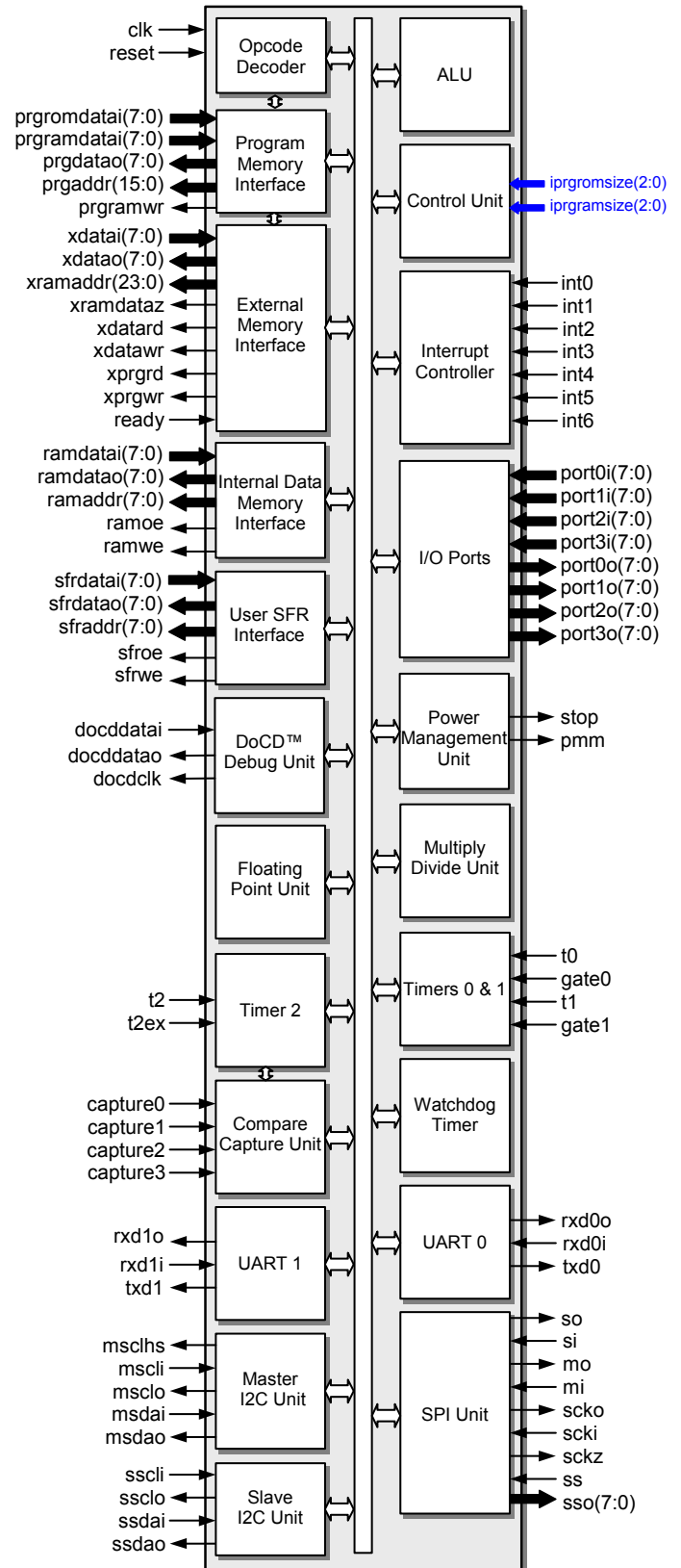
◆ WAIT STATES SUPPORT:

The DP80390XP soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

SYMBOL



BLOCK DIAGRAM



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PINS DESCRIPTION

| PIN | TYPE | DESCRIPTION |
|------------------|--------|-------------------------------------|
| clk | input | Global clock |
| reset | input | Global reset |
| port0i[7:0] | input | Port 0 input |
| port1i[7:0] | input | Port 1 input |
| port2i[7:0] | input | Port 2 input |
| port3i[7:0] | input | Port 3 input |
| iprgramsize[2:0] | input | Size of on-chip RAM CODE |
| iprgromsize[2:0] | input | Size of on-chip ROM CODE |
| prgramdata[7:0] | input | Data bus from int. RAM prog. memory |
| prgromdata[7:0] | input | Data bus from int. ROM prog. memory |
| xdatai[7:0] | input | Data bus from external memories |
| ready | input | External memory data ready |
| ramdatai[7:0] | input | Data bus from internal data memory |
| sfrdatai[7:0] | input | Data bus from user SFR's |
| int0 | input | External interrupt 0 |
| int1 | input | External interrupt 1 |
| int2 | input | External interrupt 2 |
| int3 | input | External interrupt 3 |
| int4 | input | External interrupt 4 |
| int5 | input | External interrupt 5 |
| int6 | input | External interrupt 6 |
| t0 | input | Timer 0 input |
| t1 | input | Timer 1 input |
| t2 | input | Timer 2 input |
| gate0 | input | Timer 0 gate input |
| gate1 | input | Timer 1 gate input |
| t2ex | input | Timer 2 gate input |
| capture0 | input | Timer 2 capture 0 line |
| capture1 | input | Timer 2 capture 1 line |
| capture2 | input | Timer 2 capture 2 line |
| capture3 | input | Timer 2 capture 3 line |
| rxdi0 | input | Serial receiver input 0 |
| rxdi1 | input | Serial receiver input 1 |
| mscli | input | Master I2C clock line input |
| msdai | input | Master I2C data input |
| sscli | input | Slave I2C clock line input |
| ssdai | input | Slave I2C data input |
| ss | input | SPI slave select |
| si | input | SPI slave input |
| mi | input | SPI master input |
| scki | input | SPI clock input |
| docddatai | input | DoCD™ data input |
| port0o[7:0] | output | Port 0 output |
| port1o[7:0] | output | Port 1 output |
| port2o[7:0] | output | Port 2 output |
| port3o[7:0] | output | Port 3 output |
| prgaddr[15:0] | output | Internal program memory address bus |

| | | |
|---------------|--------|---|
| prgdatao[7:0] | output | Data bus for internal program memory |
| prgramwr | output | Internal program memory write |
| xaddr[23:0] | output | Address bus for external memories |
| xdatao[7:0] | output | Data bus for external memories |
| xdataz | output | Turn xdata bus into 'Z' state |
| xprgrd | output | External program memory read |
| xprgwr | output | External program memory write |
| xramrd | output | External data memory read |
| xramwr | output | External data memory write |
| ramaddr[7:0] | output | Internal Data Memory address bus |
| ramdatao[7:0] | output | Data bus for internal data memory |
| ramoe | output | Internal data memory output enable |
| ramwe | output | Internal data memory write enable |
| sfraddr[6:0] | output | Address bus for user SFR's |
| sfrdatao[7:0] | output | Data bus for user SFR's |
| sfro | output | User SFR's read enable |
| sfrwe | output | User SFR's write enable |
| docddatao | output | DoCD™ data output |
| docdclk | output | DoCD™ clock line |
| pmm | output | Power management mode indicator |
| stop | output | Stop mode indicator |
| rxdo | output | Serial receiver output 0 |
| rxdo | output | Serial receiver output 1 |
| txdo | output | Serial transmitter output 0 |
| txdo | output | Serial transmitter output 1 |
| msclo | output | Master I2C clock output |
| msclhs | output | High speed Master I2C clock line |
| msdao | output | Master I2C data output |
| msclo | output | Slave I2C clock output |
| msdao | output | Slave I2C data output |
| sso[7:0] | output | SPI slave select lines |
| so | output | SPI slave output |
| mo | output | SPI master output |
| scko | output | SPI clock output |
| sckz | output | SPI clock line tri-state buffer control |

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic such as arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

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Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader loading new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Memory Interface - Contains memory access related registers such as Data Page High (DPH), Data Page Low (DPL) and Data Pointer eXtended (DPX) registers. It performs the external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States, and allows core to work with different speed program memories.

Internal Data Memory Interface – Internal Data Memory interface controls access into the internal 256 bytes memory. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and user defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.

I/O Ports – Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, P3.

Power Management Unit – Block contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode) to significantly reduce power consumption. Switchback feature allows UARTs, and interrupts to be processed in full speed mode if enabled. It is very desired when microcontroller is planned to use in portable and power critical applications.

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

Floating Point Unit – Block contains floating point arithmetic IEEE-754 compliant instructions (C *float*, *int*, *long int* types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of sign. Basing on specialized CORDIC algorithm a full set of trigonometric operations are also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit has included standard software interface allows easy usage and interfacing with user C/ASM written programs.

Multipl Divide Unit – It's a fixed point fast 16-bit and 32-bit multiplication and division unit. It provides shift and normalize operations, additionally. All operations are performed using unsigned integer numbers. The MDU contains MD0 to MD5 operands, the result registers and one control register called ARCON. This unit has included standard software interface allows easy usage and interfacing with user C/ASM written programs.

Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0,

TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods when appropriate timer is enabled. In the counter mode the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

Timer 2 – Second system timer module contains one 16-bit configurable timer: Timer 2 (TH2, TL2), capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit if it's presented in system. It can be used as clock source for UART0.

Compare Capture Unit – The compare / capture / reload unit is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing such as pulse generation, pulse width modulation, measurements etc.

Watchdog Timer – The watchdog timer is a 27-bit counter which is incremented every system clock periods (CLK pin). It performs system protection against software upsets.

UART0 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2.

UART1 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF1 loads the transmit register, and reading SBUF1 reads a physically separate receive

register. Works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer 1.

Master I2C Unit – I2C bus controller is a Master module. The core incorporates all features required by I2C specification. Supports both 7-bit and 10-bit addressing modes on the I2C bus. It works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization to allow it operate in multi-master systems. Built-in timer allows operation from a wide range of the input frequencies. The timer allows to achieve any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast and High Speed up to 3400 kbs.

Slave I2C Unit – I2C bus controller is a Slave module. The core incorporates all features required by I2C specification. It works as a slave transmitter/receiver depending on working mode determined by a master device. The I2C controller supports all transmission modes: Standard, Fast and High Speed up to 3400 kbs.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. SPI automatically drives slave select outputs SSO[7:0], and address SPI slave device to exchange serially shifted data. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI

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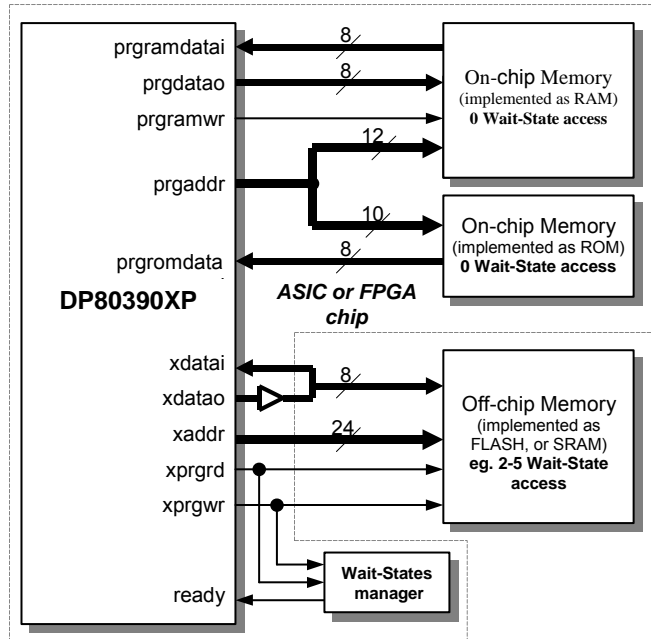
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devices simultaneously attempts to become bus master.

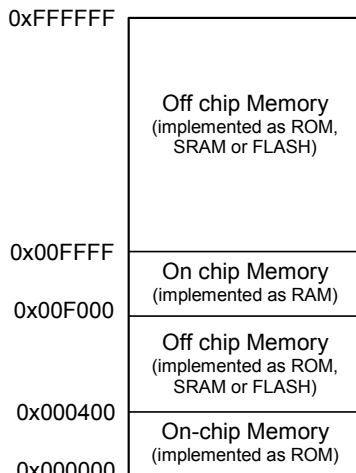
PROGRAM CODE SPACE IMPLEMENTATION

The figure below shows an example Program Memory space implementation in systems with DP80390XP Microcontroller core. The On-chip Program Memory located in address space between 0kB and 1kB is typically used for BOOT code with system initialization functions. This part of the code is typically implemented as ROM. The On-chip Program Memory located in address space between 60kB and 64kB is typically used for timing critical part of the code e.g. interrupt subroutines, arithmetic functions etc. This part of the code is typically implemented as RAM and can be loaded by the BOOT code during initialization phase from Off-chip memory or through RS232 interface from external device. From the two mentioned above spaces program code is executed without wait-states and can achieve a top performance up to 200 million instructions per second (many instructions executed in one clock cycle). The Off-chip Program Memory located in address space between 1kB and 60kB, and above 64 kB is typically used for main code and constants. This part of the code is usually implemented as ROM, SRAM or FLASH device. Because of relatively long access time the program code executed from mentioned above devices must be fetched with additional Wait-States. Number of required Wait-States depends on memory access time and DP80390XP clock frequency. In most cases the proper number of Wait-States cycles is between 2-5. The READY pin can be also dynamically modulated e.g. by SDRAM controller.

The figure below shows a typical Program Memories connections in system with DP80390XP Microcontroller core.



The described above implementation should be treated as an example. All Program Memory spaces are fully configurable. For timing-critical applications whole program code can be implemented as on-chip ROM and (or) RAM and executed without Wait-States, but for some other applications whole program code can be implemented as off-chip ROM or FLASH and executed with required number Wait-State cycles.



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PERFORMANCE

The following tables give a survey about the Core area and performance in ASICs Devices (CPU features and peripherals have been included):

| Device | Optimization | F _{max} |
|---------------|--------------|------------------|
| 0.25u typical | area | 100 MHz |
| 0.25u typical | speed | 200 MHz |

Core performance in ASIC devices

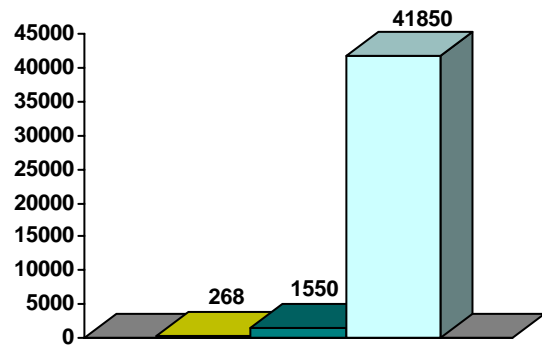
For a user the most important is application speed improvement. The most commonly used arithmetic functions and their improvement are shown in table below. Improvement was computed as {80C51 clock periods} divided by {DP80390XP clock periods} required to execute an identical function. More details are available in core documentation.

| Function | Improvement |
|--|--------------|
| 8-bit addition (<i>immediate data</i>) | 9,00 |
| 8-bit addition (<i>direct addressing</i>) | 9,00 |
| 8-bit addition (<i>indirect addressing</i>) | 9,00 |
| 8-bit addition (<i>register addressing</i>) | 12,00 |
| 8-bit subtraction (<i>immediate data</i>) | 9,00 |
| 8-bit subtraction (<i>direct addressing</i>) | 9,00 |
| 8-bit subtraction (<i>indirect addressing</i>) | 9,00 |
| 8-bit subtraction (<i>register addressing</i>) | 12,00 |
| 8-bit multiplication | 16,00 |
| 8-bit division | 9,60 |
| 16-bit addition | 12,00 |
| 16-bit subtraction | 12,00 |
| 16-bit multiplication | 13,60 |
| 32-bit addition | 12,00 |
| 32-bit subtraction | 12,00 |
| 32-bit multiplication | 12,60 |
| Average speed improvement: | 11,12 |

Dhrystone Benchmark Version 2.1 was used to measure Core performance. The following table gives a survey about the DP80390XP performance in terms of Dhrystone/sec and VAX MIPS rating.

| Device | Target | Clock frequency | Dhry/sec (VAX MIPS) |
|-----------|--------|-----------------|---------------------|
| 80C51 | - | 12 MHz | 268 (0.153) |
| 80C310 | - | 33 MHz | 1550 (0.882) |
| DP80390XP | 0.25u | 200 MHz | 41850 (23,800) |

Core performance in terms of Dhrystones



■ 80C51 (12MHz)
 ■ 80C310 (33MHz)
 ■ DP80390XP (200MHz)

Area utilized by the each unit of DP80390XP core in vendor specific technologies is summarized in table below.

| Component | Area | |
|---------------------------|--------------|-------------|
| | [Gates] | [FFs] |
| CPU* | 6500 | 310 |
| DPTR1 register | 300 | 32 |
| DPTR0 decrement | 100 | - |
| DPTR1 decrement | 100 | - |
| DPTR0 & DPTR1 auto-switch | 50 | 8 |
| Timed Access protection | 100 | 10 |
| Interrupt Controller | 500 | 40 |
| INT2-INT6 | 350 | 25 |
| Power Management Unit | 50 | 5 |
| I/O ports | 400 | 35 |
| Timers | 600 | 50 |
| Timer 2 | 600 | 60 |
| UART0 | 700 | 60 |
| UART1 | 700 | 60 |
| Master I2C Unit | 900 | 120 |
| Slave I2C Unit | 550 | 70 |
| SPI Unit | 450 | 55 |
| Compare Capture Unit | 550 | 60 |
| Watchdog Timer | 400 | 45 |
| Multiply Divide Unit | 1700 | 105 |
| Total area | 15600 | 1155 |

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface
Core components area utilization

The main features of each DP80390 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

| Design | Architecture speed grade | | | Program Memory space | | | Stack space size | Internal Data Memory space | External Data Memory space | External Data / Program Memory Wait States | Power Management Unit | Interface for additional SFRs | Interrupt sources | Interrupt levels | Data Pointers | Timer/Counters | UART | I/O Ports | Compare/Capture | Watchdog | Master I ² C Bus Controller | Slave I ² C Bus Controller | SPI | Fixed Point Coprocessor | Floating Point Coprocessor |
|------------|--------------------------|-------------|----------|----------------------|-----|-----|------------------|----------------------------|----------------------------|--|-----------------------|-------------------------------|-------------------|------------------|---------------|----------------|------|-----------|-----------------|----------|--|---------------------------------------|-----|-------------------------|----------------------------|
| | on-chip RAM | on-chip ROM | off-chip | | | | | | | | | | | | | | | | | | | | | | |
| DP80390CPU | 10 | 64k | 64k | 16M | 256 | 256 | 16M | ✓ | ✓ | ✓ | ✓ | 2 | 2 | 1 | - | - | - | - | - | - | - | - | - | - | - |
| DP80390 | 10 | 64k | 64k | 16M | 256 | 256 | 16M | ✓ | ✓ | ✓ | ✓ | 5 | 2 | 1 | 2 | 1 | 4 | - | - | - | - | - | - | - | - |
| DP80390XP | 10 | 64k | 64k | 16M | 256 | 256 | 16M | ✓ | ✓ | ✓ | ✓ | 15 | 2 | 2 | 3 | 2 | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

DP80390 family of Pipelined High Performance Microcontroller Cores

The main features of each DP8051 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

| Design | Architecture speed grade | | | Program Memory space | | | Stack space size | Internal Data Memory space | External Data Memory space | External Data / Program Memory Wait States | Power Management Unit | Interface for additional SFRs | Interrupt sources | Interrupt levels | Data Pointers | Timer/Counters | UART | I/O Ports | Compare/Capture | Watchdog | Master I ² C Bus Controller | Slave I ² C Bus Controller | SPI | Fixed Point Coprocessor | Floating Point Coprocessor |
|-----------|--------------------------|-------------|----------|----------------------|-----|-----|------------------|----------------------------|----------------------------|--|-----------------------|-------------------------------|-------------------|------------------|---------------|----------------|------|-----------|-----------------|----------|--|---------------------------------------|-----|-------------------------|----------------------------|
| | on-chip RAM | on-chip ROM | off-chip | | | | | | | | | | | | | | | | | | | | | | |
| DP8051CPU | 10 | 64k | 64k | 64k | 256 | 256 | 16M | ✓ | ✓ | ✓ | ✓ | 2 | 2 | 1 | - | - | - | - | - | - | - | - | - | - | - |
| DP8051 | 10 | 64k | 64k | 64k | 256 | 256 | 16M | ✓ | ✓ | ✓ | ✓ | 5 | 2 | 1 | 2 | 1 | 4 | - | - | - | - | - | - | - | - |
| DP8051XP | 10 | 64k | 64k | 64k | 256 | 256 | 16M | ✓ | ✓ | ✓ | ✓ | 15 | 2 | 2 | 3 | 2 | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

DP8051 family of Pipelined High Performance Microcontroller Cores

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