National Semiconductor

PRELIMINARY

DP83922A
Twisted Pair Transceiver Interface (TPI)

General Description

The DP83922A Twisted Pair Transceiver is used to connect IEEE 802.3 stations and repeaters to a twisted-pair cable medium. It integrates all the transceiver medium attachment unit (MAU) functions as specified in the IEEE 802.3 10BASE-T standard.

The DP83922A contains a full AUI interface, which makes it ideal for use both in stand-alone and integrated MAU applications. The DP83922A's primary functional blocks include transmitter, receiver, collision detection, jabber timer, link test, and SQE test (CD Heartbeat) with a disable pin for repeater applications.

The DP83922A also provides display outputs that directly drive LEDs to indicate status for all MAU functions. The TPI indicates receive and transmit activity, jabber and collision indication, and link (cable connectivity) status.

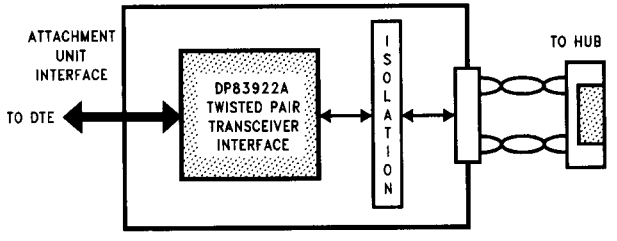
The DP83922A is part of a chip set that implements the complete IEEE802.3 10BASE-T compatible network electronics. In node applications, it can be used with the DP83910 Serial Network Interface (SNI) and the DP8390 Network Interface Controller (NIC) or the DP83932 SONIC™. The TPI may also be used in repeater applications.

Features

- Compatible with IEEE802.3 10BASE-T standard
- Integrates transceiver electronics, including:
  - — Transmitter
  - — Receiver
  - — Collision Detection
  - — CD Heartbeat
  - — Jabber Timer
  - — Link Integrity Test
- Link disable enables operation with pre-standard 10BASE-T twisted pair implementations
- Fully AUI compatible interface for both stand-alone and embedded MAU applications
- Programmable transmit and equalization levels
- Complete differential transmit and receive path for optimum jitter performance
- Transmit output waveform shaping reduces filter requirements
- Status LED Outputs
  - — Link, Transmit, Receive, Jabber, and Collision
- 24-pin narrow DIP package

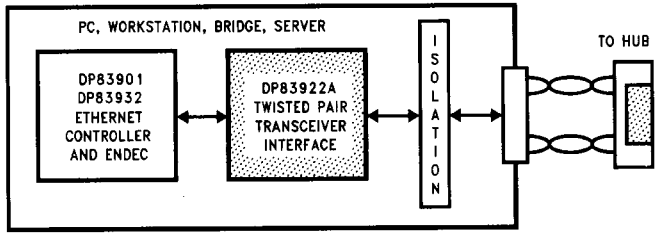
System Diagrams

Stand-Alone Twisted Pair MAU



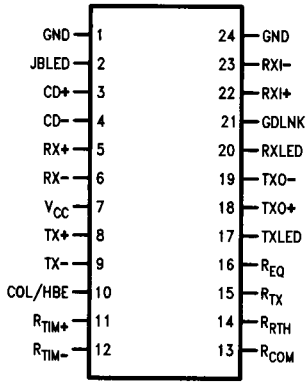
TL/F/10490–1

Node with Integrated Twisted Pair MAU



TL/F/10490–2

Connection Diagram



TL/F/10490–3

Top View

Order Number DP83922AN
See NS Package Number N24C

Pin Description

Pin No.	Pin Name	I/O	Description
1, 24	GND	—	**Ground Supply Pin**
2	JBLED	O	**Jabber LED:** This output indicates that the DTE or repeater transmitting into the TX± is jabbering (transmitting an excessively long packet). This is indicated when this output is low. This information may be displayed using a Light Emitting Diode (LED).
3 4	CD+, (CI+) CD−, (CI−)	O (AUI*)	**Collision Output:** Balanced differential line driver outputs. The 10 MHz signal from the internal oscillator is transferred to these outputs in the event of collision, excessive transmission (jabber), or during SQE Test. These outputs are emitter followers and require external pulldown resistors to GND.
5 6	RX+, (DI+) RX−, (DI−)	O (AUI)	**Receive Output:** Balanced differential line driver outputs from the TPI's receiver. These outputs are also emitter followers and require pulldown resistors to GND.
7	V_{CC}	—	**Positive 7V Supply:** A 0.1 μF ceramic decoupling capacitor must be connected across GND and V_{CC} as close to the device as possible.
8 9	TX+, (DO+) TX−, (DO−)	I (AUI)	**Transmit Input:** Balanced differential inputs to the twisted pair transmitter. The common mode voltage for these inputs is set internally and must not be externally biased.
10	COL/HBE	I/O	**Collision LED/Heartbeat Enable:** This dual-function pin disables the Heartbeat (SQE test) function when it is tied to GND. When connected to V_{CC} through an LED and series resistor, this output indicates that a collision is occurring.
11 12	R_{TIM+} R_{TIM-}	I	**Timing Resistor Pins:** A resistor is connected across these pins. This resistor is used to set the timing reference for the device.
13	R_{COM}	I	**Common Resistor Input:** Resistors are attached to this pin. This input is the common reference point for the R_{RTH}, R_{TX}, and R_{EQ}.
14	R_{RTH}	I	**Receiver Threshold Resistor:** A resistor attached to this pin sets the threshold of the twisted pair receiver squelch circuit.

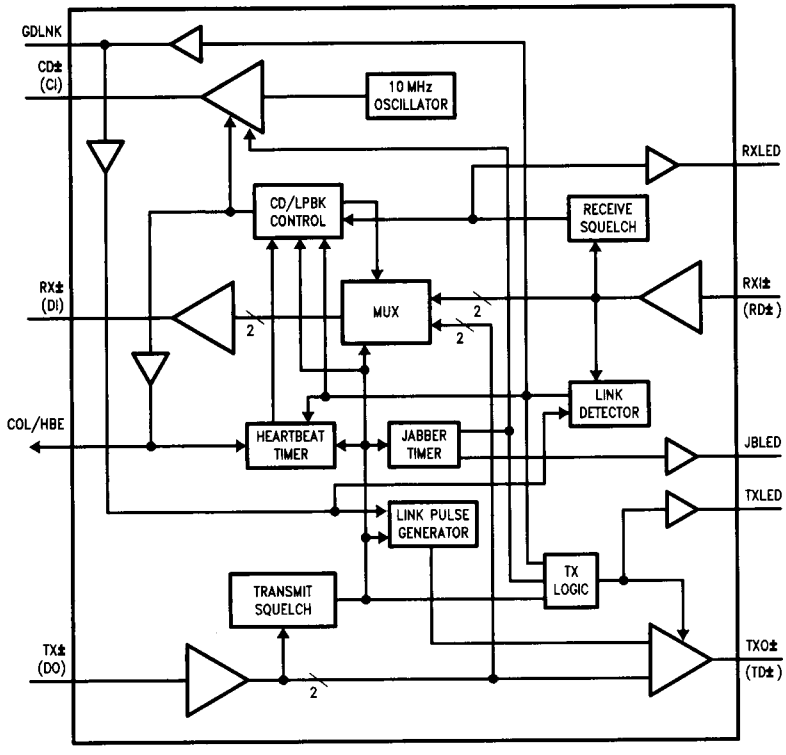
*AUI—Pins connect to Attachment Unit Interface.

Pin Description (Continued)

Pin No.	Pin Name	I/O	Description	
15 16	R_{TX} R_{EQ}	I	**Transmit Level Resistor** **Equalization Resistor**	Resistors connected to these pins are used to determine the transmit levels for the equalized output.
17	TXLED	O	**Transmit LED:** This output goes low when valid transmissions are output from the TPI. When the transmitter is disabled due to a Jabber or link fault this output is off (TRI-STATE®). This can be used to drive a status LED.	
18 19	TXO+ (TD+) TXO− (TD−)	O (TP*)	**Twisted Pair Transmit Outputs:** Balanced differential current drivers that allow external resistors and filter network to determine the output impedance. (the details of the operation of these outputs can be found in the functional description)	
20	RXLED	O	**Receive LED:** This output goes low when data is received by the TPI. This can be used to drive a status LED.	
21	GDLNK	I/O	**Good Link:** This dual-function pin indicates successful reception of link pulses by going low. This information may be displayed using a Light Emitting Diode (LED). When this pin is tied to ground the link generator, and link receive state logic is disabled.	
22 23	RXI+ (RD+) RXI− (RD−)	I (TP)	**Twisted Pair Receive Inputs:** These high impedance inputs feed a differential amplifier which then transmits the signal differentially along the receive path. The common mode voltage for these inputs is set internally and should not be altered.	

*TP—Pins connect to Twisted Pair Interface.

Block Diagram



TL/F/10490–4

Functional Description

The TPI consists of 6 basic functional blocks:

1. Receiver: This block receives data from the twisted pair wire and sends it to the DTE (Data Terminal Equipment) via the Attachment Unit Interface (AUI). In the block diagram this section is composed of the RXI± input receiver, receive squelch, the MUX and the RXI output driver.
2. Transmitter: This accepts data from the DTE connected via the AUI and transmits it onto the twisted pair cabling. In the block diagram this section is composed of the TX± input receiver, transmit squelch, and the TXO± output driver.
3. Collision Detection: This indicates to the DTE that a collision is occurring by transmitting a 10 MHz signal to the DTE. In the block diagram this section consists of the CD/Loopback Control, the 10 MHz oscillator and the CD± output driver.
4. Jabber Timer: This disables the transmitter if it was transmitting a longer than legal packet.
5. SQE (Signal Quality Error) Test: This is accomplished by the Heartbeat Timer block which generates a short burst of collision signal after every transmission.
6. Link Test: This block consists of the Link Pulse Generator and Link Detector. This block checks the integrity of the cable connecting two twisted pair MAUs.

RECEIVE FUNCTION

Receive Path

The receive path logic consists of the twisted pair receiver, loopback multiplexer, and AUI driver. From input to output the receive path is fully differential and both RX+ and RX− are matched. This provides low signal skews and jitter.

After the received signal passes through the differential input buffer, it enters the loopback multiplexer. The multiplexer routes either the received data or transmit data to the RX± pins. When the TPI is receiving valid data from the twisted pair cable, this data is sent to RX± outputs.

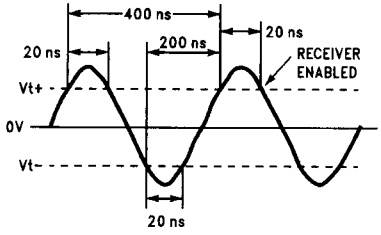
The multiplexer output is enabled by the CD/loopback control block. This block will enable data to the receiver's driver when receive squelch is turned off. (i.e., when valid data is present on RXI±). In addition, the RX± outputs have internal 5 kΩ pull-down resistors. These resistors eliminate the need for external pull downs when the TPI is located near the ENDEC.

The differential RX± line driver provides ECL compatible signals to the DTE with typically 3 ns rise and fall times. In its idle state, these outputs go to differential zero to prevent DC standing current in the isolation transformer.

Receive Squelch

The DP83922A implements an intelligent receive squelch intended to ensure external noise that appears on the receiver's inputs is not mistaken for a valid signal. This squelch uses a combination of amplitude and timing measurements to determine when to enable the receive circuitry. The operation of the squelch is as follows: An input signal must first exceed the input voltage threshold for typically 20 ns, and then typically within 150 ns later it must exceed the opposite input threshold for the same 20 ns duration. Finally the signal must exceed the original threshold within typically 150 ns after the last threshold detection time in order to turn off the receiver squelch and enable the receive circuitry. This is shown in the following illustration.

Squelch Timing for Receive Input



TL/F/10490–5

The voltage threshold level of the receive squelch is set by an external resistor, R_{RTH}. There are two levels, one level to enable the receiver (V_{Ron}), and a second smaller level to disable the receiver (V_{Roff}), providing hystersis. V_{Ron} is one third the voltage across the R_{RTH} resistor (V_{RTH}). V_{RTH} is given by:

$$V_{RTH} = \left(\frac{I_{TX(out)}}{48}\right) R_{RTH}$$

where $I_{TX(out)}$ is the total transmit current set by R_{TX} and R_{EQ} (see the description of the transmit function that follows). This equation can be rewritten in terms of R_{TX} and R_{EQ} as follows:

$$V_{RTH} = 1.245 \left(\frac{1}{R_{TX}} + \frac{1}{2R_{EQ}}\right) R_{RTH}.$$

V_{Roff} is equal to half of V_{Ron}. This adds hysterisis to the squelch circuit making it more reliable, especially in noisy environments.

Note that the receive threshold voltage is dependent on transmit output levels. It is therefore recommended to design the transmit section first, then choose the R_{RTH} resistor value.

TRANSMIT FUNCTION

Transmit Path

The transmitter has a differential input (TX±) and a differential open collector current driver (TXO±). From input to output the transmit path is fully differential and both TX+ and TX− are matched. This provides low signal skews and jitter. The differential input common mode voltage is established by the TPI and should not be altered by external circuitry. Either transformer or capacitive coupling of the TX± inputs will accomplish this. The general transmit waveform is shown below.

On the TX± inputs the transmitter squelch circuit rejects signals with pulse widths less than 20 ns typically, or with levels that are less than −175 mV. The transmitter turns off at the end of the packet if the signal stays higher than −175 mV for more than approximately 150 ns.

The transmitter differential outputs when coupled through a 2:1 pulse transformer can meet all the 10BASE-T output level specifications.

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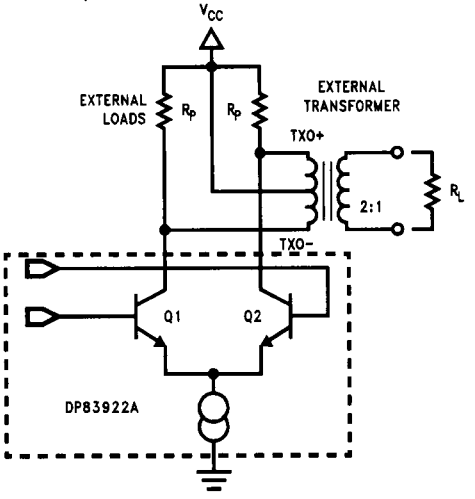
Functional Description (Continued)

Simplified Transmitter Differential Output



TL/F/10490–6

The transmitter differential outputs, when coupled through a 2:1 pulse transformer, can meet all the 10Base-T output levels specifications defined by IEEE.

As is shown in simplified form, the TXO± is a differential current mode output. This output integrates the equalization and wave shaping circuitry to pre-filter the output waveform. The driver level and equalization are externally programmable. Driver output current levels of the DP83922A are set by a built-in bandgap reference and two external resistors, R_{TX}, R_{EQ}. These two resistors set the output current for both the maximum and equalized portions of the output waveform. Controlled rise and fall times of the driver output circuits minimize the higher harmonic components, and therefore ease external filtering requirements. The rise and fall times are also matched to minimize jitter.

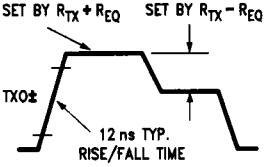
The relationship of the R_{TX} and R_{EQ} resistor values to the output current are:

$$I_{TX(out)} = \frac{59.76}{R_{TX}} + \frac{29.88}{R_{EQ}} \text{ mA}$$

$$I_{EQ(out)} = \frac{59.76}{R_{TX}} - \frac{29.88}{R_{EQ}} \text{ mA}$$

Note: Above resistor values are in kΩ.

TXO± Transmit Output Current Waveform



TL/F/10490–7

As can be seen above the transmit output will first go to an output current level set by the sum of the currents set by the R_{TX} and R_{EQ} resistor, and if the waveform is wider than 50 ns, the output current will drop to a value set by the difference between the currents set by R_{TX} and R_{EQ} resistors. Due to the tight IEEE output level specifications it is recommended to use 1% resistors for R_{TX} and R_{EQ}.

For each TXO output, the output current from the TXO± outputs will generate a voltage across R_P, the pulse transformer, and the twisted pair line impedance. The approximate equation for the single ended maximum output voltage output on the primary side (chip side) of the transformer is shown below:

(Note: The equations calculate the TPI's output voltage from the output pin to ground.)

$$V_{TXOUT} = \frac{I_{TX}}{2}\left(R_P \,||\, \frac{R'_L}{2}\right)$$

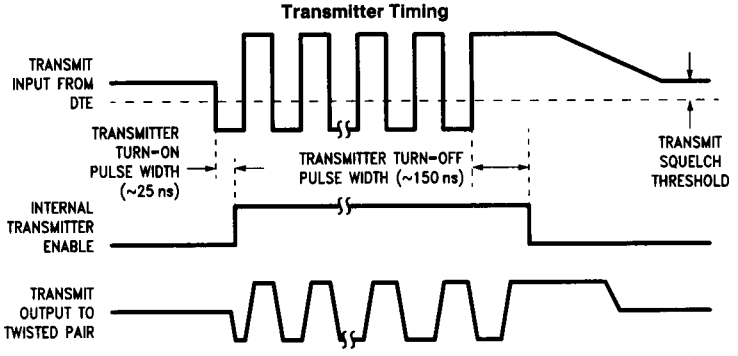
For the equalized single ended output voltage (the || operator is the parallel resistor combination):

$$V_{EQOUT} = \frac{I_{EQ}}{2}\left(R_P \,||\, \frac{R'_L}{2}\right)$$

Where R_P is the pullup resistor (typically 200Ω), and R'_L is the impedance of the twisted pair line as seen through the 2:1 transformer, $R'_L = 4\ R_L$ (typically 400Ω). For example if I_{TX} = 50 mA and I_{EQ} = 30 mA, then V_{TXOUT} peak is $\frac{50}{2}\left(100\Omega\right)$ = 2.5V and the V_{EQOUT} would be 1.5V.

An example of TXO outputs is shown on the following page. This diagram shows the typical TXO output waveform. This waveform is a 5V peak-to-peak signal centered at V_{CC}. The TXO+ and TXO− feed into the 2:1 transformer and filter, and result in the bottom waveform shown in the figure. The resultant output waveform is a ±2.5V differential typical signal per the IEEE standard.

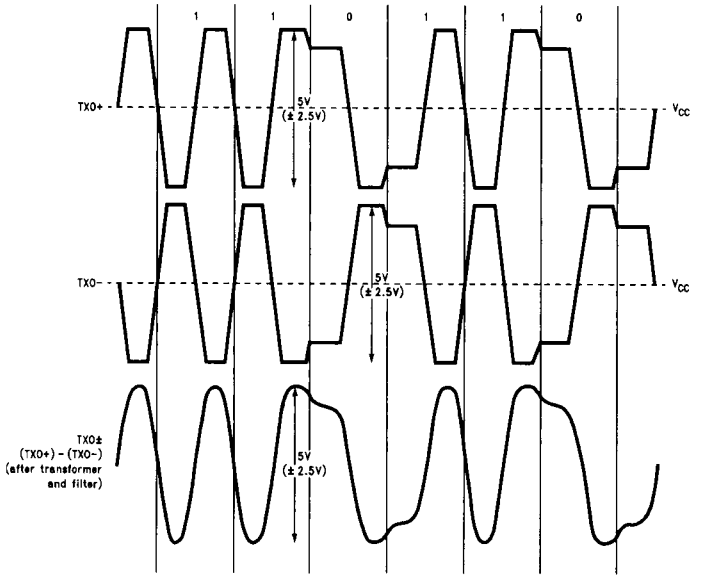
Transmitter Timing



TL/F/10490–8

Functional Description (Continued)

Typical Twisted Pair Transmit Output Waveforms



TL/F/10490–18

TOP: TXO+ Output voltage waveform measured relative to ground
MIDDLE: TXO− Output voltage waveform measured relative to ground
BOTTOM: Differential output voltage waveform on TXO+ to TXO−

COLLISION FUNCTION

The collision detection circuitry detects when the TX± inputs and the RXI± inputs are active simultaneously. This is done by logically ANDing the output of the transmit squelch and the receive squelch blocks. If both squelch indicate valid activity then the collision oscillator is enabled.

The collision circuits output a 10 MHz signal during a collision. The 10 MHz is generated by an internal oscillator. This oscillator is also used as a timebase for other internal functions.

HEARTBEAT FUNCTION

The collision circuits also generate the Heartbeat (SQE Test) signal at the end of every transmission to ensure that the collision circuitry is functioning. The burst of 10 MHz on the collision output occurs typically 1.1 μs after the transmission, and has a duration of about 1 μs. For repeaters this function can be disabled via the COL/HBE input.

JABBER TIMER FUNCTION

The Jabber Timer monitors the transmitter and inhibits the transmission if the Transmitter is active for longer than about 50 ms typical. It also enables the collision output for the fault duration. After the fault is removed, the Jabber Timer waits for about 500 ms typical (unjab time) before re-enabling the Transmitter. The transmit input must stay inactive during the unjab time.

LINK FUNCTION

The link integrity function consists of two parts, one part generates the link pulses, and the other detects the reception of link pulses. Both the transmission of the link pulse and then monitoring receptions of link pulses can be disabled by grounding the GDLNK pin.

Link Detector

The link detector circuitry is connected to the twisted pair receive circuits, and implements the IEEE 10BASE-T link state diagram. This block checks for the arrival of link pulses from the remote MAU, and if they arrive properly this logic keeps the transmit and receive functions enabled. If the link pulses fail to arrive then the link detector will disable the receive, transmit, collision, and heartbeat functions. When transmitting a packet the DTE is informed of the link failure by not receiving the loopback or the subsequent heartbeat signals from the TPI.

Link Generator

The link generator is a timer circuit that generates a link pulse by enabling the transmit output drivers. This 100 ns wide pulse will be generated if the transmitter is idle for 16 ms ±8 ms. The output of this circuit feeds into the TXO± driver circuit.

STATUS LED LOGIC

To ease the design of external LEDs that indicate to the end user various MAU status functions, the TPI includes 5 LED output drivers on-chip. These outputs are directly derived by the internal circuitry, and they indicate the following status information:

Reception: The RXLED output will go low whenever the receive (RXI±) squelch is disabled (receiver turned on).

Transmission: The TXLED output will go low (lighting the LED) whenever the AUI side transmit (TX±) squelch is disabled (transmitter turned on). The TXLED output will not go low during link pulse transmission or during a Jabber condition.

2

Functional Description (Continued)

Good Link: The GDLNK output will remain low while the Link state machine receives valid link pulses from the remote MAU. If the Link state logic does not properly receive link pulses, then the output will turn off the LED.

Collision: The HBE/COL output will turn on an LED if a collision is detected by the TPI (output goes low). This driver is directly driven by the output of the logical ANDing of the TX± and RXI± squelch.

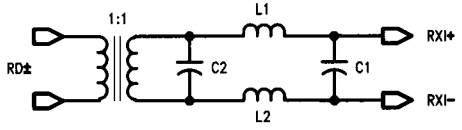
Jabber: The JBLED output is derived directly from the Jabber timer circuits. The output will go low (light the LED) whenever the TPI has determined that a Jabbering transmission is in progress, and will stay on until the transmit output is re-enabled.

All these LED outputs are driven directly by the internal circuits, and are not delayed or otherwise altered. This feature allows these outputs to be used logically if desired.

EXTERNAL RECEIVE AND TRANSMIT FILTER DESIGN CONSIDERATIONS

A requirement to interface to the twisted pair cabling is to provide adequate filtering on both the receive and transmit signal lines.

Three Pole Receive Butterworth Filter (100Ω)



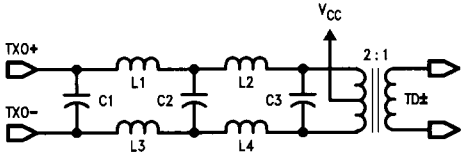
TL/F/10490–9

On the receive path, the 10BASE-T standard recommends a filter. A 3 pole Butterworth low pass filter yields acceptable high frequency rejection, for example a filter with the following characteristics may be used:

1. 3 dB Cut Off Frequency:	15 MHz
2. Insertion Loss (5 MHz–10 MHz)	≤ 1.0 dB
3. 30 MHz Attenuation:	17.5 dB min
4. I/O Impedance:	100Ω
5. Return Loss: (5 MHz–10 MHz)	≥20 dB

Additionally it may be desirable to add on the input to the pulse transformer a common mode choke to further filter out common mode noise.

Five Pole Transmit Butterworth Filter (400Ω)



TL/F/10490–10

On the transmit path there are numerous criteria for selection of the filter. To meet the general requirements a 5 pole Butterworth filter that can meet the following characteristics can be used:

1. 3 dB Cut Off Frequency	15 MHz
2. Insertion Loss: (5 MHz–10 MHz)	≤1.0 dB
3. 30 MHz Attenuation	27 dB Min
4. I/O Impedance	400Ω
5. Return Loss: (5 MHz–10 MHz) (Including Load Impedances)	≥20 dB

The Butterworth filter can be replaced by other filter types should the requirements demand it, but given the equalization-filtering the harmonic content of the TPI's transmit waveform, the filter requirements are reduced compared to pure digital implementations thus simplifying the design.

The transmit output is designed to drive an equivalent 400Ω impedance. This reduces the power/driver requirements of the transmitter, but also requires a 2:1 windings ratio on the transmit pulse transformer.

Integrated Filter Module Vendors

Several vendors are supplying filter, and transformer components that may be used with the DP83922A. The following companies provide products for use with the DP83922A.

Pulse Engineering
P.O. Box 12235
San Diego, California USA
92112
Phone: (619) 268-2400
Product: PE65423

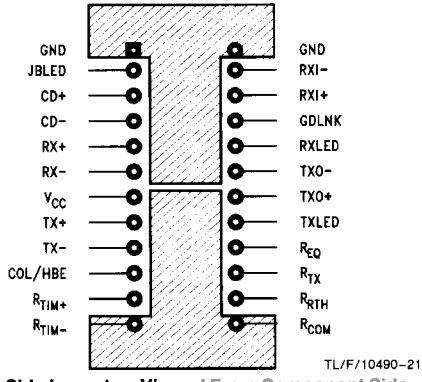
Belfuse
198 Van Vorst St.
Jersey City, NJ USA
07302
Phone: (201) 432-0463
Product: 0556-3899-00

Valor Electronics
6275 Nancy Ridge Dr.
San Diego, California USA
92121
Phone: (619) 458-1471
Product: PT3884

PCB LAYOUT CONSIDERATIONS

For heat dissipation purposes, it is recommended that a heat dissipation plane be added to the PCB layout of the TPI. The minimum required plane area should be 0.5 sq. in. This plane should be located on the solder side of the PCB, and can be most conveniently placed directly under the TPI package, between the pins as shown in the following figure. Alternately, the designer may add a heatsink to the top of the chip itself.

Ground Dissipation Trace

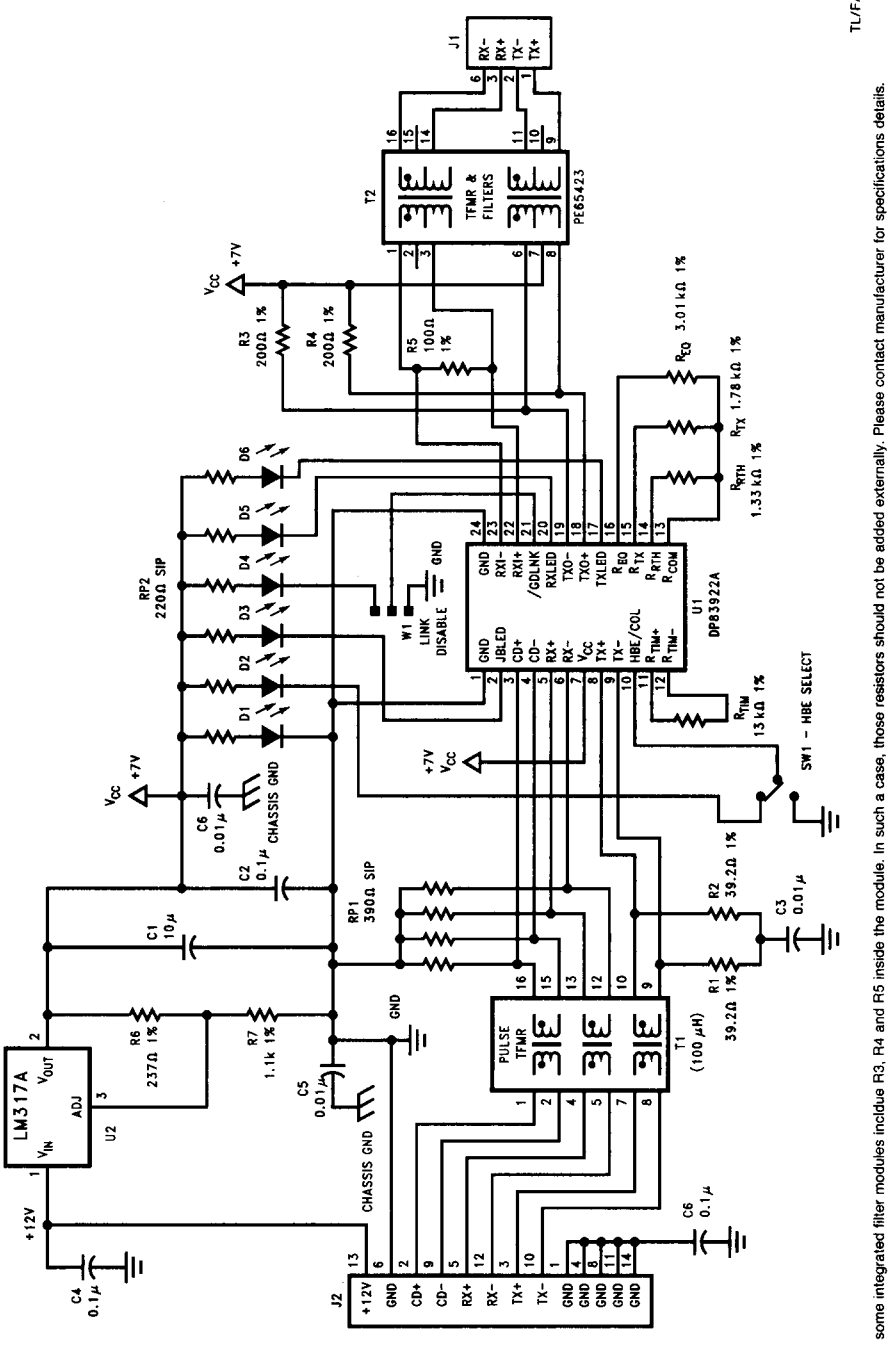


TL/F/10490–21

Solder Side Layout as Viewed From Component Side

Typical Application

Typical Medium Attachment Unit Application Using the DP83922A



TL/F/10490–11

Note: For T2, some integrated filter modules include R3, R4 and R5 inside the module. In such a case, those resistors should not be added externally. Please contact manufacturer for specifications details.

2

Absolute Maximum Ratings

(Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +9.0V
DC Input Voltage (V_{IN})	−0.5V to +9V
Storage Temperature (T_{STG})	−65°C to +165°C
Package Power Dissipation (P_D)	3.5W
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	6.65	7.35	V
Operating Temperature (T_A)	0	+70	°C
ESD Tolerance:	TBD		V
C_{ZAP} = 100 pF, R_{ZAP} = 1.5 kΩ (Note 3)			

PARAMETRICS DISCLAIMER

The current AC and DC specifications contained in this document are considered target design specifications and may not represent actual guaranteed tested timing parameters. This information represents simulated, as well as, limited sampled empirical "bench test" data. Guaranteed specifications will be provided after full device characterization.

Do not use these specifications for final production designs without directly contacting National Semiconductor.

Electrical Characteristics

V_{CC} = 7V ±5%, R_{TX} = 1.78 kΩ 0.1%, R_{EQ} = 3.01 kΩ 0.1%, R_{RTH} = 1.33k 0.1%, R_{TIM} = 13 kΩ 0.1%, T_A = 0°C − 70°C, unless otherwise specified (Note 4)

Symbol	Description	Conditions	Min	Max	Units
I_{CC}	Power Supply Current	RX± and CD± Open		200	mA
AUI					
V_{ROD1}	Differential Output Voltage (RX±, CD±)	Test *Figure 1*	±550	±1200	mV
V_{ROD2}	Differential Output Voltage (RX±, CD±)	Test *Figure 2*	±350		mV
V_{TS}	Transmitter Squelch Threshold (TX±)			−175	mV
TWISTED PAIR INTERFACE					
V_{Ron}	Receive Turn On Threshold (Note 5)		300	585	mV
r_{Roff}	Ratio of Receive Squelch Turn Off Threshold to Turn On Threshold $\left(\frac{V_{Roff}}{V_{Ron}}\right)$ (Note 5)		1.8	2.2	
V_{TOD}	Differential Output Voltage (TXO±) (Note 5)		±4.4	±5.6	V
RX_{IN}	Receiver Input Impedance		10		kΩ
LED OUTPUTS, HBE AND GDLNK INPUT					
V_{LOL}	LED Output Voltage	I_{OL} = 10 mA		2.4	V
V_{IL}	HBE, GDLNK Input Low Voltage			0.2	V
V_{IH}	HBE, GDLNK Input High Voltage		1.8		V

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

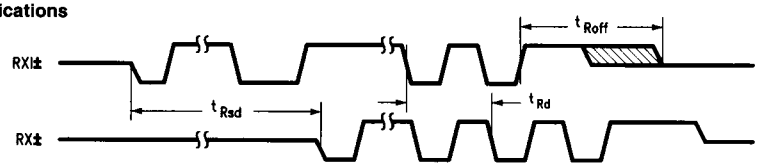
Note 3: Value based on test complying with NSC SOP 5-028 human body model ESD testing using the ETS-910 tester.

Note 4: These DC Electrical Characteristics are measured statically, and not under dynamic conditions. 0.1% resistors are used for test purposes. 1% resistors should be used in the end application.

Note 5: This specification is dependent on selection of R_{TX}, R_{EQ}, and R_{RTH} which have not been determined at this time. Typical values for these specifications can be derived from the design equations presented previously in this datasheet.

Switching Characteristics V_{CC} = 7V ±5%, T_A = 0°C to +70°C unless otherwise specified

Receiver Specifications

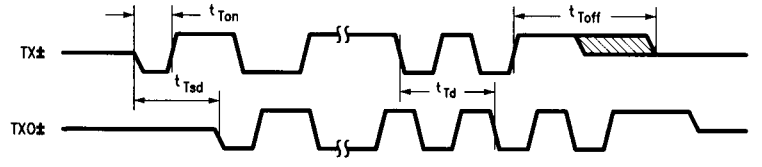


TL/F/10490–12

Symbol	Description	IEEE	Min	Max	Units
t_{Rsd}	Receiver Startup Delay (RXI ± to RX ±) (Note 6)	M1		800	ns
t_{Roff}	Receiver Turn Off Delay (RXI ± to RX ±)		130	250	ns
t_{Rd}	Receiver Propagation Delay (RXI ± to RX ±)	M1		200	ns
f_{RON}	Receiver Turn On Frequency (Squelch Disable)				MHz

Note 6: t_{Rsd} = (Propagation Delay) + (Invalid Bits) + (Bit Loss)

Transmitter Specifications

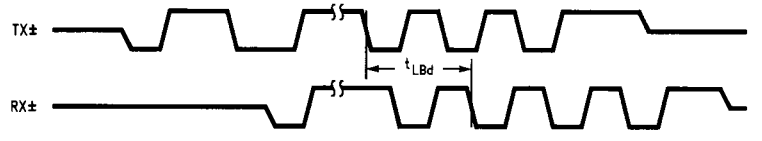


TL/F/10490–13

Symbol	Description	IEEE	Min	Max	Units
t_{Tsd}	Transmit Startup Delay (TX ± to TXO ±) (Note 7)	M2		500	ns
t_{Ton}	Transmit Turn On Pulse Width (TX ± to TXO ±)		5	40	ns
t_{Toff}	Transmit Turn Off Pulse Width (TX ± to TXO ±)		110	200	ns
t_{Td}	Transmitter Propagation Delay (TX ± to TXO ±)			200	ns

Note 7: t_{Tsd} = (Propagation Delay) + (Invalid Bits) + (Bit Loss)

Loopback Specifications

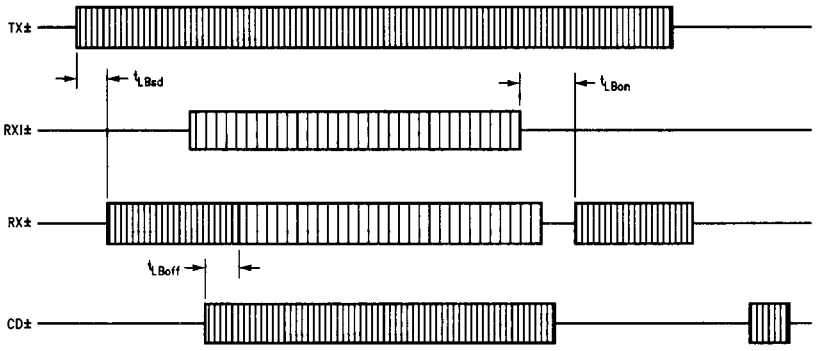


TL/F/10490–14

Symbol	Description	IEEE	Min	Max	Units
t_{LBd}	Loopback Propagation Delay (TX ± to RXI ±)			100	ns

2

Switching Characteristics V_{CC} = 7V ±5%, T_A = 0°C to +70°C unless otherwise specified (Continued)

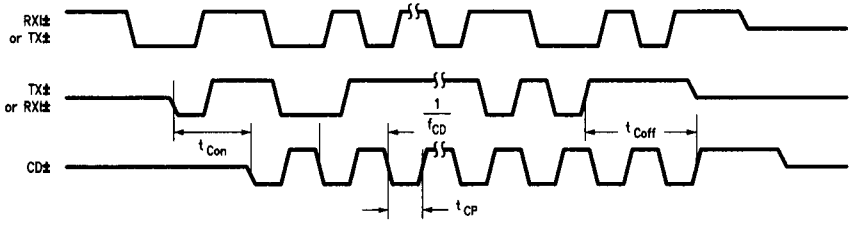


TL/F/10490–22

Symbol	Description	IEEE	Min	Max	Units
t_{LBsd}	Loopback Startup Delay (Start of TX± to start of RX±) (Note 8)	M9		700	ns
t_{LBoff}	Loopback Deassert (CD± to RX±)	M5		900	ns
t_{LBon}	Loopback Assert (TX± to RX±)	M6		900	ns

Note 8: t_{LBsd} = (Propagation Delay) + (Invalid Bits) + (Bit Loss)

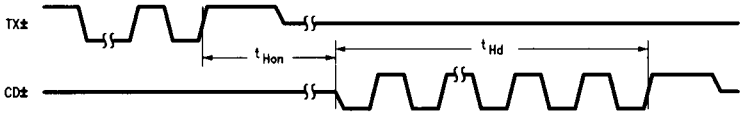
Collision Specifications



TL/F/10490–15

Symbol	Description	IEEE	Min	Max	Units
t_{Con}	Collision Turn On Delay	M3		900	ns
t_{Coff}	Collision Turn Off Delay	M4		900	ns
f_{CD}	Collision Frequency		8.5	12.5	MHz
t_{CP}	Collision Pulse Width		35	70	ns

Heartbeat Specifications

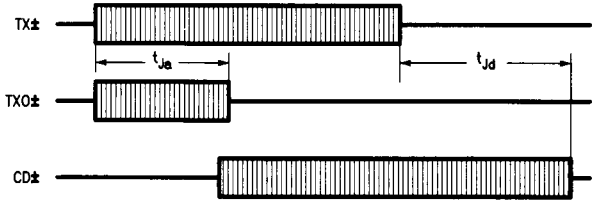


TL/F/10490–16

Symbol	Description	IEEE	Min	Max	Units
t_{Hon}	CD Heartbeat Delay (TX± to CD±)	M7	600	1600	ns
t_{Hd}	CD Heartbeat Duration (CD± to CD±)	M8	500	1500	ns

Switching Characteristics V_{CC} = 7V ±5%, T_A = 0°C to +70°C unless otherwise specified (Continued)

Jabber Specifications



TL/F/10490–17

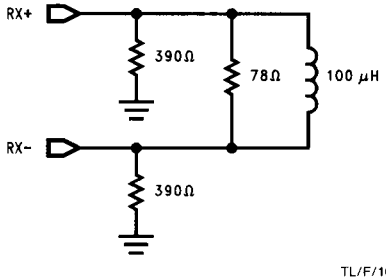
Symbol	Description	IEEE	Min	Max	Units
t_{Ja}	Jabber Activation Time (TX ± to TXO ± and CD ±)		20	150	ms
t_{Jd}	Jabber Deactivation Time (TX ± to TXO ± and CD ±)		0.25	0.75	S

Link Specifications

Symbol	Description	IEEE	Min	Max	Units
t_{LP}	Transmit Link Pulse Spacing		8	24	ms
t_{Lloss}	Received Link Pulse Loss Time		50	150	ms
t_{Lmax}	Received Link Maximum Time		25	150	ms
t_{Ltmin}	Received Link Minimum Time		2	7	ms
LC	Link Count		2	10	Pulses

Switching Specifications Test Loads

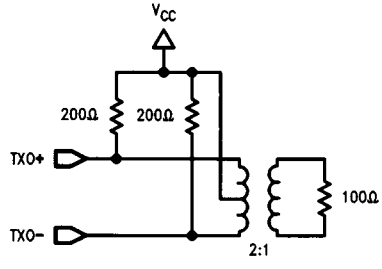
RX ± and CD ± Outputs Test Load



TL/F/10490–19

Test Figure 1

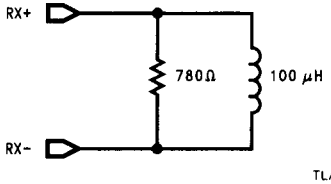
TXO ± Outputs Test Load



TL/F/10490–20

Test Figure 3

RX ± and CD ± Output Test Load



TL/F/10490–23

Test Figure 2