National Semiconductor Corporation

PRELIMINARY
April 1986

DP8470 Floppy Disk Support Chip Data Separator & Write Precompensation

General Description

This part is a general purpose data separator which can be used to generate a read clock for FM or MFM encoded data. This read clock can be used with many existing floppy disk controllers including the μPD765A, 8272A, and WD179x. It can also be used with National Semiconductor's Hard Disk Controller, DP8466, for a combination hard disk/floppy disk system. The data separator can be used for data rates ranging from 125 kbits/sec up to 1.25 Mbits/sec.

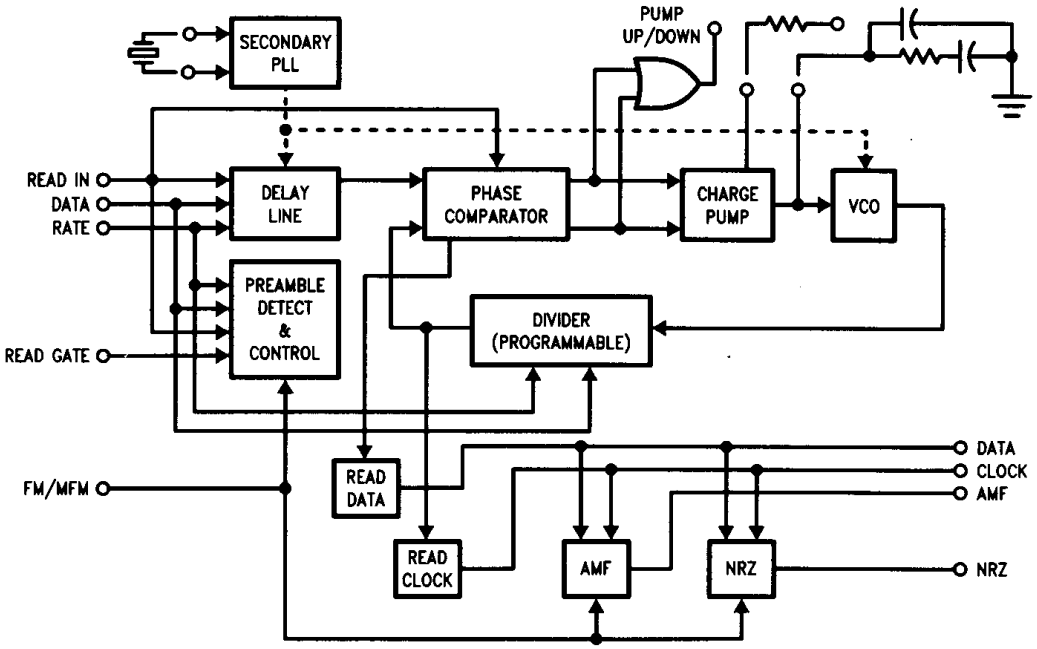
This part also contains a write precompensation circuit. Normally a disk controller will determine whether a bit of data needs to be shifted early, late, or not at all. The controller does not do the actual shifting however. This disk support chip will do the actual shifting that is requested by the controller.

A few other miscellaneous circuits have been included to enable this part to be interfaced to a hard disk controller such as the DP8466. The hard disk controller requires that the data read off from the disk be converted to an NRZ format rather than MFM encoded. Also, the controller needs to know when a valid address mark has been read from the data stream. This disk support chip does both of these functions.

Features

- Analog dual-gain PLL data separator
- Write precompensation (0–393 ns)
- Requires no external trimmable components
- Supports FM/MFM 125 kbits–1.25 Mbits/sec
- Interface to all popular floppy disk controllers.
- Interface to DP8466 hard disk controller
  - — Address Mark Found output
  - — NRZ output
- Pump up/down output for testing
- Low power CMOS
- 24-pin narrow package or 28-pin PCC

Block Diagram



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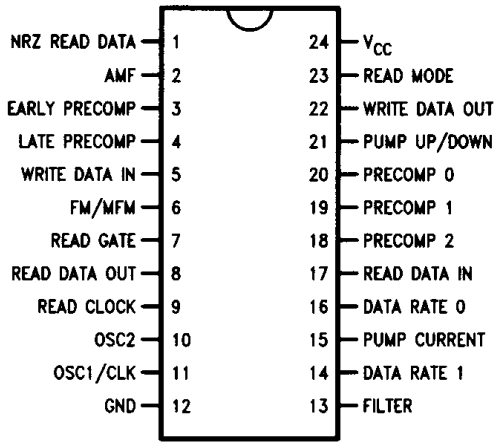
DP8470 Floppy Disk Support Chip Data Separator & Write Precompensation

Connection Diagram

Dual-In-Line Package



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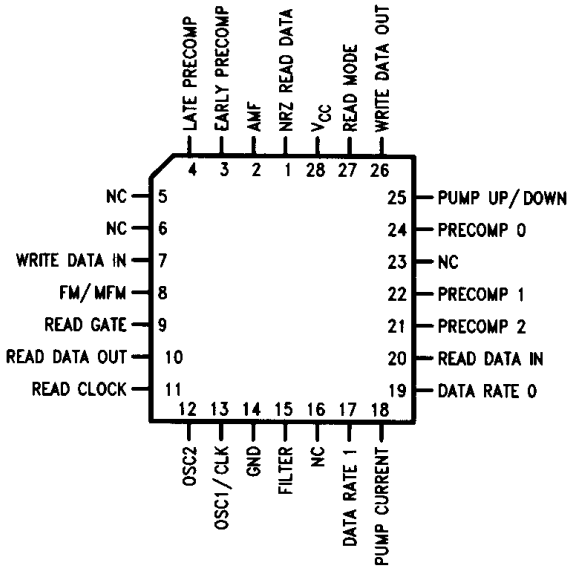
Top View

Plastic Chip Carrier



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Top View

Note: Make no corrections to NC pins (No connection).

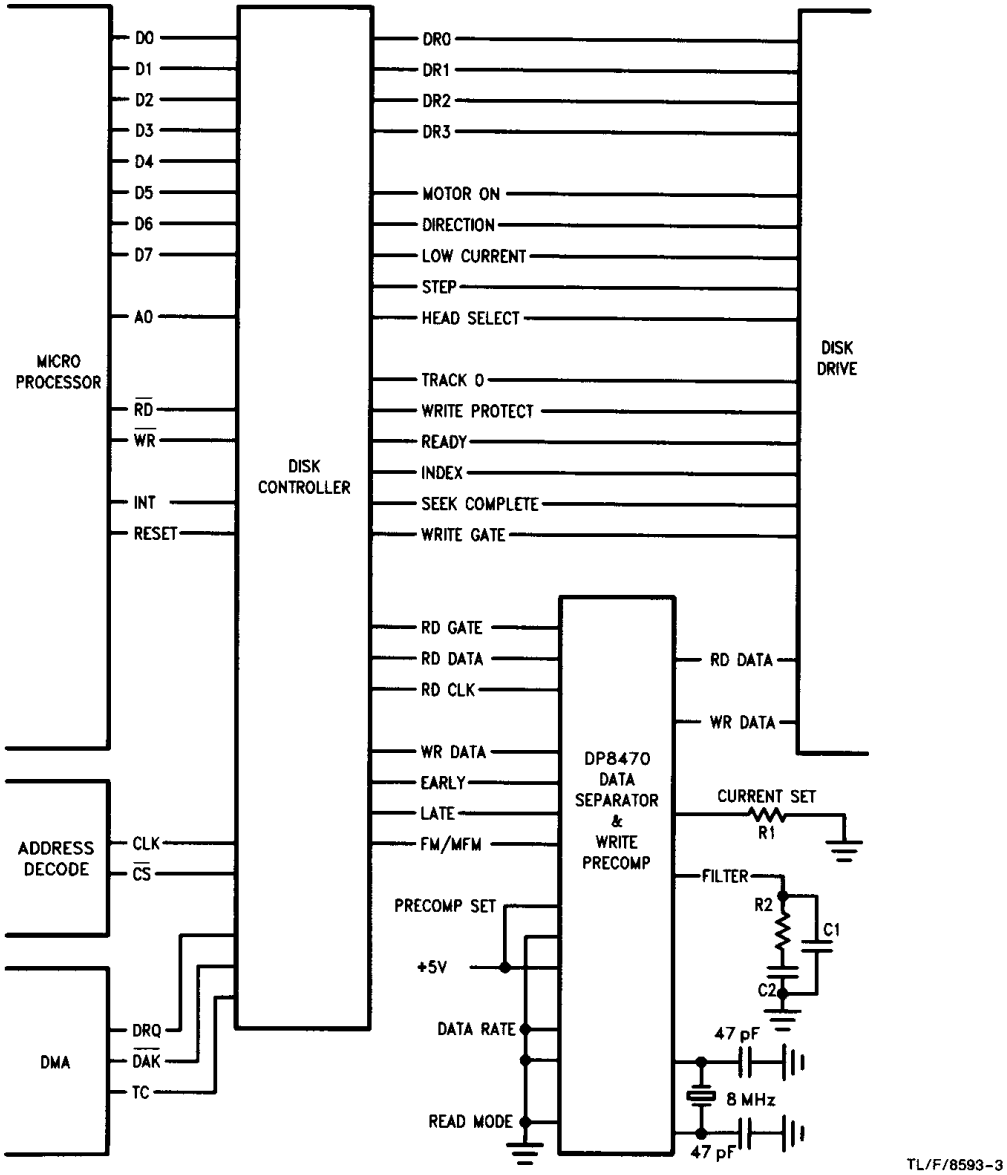
Pin Descriptions

Symbol	DIP Pin No.	PCC Pin No.	Function
NRZ READ DATA	1	1	This output will present data read from the disk in NRZ format based on the read clock. This output is set to a high impedance state when Read Gate is not asserted.
AMF	2	2	This output could be used with any controller that needs an indication of a valid address mark. This pin goes high for one bit period when an address mark is detected. This output is set to a high impedance state when Read Gate is not asserted.
EARLY/PRECOMP LATE/PRECOMP	3 4	3 4	These two active-high inputs determine whether the incoming write-data pulse should be shifted early or late in time.
WRITE DATA IN	5	7	Active-high data input from the disk controller.
FM/MFM	6	8	0 = FM, 1 = MFM. This pin also affects the data rate.
READ GATE	7	9	While this input is low, the PLL will lock to its center frequency. While this input is high, the PLL will lock to signal on the Read Data In pin.
READ DATA OUT	8	10	Active-high data output to the floppy controller. The Read Data Out is synchronized to the Read Clock Output.
READ CLOCK	9	11	This is a clock output that has the same frequency as the data rate. This output is always derived from the output of the VCO. While reading data, the VCO is tracking the data rate. When not reading data, the VCO is locked to its reference frequency.
OSC 1,2	10,11	12,13	These two pins enable the connection of a crystal to form the reference oscillator. Optionally an external clock can be used instead. The clock would drive Osc 1 while Osc 2 would be left open.
FILTER	13	15	This pin is the output of the dual-gain charge pump and is also the input to the VCO. A simple filter is attached to this pin.
DATA RATE 0 DATA RATE 1	16 14	19 17	These two pins select the data rate that this chip will sync to: 00 = 125FM/250MFM 01 = 250FM/500MFM 10 = 500FM/1000MFM 11 = Test Mode
PUMP CURRENT	15	18	A resistor is attached to this pin to set the charge pump current.

Pin Descriptions (Continued)

Symbol	DIP Pin No.	PCC Pin No.	Function
READ DATA IN	17	20	Active-high data input from the disk drive.
PRECOMP 0 PRECOMP 1 PRECOMP 2	20 19 18	24 22 21	These three input pins select the amount of write precompensation.
PUMP UP/DOWN	21	25	This active-high output is the logical OR of Pump Up and Pump Down. This is used for diagnostic purposes.
WRITE DATA OUT	22	26	Active-high data output to the floppy drive. This is the same data as is input on the Write Data In pin, except it has been write-precompensated and delayed.
READ MODE	23	27	This input determines what read algorithm is used to select between the low and the high gain mode. (Low = 4-state algorithm, high = 2-state algorithm.)
V_{CC} GROUND	24 12	28 14	These pins are the power supply pins for both the digital circuitry and the analog circuitry.

Typical Floppy Disk Drive Application



Functional Description

The data separator consists of a dual gain analog PLL (Phase Locked Loop). This PLL synchronizes a VCO (Voltage Controlled Oscillator) to the raw data signal read from a disk drive. The Read Clock pin is derived from the VCO. The Read Data Out pin mirrors the Read Data In pin except that it is centered with respect to the Read Clock. In addition, NRZ encoded data is available at the Read Clock. In addition, NRZ encoded data is available at the NRZ Read Data pin.

The PLL consists of three main components, a phase comparator, a filter, and a voltage controlled oscillator (VCO), as shown in the Block Diagram. The basic operation of a PLL is fairly straightforward. The phase comparator detects the difference between the phase of the VCO output and the phase of the raw data being read from the disk. This phase difference is converted to a current which either charges or discharges a filter. The resulting voltage of the filter changes the frequency of the VCO in an attempt to reduce the phase difference between the two signals. A PLL is "locked" when the frequency of the VCO is exactly the same as the average frequency of the read data. This is somewhat of a simplified view because it ignores such topics as loop stability, acquisition time, and filter values.

The external filter simply consists of two capacitors and a resistor as shown in the typical application diagram. Another resistor is used to set the charge pump current.

The quarter period delay line is used to determine the center of a bit cell. It is important that this delay line be as accurate as possible. A typical data separator would normally require an external trim to adjust the delay. An external trim is not required for the DP8472/74 however. A secondary PLL is used to automatically calibrate the delay line. The secondary PLL also calibrates the center frequency of the VCO.

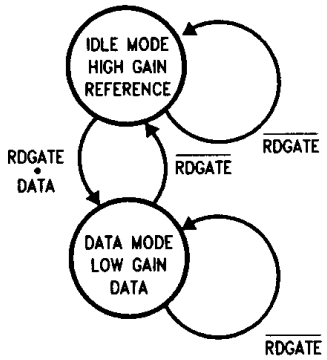
The Preamble Detect circuit is used with the four-state algorithm to determine when the PLL switches from the high gain mode to its low gain mode. This circuit scans the incoming data for the frequency corresponding to a preamble plus or minus 15 percent.

Circuit Operation

READ MODE

There are two read modes to choose from. The Read Mode is selected with the Read Mode pin. The state of this pin should not change during an actual read operation.

Two-State Diagram



Data = first incoming pulse received. TL/F/8593–4

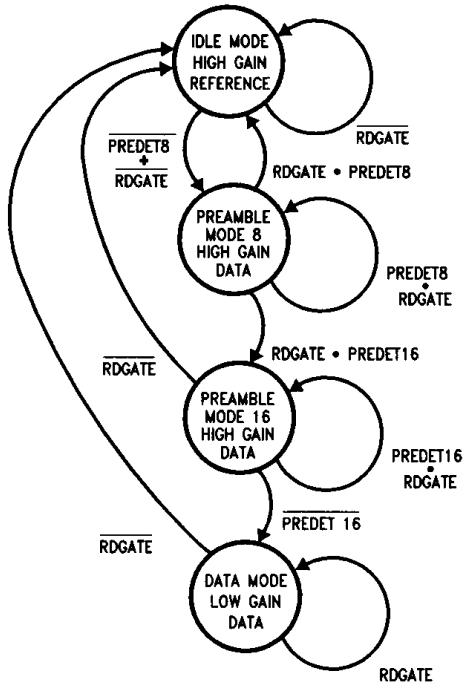
MODE ONE (TWO-STATE DIAGRAM)

When Read Gate is not asserted, the PLL is locked to the crystal frequency in its high-gain mode with a phase/frequency comparator. When Read Gate is asserted, the PLL will remain locked to the crystal until the first data bit arrives.

It will then lock to the incoming data in its low-gain mode with a phase-only comparator. It will stay in this mode until Read Gate is deasserted.

The NRZ Data Output will remain low until 8 bits have been read. This is to guarantee that the clock pulses from the preamble have become stable. The Read Data Out is enabled as soon as the first data bit arrives.

Four-State Diagram



PreDet8 = 8 consecutive bits of preamble frequency. TL/F/8593–5
PreDet16 = 16 consecutive bits of preamble frequency.

MODE TWO (FOUR-STATE DIAGRAM)

When Read Gate is not asserted, the PLL is locked to the crystal frequency in its high-gain mode with a phase/frequency comparator. When Read Gate is asserted, a preamble-detect circuit is enabled. This circuit looks for consecutive bits of the correct preamble frequency. The PLL will stay locked to the crystal frequency until 8 consecutive preamble bits are read. At this point the PLL will lock on to the incoming data (preamble) in its high-gain mode with a phase-only comparator. When the preamble-detect circuit finds 16 consecutive bits of the preamble frequency, the Data Output and the NRZ Data Output logic will be enabled. If at any time before the 16 bits are counted the preamble-detect circuit goes false, the PLL will return to the Idle Mode locked to the crystal. As soon as the preamble-detect circuit goes false after the 16 bits are counted (such as when beginning of the address mark is read) the PLL will switch to its low-gain mode. It will stay in this mode until Read Gate is deasserted. The timing is such that the comparison of the first bit of the Address Mark is done in the low-gain mode.

Between the time in which Read Gate is asserted and the Read Data Output is enabled (states 1 and 2 of the 4-state diagram), the data pattern 4E(hex) or FF(hex) will be output

Circuit Operation (Continued)

for MFM and FM respectively on the Read Data Output pin. The NRZ Data Output will remain low during this time.

WRITE MODE

When writing data, the rising edge of the signal presented to the Write Data Input is delayed before it appears on the Write Data Output. The number of delays is shown in Table I.

The actual value of the delay is determined by the PreComp Set pins. There is also a base delay as specified in the AC timing characteristics.

TABLE I

Early	Late	# of Delays
0	0	1
0	1	2
1	0	0
1	1	illegal

Design Considerations

The operating characteristics of this part are totally pin programmable. The designer needs to set three parameters by tying pins either high or low. These three parameters are the data rate, the amount of write precompensation, and the read mode algorithm.

DATA RATE, FM/MFM

The data rate is determined by three pins (Data Rate 0, Data Rate 1, FM/MFM) and also the clock frequency. The normal clock frequency is 8 MHz. The selectable data rates based on an 8 MHz clock are shown in Table II. If a data rate is needed that is not shown in the 8 MHz column, it may be produced by varying the clock frequency. See the AC Electrical Characteristics for the acceptable range of clock frequencies.

If either of these parameters (data rate or FM/MFM) are subject to change then these pins could be connected to switches, an output port, or through some logic from the controller's drive select output.

TABLE II

Data 1	Rate 0	FM/ MFM	Actual Data Rate (f = 8 MHz)	Actual Data Rate (Variable f)
0	0	0	125 kbits/sec	f/64
0	0	1	250 kbits/sec	f/32
0	1	0	250 kbits/sec	f/32
0	1	1	500 kbits/sec	f/16
1	0	0	500 kbits/sec	f/16
1	0	1	1.00 Mbits/sec	f/8
1	1	0	test mode	
1	1	1	test mode	

f = clock frequency.

The test mode is used by National for testing purposes. It should not normally be used for anything else.

WRITE PRECOMPENSATION

Another parameter to set is the amount of write precompensation needed for the disk drive being used. This value is generally specified by the drive manufacturer. The amount of precompensation used is based on the Precomp Set pins and the Data Rate as shown in Table III.

If the amount of write precompensation is subject to change, then these pins could be connected to switches, an output port, or through some logic from the controller's drive select output.

It is sometimes desirable to enable write precompensation for the inner tracks of a disk only. Some controllers have an output signal that indicates when the head is over a track that needs write precompensation. The easiest way to implement this signal is to choose the amount of write precompensation needed, look up in the table which pins need to be tied high and which need to be tied low. Connect the low pins to ground. Connect the high pins to the controller's write precompensation enable output pin.

CRYSTAL

Normally an 8 MHz crystal is attached in parallel across the two oscillator pins. There should also be a separate 47 pF capacitor attached to each pin with the other side of each capacitor attached to ground. If the system already has an 8 MHz source, this may be used to drive the Osc 1 pin while leaving the Osc 2 pin floating. The frequency at this pin is used to set the center frequency of the VCO and the initial delay of the quarter period delay line. It is also used for the write precompensation circuit timing. See the AC Electrical Characteristics for the acceptable range of the crystal. Varying the frequency will affect many operating parameters as specified in the appropriate sections.

FILTER

The filter is used for the main PLL. The values recommended for the two resistors and the capacitor are given in Table IV based on the data rate needed. If more than one data rate will be used, there are two alternatives. The values can be used that are shown in the table for the multiple data rates. These values are a trade off of PLL characteristics that are not ideal for either data rate. Another alternative is to actually have two separate filters with the capability of switching in one or the other either with a manual switch or an analog switch which can be software controlled.

TABLE III

Precomp Set			Amount of Precompensation					
2	1	0	Data Rt = 00		Data Rt = 01		Data Rt = 10	
			f = 8 MHz	Variable f	f = 8 MHz	Variable f	f = 8 MHz	Variable f
0	0	0	0 ns	0X	0 ns	0X	0 ns	0X
0	0	1	107 ns	3X	36 ns	1X	36 ns	1X
0	1	0	143 ns	4X	71 ns	2X	71 ns	2X
0	1	1	179 ns	5X	107 ns	3X	107 ns	3X
1	0	0	214 ns	6X	143 ns	4X	143 ns	4X
1	0	1	250 ns	7X	179 ns	5X	179 ns	5X
1	1	0	321 ns	9X	214 ns	6X	illegal	
1	1	1	393 ns	11X	250 ns	7X	illegal	

X = 2/7f ns, where f = clock frequency.

TABLE IV

Data Rate	R1	R2	C1	C2
125 kbits/sec FM	kΩ	Ω	nF	μF
250 kbits/sec FM	kΩ	Ω	nF	μF
500 kbits/sec FM	kΩ	Ω	nF	μF
250 kbits/sec MFM	10.0 kΩ	100 Ω	4.7 nF	0.047 μF
500 kbits/sec MFM	kΩ	Ω	nF	μF
1 Mbit/sec MFM	kΩ	Ω	nF	μF
1.25 Mbits/sec MFM	kΩ	Ω	nF	μF
125 FM/250 MFM kbits/sec	kΩ	Ω	nF	μF
250 FM/500 MFM kbits/sec	kΩ	Ω	nF	μF
500 FM/1000 MFM kbits/sec	kΩ	Ω	nF	μF

Interfacing

DISK DRIVE INTERFACE

The connection between the Support Chip and the Disk Drive is very simple. The disk drive's Write Data line connects to the support chip's Write Data Out pin. The disk drive's Read Data line connects to the support chip's Read Data In pin.

FLOPPY CONTROLLER

Simply connect the Write Data and Read Data pins of the controller to the Write Data In and Read Data Out pins of the Support Chip. Connect the Early and Late Precomp outputs from the controller to the Early and Late Precomp inputs of the disk support chip.

The Read Gate input pin of the disk support chip must be connected to the pin of the controller that indicates when the controller is trying to read valid data. On the μPD765A, 8272A this is the VCO pin. On the WD179x this is the VFOE pin.

The Read Clock output pin of the disk support chip must be connected to the pin of the controller that requires a data window (or data clock). This is a window that defines whether an MFM encoded pulse is a data pulse or a clock pulse. The polarity of this pulse is indeterminant. On the μPD765A, 8272A this is the DW pin. On the WD179x this is the RCLK pin.

HARD DISK CONTROLLER

This floppy support chip has been designed to interface directly to the DP8466 Hard Disk Controller. Connect the Write Data lines exactly the same way as for the floppy controller. Connect the Write Precomp lines the same way also.

The hard disk's Read Data line should be connected to the support chip's Read Data In pin. Also, the controller's Read Gate output is connected to the Read Gate input of the support chip. The controller does not use the support chip's Read Data Out pin. The controller needs the data read from the disk to be in NRZ format rather than MFM encoded format. Simply connect the NRZ Read Data pin of the support chip to the Read Data pin of the controller. Connect the Read Clock output of the support chip to the Read Clock input of the controller.

The Address Mark Found output of the support chip gets connected to the Address Mark Found input of the controller.

Note: If write precompensation is used as well as AMF with the DP8466, the signal to indicate early precomp and the signal to indicate AMF must be multiplexed by the Write Gate output of the controller since the DP8466 combines these two functions on the same pin.

PLL Performance

The information in this section is not needed to use this part. It is included for completeness. The performance of the PLL is determined from the following factors:

K_{VCO} — Change in the frequency of the VCO due to a voltage change at the VCO input.

$$K_{VCO} \approx 10 \text{ MRad/s/volt.}$$

I_{CP} — Charge pump current. Set by the external resistor R_1 across the reference voltage set by the chip. $I_{CP} = 1.2 \text{ V}/R_1$. This current can be set anywhere between 50 μA and 350 μA. While in the high gain mode, the current is doubled.

C_2 — Filter capacitor.

R_2 — Filter resistor. Determines the PLL damping factor.

C_1 — This filter capacitor improves the performance of the PLL although it has only a secondary effect.

Using second order PLL formulas (i.e. ignoring the effect of C_1) the filter components can be chosen to obtain the required performance.

The bit jitter tolerance of the PLL is given by,

$$\omega_n = (K_{VCO}/2N \times I_{CP}/2\pi \times 1/C_2)^{1/2}$$

where N is the number of VCO cycles between two phase comparisons (N = 2 during the preamble).

The acquisition time (time to lock to the correct phase and frequency) is given by,

$$t_{lk} \approx 6/\omega_n.$$

The trade off, when choosing filter components, is between acquisition time while the PLL is locking and jitter immunity while reading data.

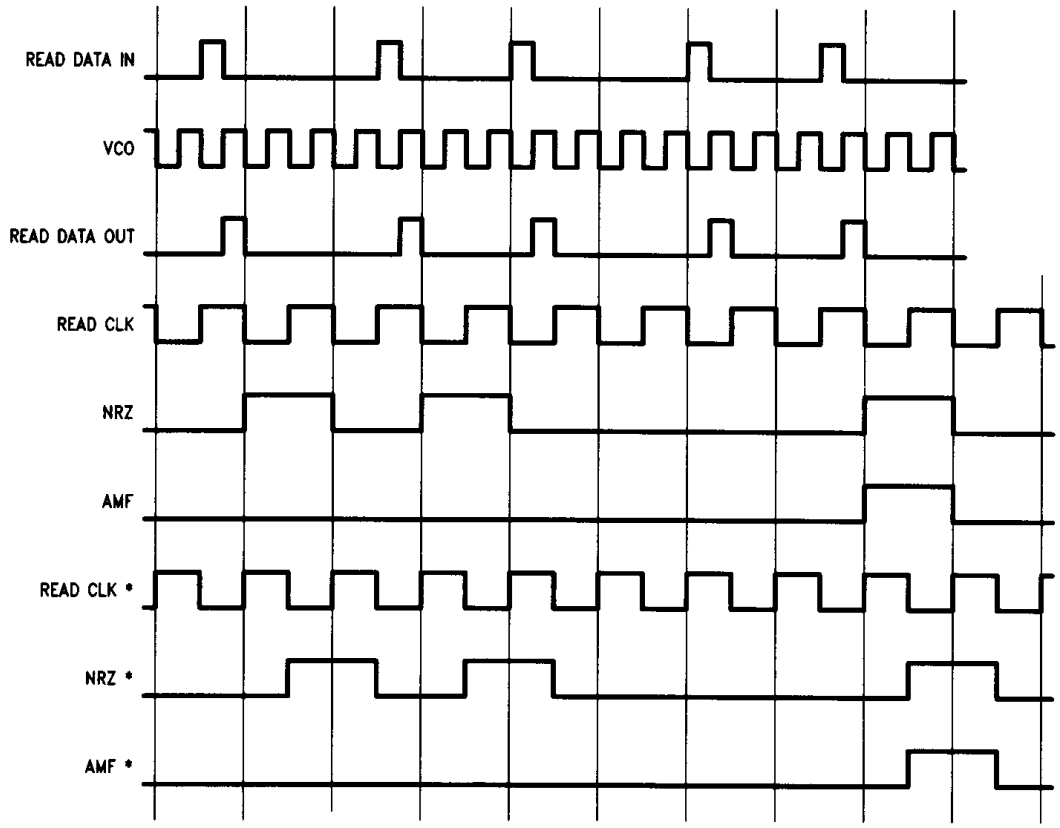
The damping factor is given by,

$$\zeta = \omega_n \times (R_2 \times C_2)/2$$

and is usually set at about 0.7.

Functional Waveform

Read Data Timing



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* = If Read Clock starts out of phase.

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current	±20 mA

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage	0	V_{CC}	V
Operating Temperature Range (T_A):	0	+70	°C

DC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 0°C to +70°C Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0	V
V_{IL}	Maximum Low Level Input Voltage		0.8	V
V_{OH}	Minimum High Level Out	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 2 mA	3.7	V
V_{OL}	Maximum Low Level Out	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 2 mA	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	±1.0	μA
I_{OZ}	Maximum TRI-STATE® Leakage Current	V_{OUT} = V_{CC} or GND	±10.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND F_{IN} = 8 MHz	3.0	mA
I_{CC}	Maximum Supply Current	V_{IN} = 2.4V or 0.5V F_{IN} = 8 Mhz	20.0	mA

AC Electrical Characteristics V_{CC} = 5V ±10%, C = 150 pF, unless otherwise specified

Symbol	Parameter	T_A = 0°C to 70°C				Units
		f = 8 MHz		f = variable		
		Min	Max	Min	Max	
f	Crystal Frequency	4	10			MHz
DR	Data Rate	125	1250			Kbit/s
READ TIMING						
t_{DRS}	Data Rate Setup to Data In	Depends on Filter Used				
t_{RMS}	Read Mode Setup to Read Gate	100				ns
t_{FMS}	FM/MFM Setup to Data In	Depends on Filter Used				
t_{RGS}	Read Gate Setup to Data In	600		$100 + \frac{4\times10^9}{f}$		ns
t_{DRH}	Data Rate Hold from Read Gate	2 Bit Windows				
t_{RMH}	Read Mode Hold from Read Gate	2 Bit Windows				

AC Electrical Characteristics V_{CC} = 5V ±10%, C = 150 pF, unless otherwise specified (Continued)

Symbol	Parameter	T_A = 0°C to 70°C				Units
		f = 8 MHz		f = variable		
		Min	Max	Min	Max	
READ TIMING (Continued)						
t_{FMH}	FM/MFM Hold from Read Gate	2 Bit Windows				
t_{RGH}	Last Data In to Read Gate Disable	2 Bit Windows				
t_{RGF}	Read Gate Off Time between Reads	600				ns
t_{RDO}	Read Data Offset from Center of Read Clock		34			ns
t_{NRZ}	NRZ & AMF Data Offset from Read Clock Edge		20			ns
t_{IN}	Pulse Width of Data In	50				ns
t_{OUT}	Pulse Width of Data Out	110	200	$\frac{8.8\times10^8}{f}$	$\frac{1.6\times10^9}{f}$	ns
WRITE TIMING						
t_{DRWS}	Data Rate Setup to Write Data In	125				ns
t_{PSS}	Precomp. Setup to Write Data In	125				ns
t_{RGS}	Read Gate Setup to Write Data In	600		$100 + \frac{4\times10^9}{f}$		ns
t_{PS}	Early/Late Setup to Write Data In	−160 (Note 1)				ns
t_{PH}	Early/Late Hold from Write Data In	200				ns
t_{DRWH}	Data Rate Hold from Write Data In	1.0				µs
t_{PSH}	Precomp. Hold from Write Data In	1.0				µs
t_{RGH}	Read Gate Hold from Write Data In	1.0				µs
t_{WI}	Write In Pulse Width	20				ns
t_{WO}	Write Out Pulse Width	220	350	$\frac{1.76\times10^9}{f}$	$\frac{2.8\times10^9}{f}$	ns
t_{IO}	Write In to Write Out	280 Typ. (Early Precomp.)		$30 + \frac{2\times10^9}{f}$		ns
e_{WP}	Error of Write Precomp.		±10			%

Note 1: The Early and Late pins do not need to be valid until 160 ns after the rising edge of the write data in signal. This is to accommodate interfacing to the µPD765A.

PLL Characteristics

Symbol	Parameter	Value	
$K_{\phi High}$	Phase Comparator & Charge Pump Gain Constant. High Gain Mode. (Note 1)	$\frac{5\ V_{REF}}{2\pi R}$	Typ.
V_{REF}	Voltage at Set Pump Current Pin	1.2V	Typ.
$K_{\phi Low}$	Low Gain Mode (Note 1)	$\frac{2.5\ V_{REF}}{2\pi R}$	Typ.
K_{VCO}	Gain of VCO (Note 2)	5/N MRad/S/V	Typ.
f_{VCO}	Center Frequency of VCO	f/2	Typ.
t_{JITTER}	Maximum Tolerance of Bit Jitter (Note 3)	$\frac{(0.95)}{4 \times DR}$	Typ.
$t_{POWER\ ON}$	Time from Full V_{CC} Power to Guaranteed Functionality	50 ms	Max

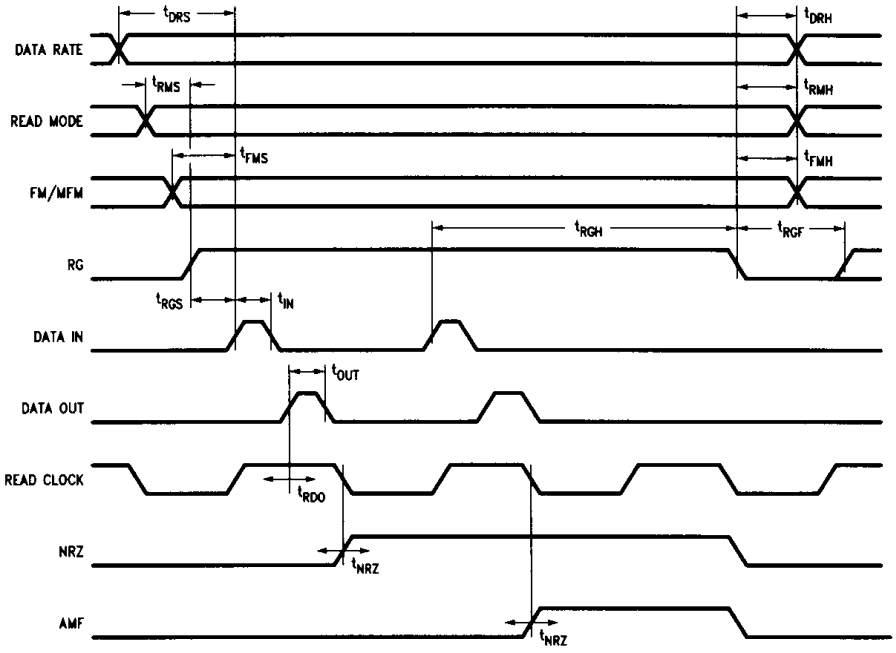
Note 1: R = pump current set resistor (8k–20k).

Note 2: N = # of VCO cycles per bit.

Note 3: DR = Data Rate.

Timing Diagrams

Read Timing



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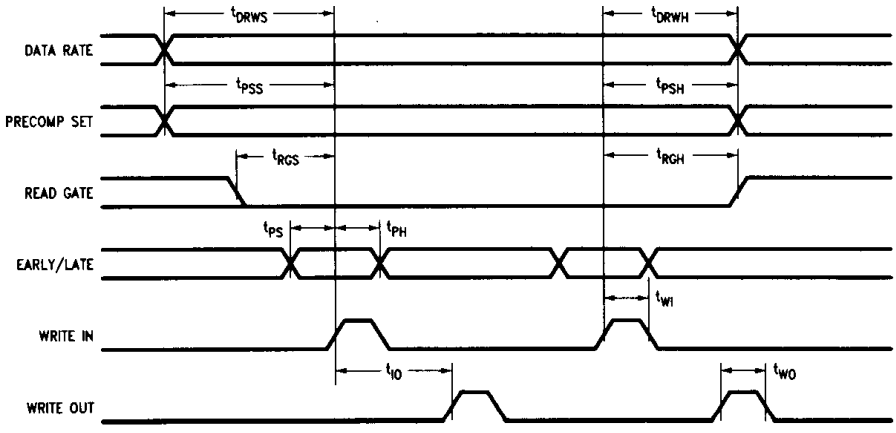
Write Timing



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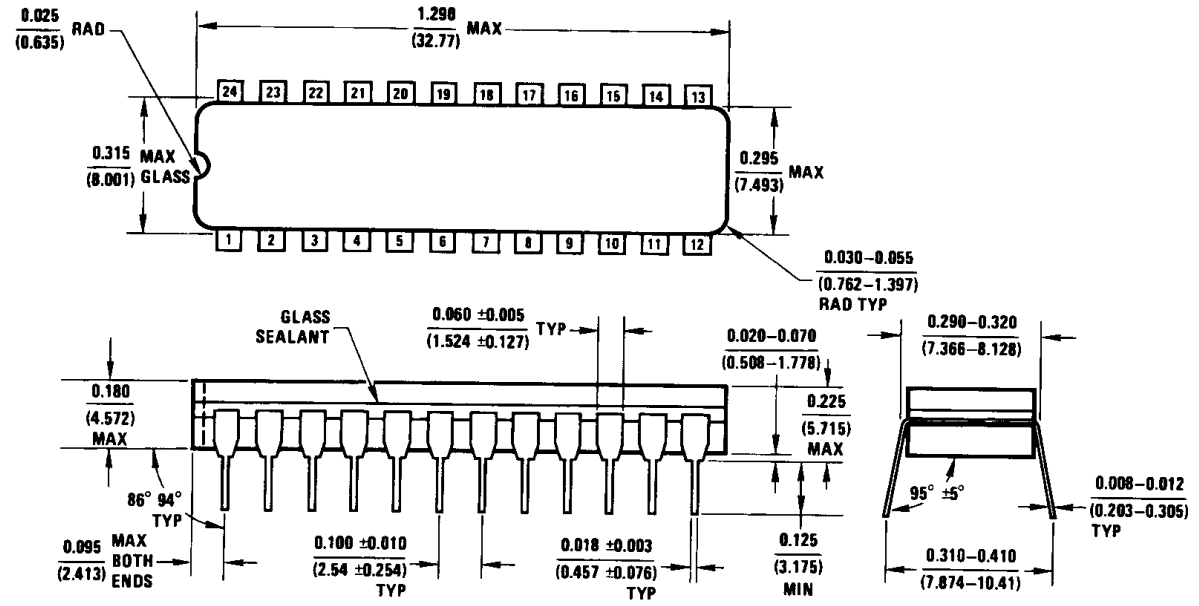
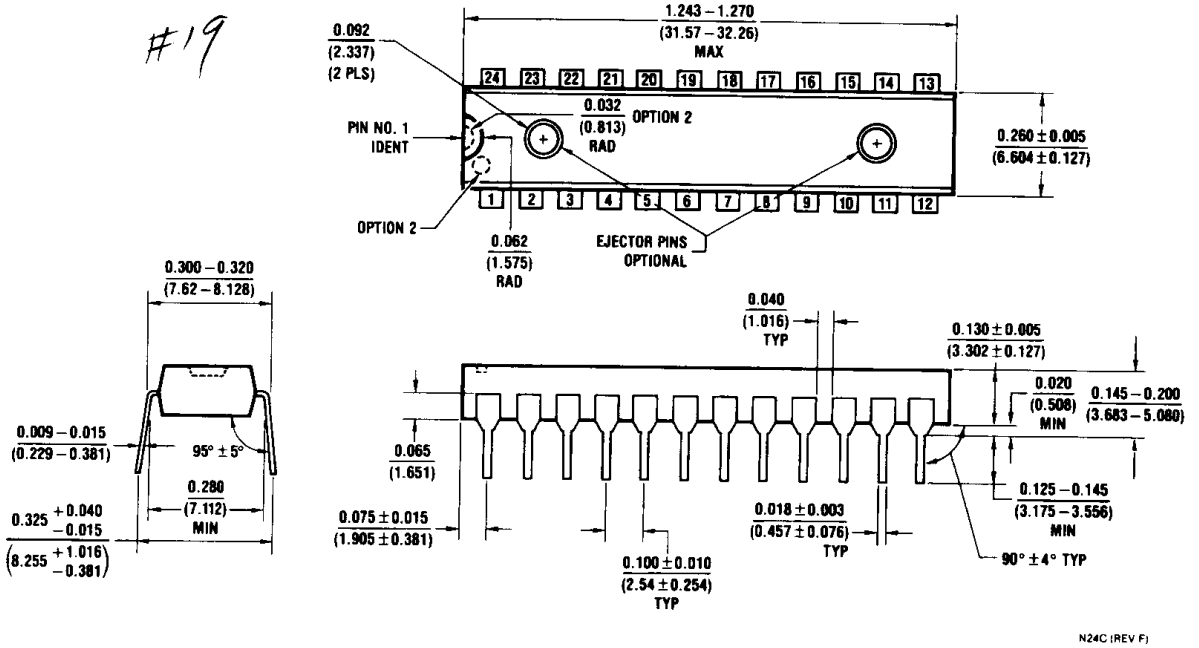
Physical Dimensions inches (millimeters)

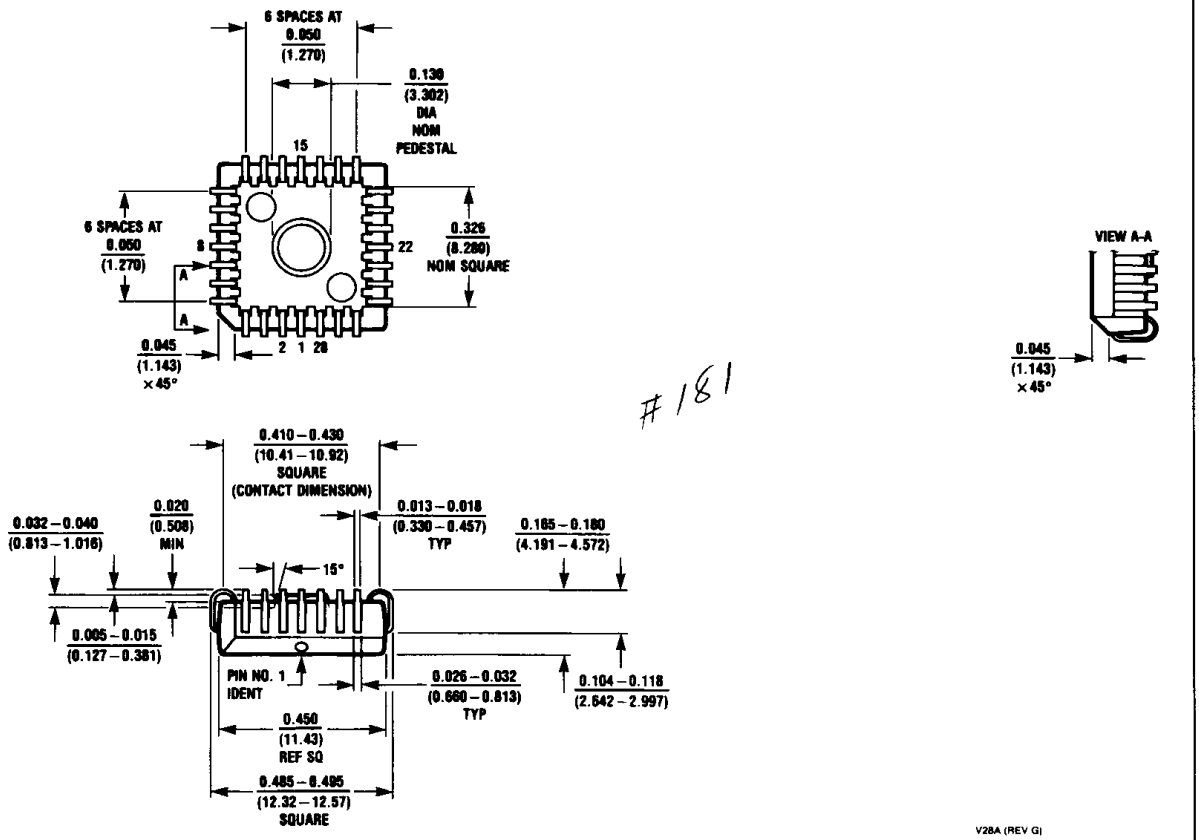


Molded Dual-In-Line Package (J)
Order Number DP8470J
NS Package Number J24F



Dual-In-Line Package (N)
Order Number DP8470N
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier (V)
Order Number DP8470V
NS Package Number V28A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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