

# DPC2020R/DPC2021R

## Thin-Film or MIG Head Read/Write Preamplifier

### General Description

The DPC2020R/DPC2021R are high performance, four channel, low power, read preamplifier/write current driver circuits designed for two-terminal recording heads. Power supply fault protection is included to disable the write current generator whenever the supply voltage is below 4V. When in the idle mode, the device conserves power to a level of 3 mW (typically). Switched resistors across the heads provide damping in the write mode.

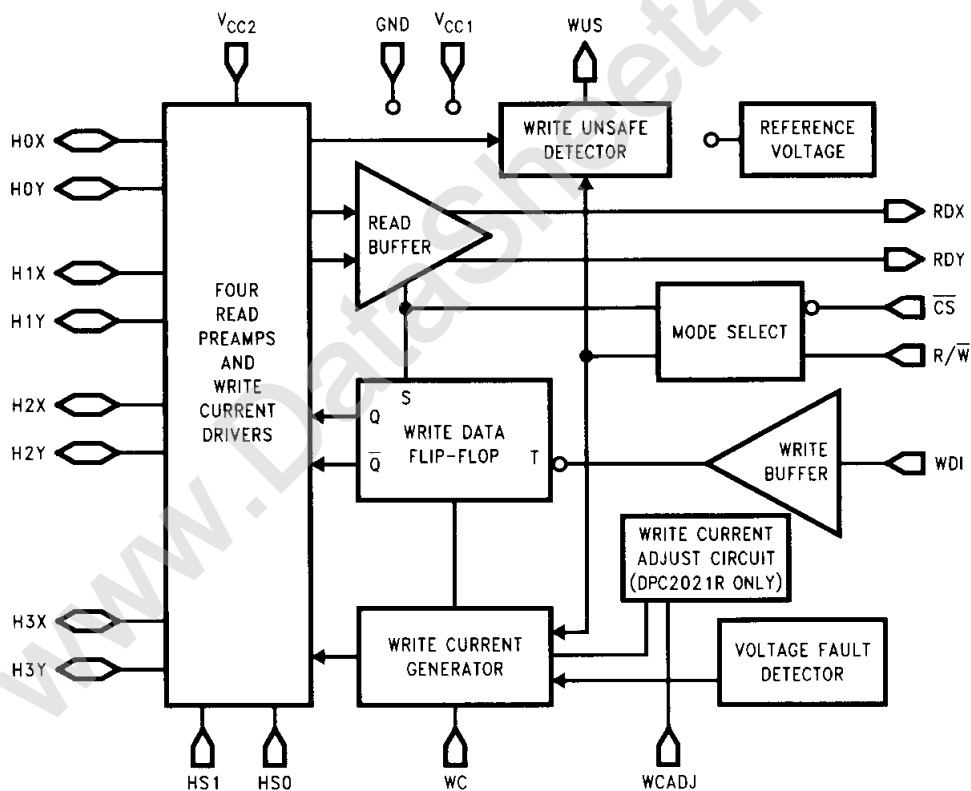
The DPC2021R provides the user with the additional feature of a programmable write current adjustment pin (WCADJ).

Upon request, other options such as lower read gain, no damping resistance, and various packages are available.

### Features

- Designed for two-terminal heads
- Low input noise: 0.47 nV/ $\sqrt{\text{Hz}}$  typical
- Low power: 120 mW typical in read mode
- Very low idle power: 3 mW typical
- Low input capacitance: 17 pF typical
- Programmable write current source (5 mA–35 mA)
- Write unsafe detection circuitry
- Low power supply protection in write mode
- Head short to ground protection
- Read mode gain: 300 V/V
- Pin compatible with the SSI 32R2020R or 32R2021R respectively

### Circuit Block Diagram



TL/F/11772-1

## Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC1}$ and $V_{CC2}$ )	-0.3 to 7V
TTL Input Maximum Voltage	-0.3 to ( $V_{CC} + 0.3$ )V
Maximum Head Port Voltage	-0.3 to ( $V_{CC} + 0.3$ )V
Maximum Output Current (RDX, RDY)	-10 mA
Maximum Output Current (WUS)	8 mA
Maximum Output Write Current	60 mA
ESD Susceptibility (Note 2)	2000V
Storage Temperature Range	-65°C to +150°C

**Note 1:** Operation beyond these limits may permanently damage the device.

**Note 2:** Human body model is used (120 pF through 1.5 k $\Omega$ ).

## Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC1}$ and $V_{CC2}$ )	4.5	5	5.5	V
Operating Free Air Temperature Range ( $T_A$ )	0		70	°C

## DC Electrical Characteristics

Over recommended operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Test
$I_{CC1R}$	$V_{CC1}$ Supply Current in Read Mode	$\overline{CS} = \text{LOW}$ , $R/\overline{W} = \text{HIGH}$		24	35	mA	(Note A)
$I_{CC1W}$	$V_{CC1}$ Supply Current in Write Mode	$\overline{CS} = \text{LOW}$ , $R/\overline{W} = \text{LOW}$		15	21	mA	(Note A)
$I_{CC1I}$	$V_{CC1}$ Supply Current in Idle Mode	$\overline{CS} = \text{HIGH}$ , $R/\overline{W} = \text{LOW}$		0.6	1	mA	(Note A)
$I_{CC2R}$	$V_{CC2}$ Supply Current in Read Mode	$\overline{CS} = \text{LOW}$ , $R/\overline{W} = \text{HIGH}$		0	0.01	mA	(Note A)
$I_{CC2W}$	$V_{CC2}$ Supply Current in Write Mode	$\overline{CS} = \text{LOW}$ , $R/\overline{W} = \text{LOW}$		$4 + I_W$	$7 + I_W$	mA	(Note A)
$I_{CC2I}$	$V_{CC2}$ Supply Current in Idle Mode	$\overline{CS} = \text{HIGH}$ , $R/\overline{W} = \text{LOW}$		0	0.01	mA	(Note A)
$PD_R$	Power Dissipation in Read Mode	$\overline{CS} = \text{LOW}$ , $R/\overline{W} = \text{HIGH}$		120	195	mW	(Note A)
$PD_W$	Power Dissipation in Write Mode	$\overline{CS} = \text{LOW}$ , $R/\overline{W} = \text{LOW}$		$100 + 4I_W$	$155 + 4.3I_W$	mW	(Note A)
$PD_I$	Power Dissipation in Idle Mode	$\overline{CS} = \text{HIGH}$ , $R/\overline{W} = \text{LOW}$		3	5.5	mW	(Note A)
$V_{IH}$	TTL Input High Voltage		2			V	(Note A)
$V_{IL}$	TTL Input Low Voltage				0.8	V	(Note A)
$I_{IH}$	TTL Input High Current	$V_{IH} = 2.0V$	-100		100	$\mu A$	(Note A)
$I_{IL}$	TTL Input Low Current	$V_{IL} = 0.8V$	-150		100	$\mu A$	(Note A)

**Note A:** This parameter is guaranteed by outgoing testing.

**Note B:** The limit values have been determined by characterization data. No outgoing tests are performed.

**AC Electrical Characteristics** Over recommended operating conditions unless otherwise specified.  $I_W = 20 \text{ mA}$ ,  $L_h = 1 \mu\text{H}$ ,  $R_h = 30\Omega$  and  $f(\text{data}) = 5 \text{ MHz}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Test
$t_{dRW}$	Time Delay Switching from Read to Write Modes	R/ $\bar{W}$ Transition to 90% of Write Current		0.15	0.6	$\mu\text{s}$	(Note A)
$t_{dWR}$	Time Delay Switching from Write to Read Modes	R/ $\bar{W}$ Transition to 90% of 100 mV Read Signal Envelope		0.40	0.8	$\mu\text{s}$	(Note A)
$t_{dSELECT}$	Time Delay Switching from Idle to Either Read or Write Modes	$\bar{CS}$ Negative Transition to 90% $I_{write}$ or 90% of 100 mV, 10 MHz Signal Envelope		0.15	0.6	$\mu\text{s}$	(Note A)
$t_{dIDLE}$	Time Delay Switching from Either Read or Write to Idle Mode			0.10	0.6	$\mu\text{s}$	(Note A)
$t_{dHEAD}$	Time Delay Switching from One Head to Another	HS0/HS1 to 90% of 100 mV, 10 MHz Read Signal Envelope			0.6	$\mu\text{s}$	(Note A)
$t_{dUNSAFE}$	Time Delay from a Write Safe to a Write Unsafe Condition	WDI Negative Transition to WUS Positive Transition	1	2.5	3.6	$\mu\text{s}$	(Note A)
$t_{dSAFE}$	Time Delay from a Write Unsafe to a Write Safe Condition	WDI Negative Transition to WUS Negative Transition			0.6	$\mu\text{s}$	(Note A)
$t_{dHDi}$	Time Delay from WDI to a Current Direction Change in a Head Output	$L_h = R_h = 0$ , Measurements Made from 50% Points		7	15	ns	(Note A)
ASY <sub>HD</sub>	Head Current Asymmetry	WDI has 1 ns $t_{r/f}$ Times, $L_h = R_h = 0$			1	ns	(Note B)
$t_{r/f}(\text{HD})$	Head Current Rise and Fall Times	Measurements Made from 10%–90% Points, $L_h = R_h = 0$		4	8	ns	(Note B)

**Note A:** This parameter is guaranteed by outgoing testing.

**Note B:** The limit values have been determined by characterization data. No outgoing tests are performed.

## DC and AC Electrical Characteristics

Over recommended operating conditions unless otherwise specified.

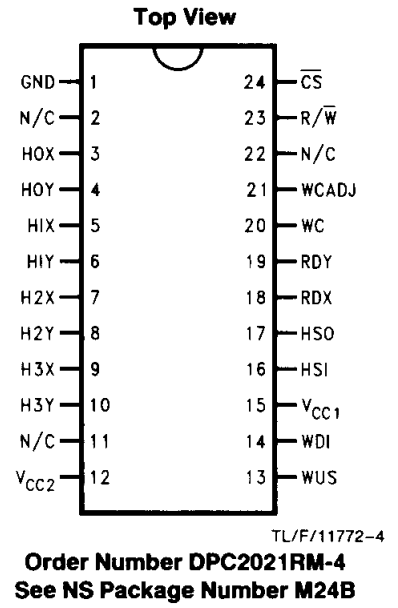
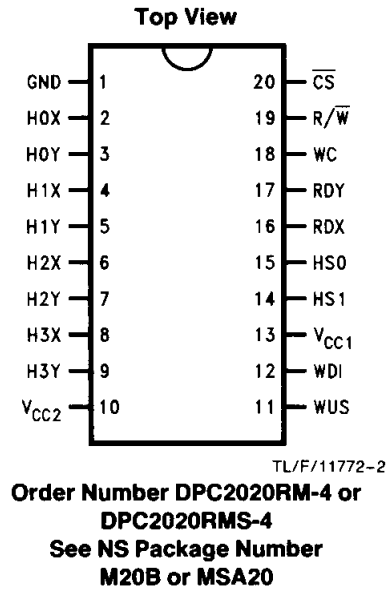
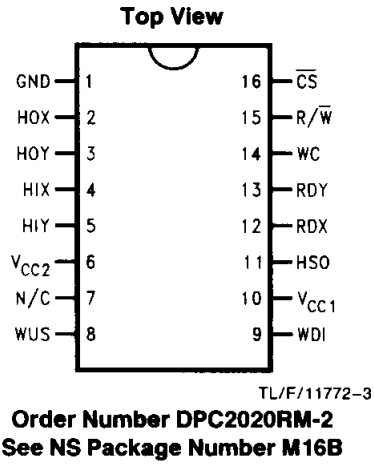
Symbol	Parameter	Conditions	Min	Typ	Max	Units	Test
<b>READ MODE (DC and AC) Read Characteristics: <math>C_L</math> (RDX, RDY) &lt; 20 pF, <math>R_L</math> (RDX, RDY) = 1 k<math>\Omega</math></b>							
$A_V$	Differential Voltage Gain	$V_{IN} = 1 \text{ mV}_{PP}$ @ 1 MHz	250	300	350	V/V	(Note A)
$V_N$	Input Noise Voltage	$BW = 15 \text{ MHz}$ , $L_h = R_h = 0$		0.47	0.7	nV/ $\sqrt{\text{Hz}}$	(Note B)
$C_I$	Differential Input Capacitance	$V_{IN} = 1 \text{ mV}_{PP}$ , $f = 5 \text{ MHz}$		17	22	pF	(Note B)
$R_I$	Differential Input Resistance	$f = 5 \text{ MHz}$ , $V_{IN} = 1 \text{ mV}_{PP}$	720	1250		$\Omega$	(Note A)
$V_{IRANGE}$	Input Voltage Dynamic Range (Note 1)	$f = 5 \text{ MHz}$	4	6		mV $_{PP}$	(Note A)
$V_{O(OFF)}$	Output Offset Voltage		-150		150	mV	(Note A)
$R_{O(SE)}$	Single Ended Output Resistance	$f = 5 \text{ MHz}$			40	$\Omega$	(Note A)
$I_{OUT}$	Output Current	AC Coupled Load, RDX to RDY	1.4			mA	(Note A)
$V_{O(CM)}$	Common Mode Output Voltage at RDX, RDY Pins		$V_{CC}$ -2.7		$V_{CC}$ -1.8	V	(Note A)
$BW_{1dB}$	Voltage Bandwidth—1 dB	$V_{IN} = 1 \text{ mV}_{PP}$ , $Z_{source} < 5\Omega$	20			MHz	(Note B)
$BW_{3dB}$	Voltage Bandwidth—3 dB	$V_{IN} = 1 \text{ mV}_{PP}$ , $Z_{source} < 5\Omega$	40	65		MHz	(Note B)
CMRR	Common Mode Rejection Ratio	$V_{CM} = 100 \text{ mV}_{PP}$ @ 5 MHz	60	90		dB	(Note A)
PSRR	Power Supply Rejection Ratio	$\Delta V_{CC} = 100 \text{ mV}_{PP}$ @ 5 MHz	60	90		dB	(Note A)
CSRR	Channel Separation	Unselected Channel 100 mV $_{PP}$	50	60		dB	(Note A)
<b>WRITE MODE (DC) Write Characteristics: <math>I_W = 20 \text{ mA}</math>, <math>L_h = 1 \mu\text{H}</math>, <math>R_h = 30\Omega</math></b>							
$K_W$	Write Current Constant		0.96	0.99		mA/mA	(Note A)
$V_{WC}$	Write Current Voltage	$1 \text{ mA} < I_W < 35 \text{ mA}$	1.15	1.25	1.35	V	(Note A)
$V_H$	Differential Head Voltage Swing	$I_W = 20 \text{ mA}$ , Open Head	3.4	5.0		V $_{PP}$	(Note A)
$I_{H(NS)}$	Unselected Head Current				100	$\mu\text{A}$	(Note A)
$C_D$	Differential Head Load Capacitance				25	pF	(Note B)
$R_D$	Differential Head Load Resistance	Switched Resistor in Write Only		320		$\Omega$	(Note A)
$I_W$	Write Current Range		5		35	mA	(Note A)
$f_W$	WDI Transition Frequency		1			MHz	(Note A)
$V_{OLWUS}$	WUS Output Low Voltage	$I_{LOAD} < 2 \text{ mA}$			0.5	V	(Note A)
$V_{CC1F}$	$V_{CC1}$ Shut-Off Voltage	$I_W < 0.2 \text{ mA}$	3.8		4.2	V	(Note A)
$t_{PWH(WDI)}$	WDI Pulse Width (HIGH)	$V_{IL} \geq 0.2\text{V}$	10			ns	(Note B)
$t_{PWL(WDI)}$	WDI Pulse Width (LOW)		5			ns	(Note B)
$V_{WCADJ}$	Write Current Adjust Voltage	DPC2021R Only	2.0	2.5	3.0	V	(Note A)
$I_{WCADJ}$	Write Current Adjust Range	DPC2021R only	0		0.5	mA	(Note A)
$A_{WCADJ}$	Write Current Adjust Gain	DPC2021R only	26	30	32	mA/mA	(Note A)

**Note 1:** The dynamic input voltage range specification limit is defined as the point where the gain falls to 90% of its small signal gain value.

**Note A:** This parameter is guaranteed by outgoing testing.

**Note B:** The limit values have been determined by characterization data. No outgoing tests are performed.

# Connection Diagrams



## Pin Descriptions

Name	Type	Description
V <sub>CC1</sub>	Power Supply	Power supply pin (5V ± 10%)
V <sub>CC2</sub>	Power Supply	Power supply pin for write current drivers only (5V ± 10%)
WDI	Input (TTL)	A negative transition (logical HIGH-to-LOW) toggles the head current between the X and Y head connections.
HS0, HS1	Input (TTL)	Logic levels are applied to these pins to select 1 of 4 heads (see Table I).
R/W	Input (TTL)	A logic HIGH level selects the read mode while a LOW logic level selects the write mode.
CS	Input (TTL)	A HIGH logic level disables the operation of the device and puts the read data outputs (RDX, RDY) into a high impedance state.
H0X, H0Y – H3X, H3Y	Outputs	X and Y connections to the read/write heads.
WUS	Output	A logical HIGH level at this pin indicates that one of several conditions has been detected by internal circuitry which makes writing unsafe.
RDX, RDY	Output	Differential read data outputs.
WC		A resistor is connected from this pin to ground to control the magnitude of the write current.
WCADJ		A resistor is connected from this pin to ground to reduce the magnitude of the write current. Available on the DPC2021R only.
GND	Ground	Device ground.

## Basic Circuit Operation

The DPC2020R can address up to four two-terminal heads, providing the write current drive in the write mode or read data amplification in the read mode.

Head selection is controlled by the logic states on two pins, HEAD SELECT 0 (HS0) and HEAD SELECT 1 (HS1). Table I defines the results of each combination of these two pins. These pins have internal pull-down current so that head 0 is selected if an open condition exists on these pins.

**TABLE I. Head Selection**

HS1	HS0	Head Selected
0	0	0
0	1	1
1	0	2
1	1	3

The selection of device mode (write, read or idle) is also controlled by two pins, CHIP SELECT ( $\overline{CS}$ ) and READ/WRITE (R/ $\overline{W}$ ). Table II defines the results of each combination of these two pins. These pins have internal pull-up resistors so that the idle condition is selected if an open condition exists on these pins.

**TABLE II. Mode Selection**

$\overline{CS}$	R/ $\overline{W}$	Mode Selected
0	0	WRITE
0	1	READ
1	0	IDLE
1	1	IDLE

### WRITE MODE

The write mode is entered by setting both  $\overline{CS}$  and R/ $\overline{W}$  to logical LOW values. In this mode, the device acts as a current switch which toggles between the X and Y sides of the selected head on each HIGH-to-LOW logic level transition of the WRITE DATA INPUT (WDI). When entering the write mode from the read mode, the write data flip-flop is initialized to pass current into the X side of the selected head. The magnitude of the write current is set by an external resistor,  $R_{WRITE}$ , connected between the WC pin and ground. The relationship between the write current and the write resistor is:

$$I_{WRITE} = K_W \times \frac{V_{write}}{R_{write}}$$

The portion of the write current that passes through the head ( $I_h$ ) is defined as:

$$I_h = \frac{I_W}{1 + R_h/R_d}$$

where:  $R_h$  = the sum of the head and external wire resistance and  $R_d$  = the damping resistance (if any).

When entering the write mode, the write unsafe detector circuitry is enabled. This circuit disables the write current

generator and issues a high level output at the WRITE UNSAFE (WUS) output when any of the following conditions exists;

1. Write data input frequency is too low.
2. The device is in the read mode.
3. The chip is disabled.
4. No write current exists.
5. The head is an open circuit.

The WUS pin is an open-collector output and requires an external pull-up resistor. After the fault condition has been removed, two negative transitions of the WDI pin are required to clear the write unsafe circuitry.

A power supply fault detection circuit is provided on chip. This circuit will disable the write current generator during device power-up, power-down or when a power supply fault occurs. This will prevent the possibility of writing bad data onto the media.

The DPC2021R has an added feature which allows for the adjustment of the write current through the use of the write current adjust pin (WCADJ). A resistor is connected between the WCADJ pin and ground to divert a proportional amount of current from the actual head write current. The WCADJ pin is nominally biased at half of the supply voltage ( $V_{CC1}$ ). The amount of write current decreased is shown below:

$$I_{W(DECREESE)} = 29(I_{WCADJ}) = 29 \left( \frac{V_{WCADJ}}{R_{WCADJ}} \right)$$

or

$$I_{W(FINAL)} = I_{WC} - 29(I_{WCADJ})$$

Allowing the WCADJ pin to float or pulling it high will disable this feature. A DAC which can sink a controllable amount of current may also be connected to the WCADJ pin.

### READ MODE

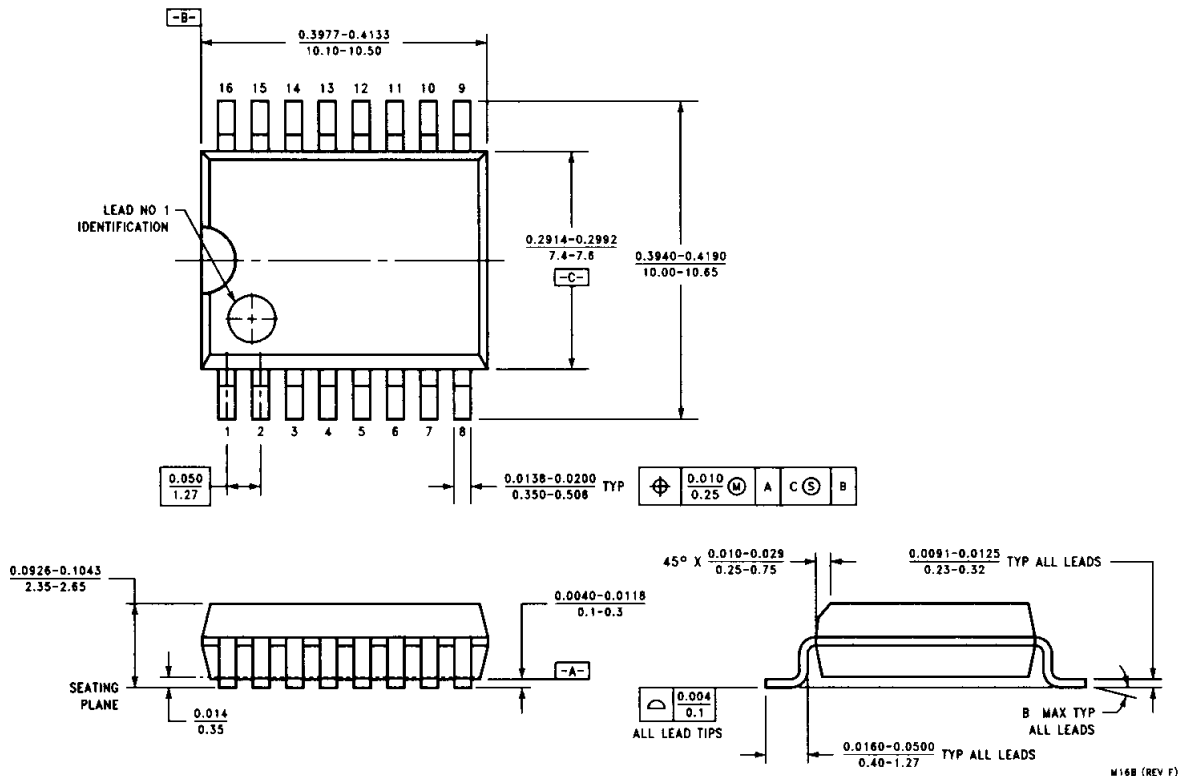
The read mode is entered by setting  $\overline{CS}$  to a LOW logic level and R/ $\overline{W}$  to a HIGH logic level. In this mode the write current generator is disabled and a low noise differential amplifier is enabled. The amplified head read-back signal is available at the RDX and RDY pins. These outputs are differential emitter-followers and should be AC coupled to the load.

During the write or idle modes, the read amplifier is disabled and the RDX, RDY outputs are forced to a high impedance state. This allows these outputs to be wire-ORed with outputs from other devices to support multiple read/write applications.

### IDLE MODE

The idle mode is entered by applying a logical HIGH level to the  $\overline{CS}$  pin. In this mode the RDX and RDY outputs are in a high impedance state and the device is disabled. This will reduce the power consumption to a minimum value when the device is not needed, which is particularly important for battery applications.

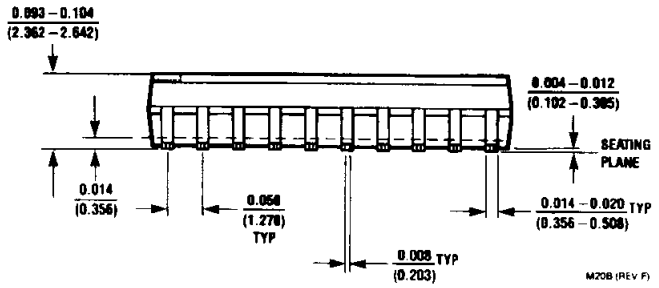
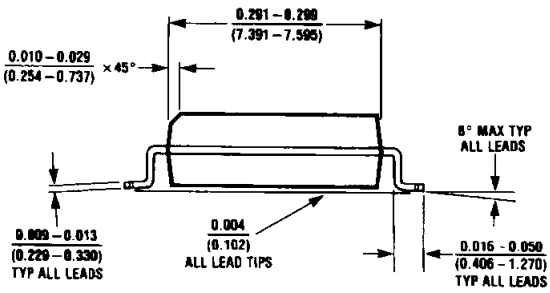
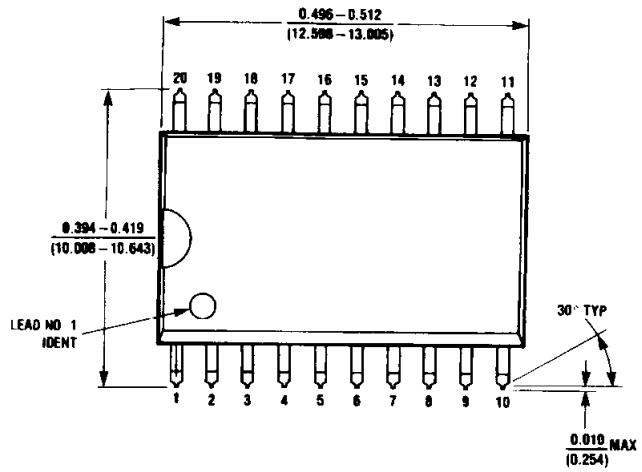
**Physical Dimensions** inches (millimeters)



**16-Pin Small Outline Package**  
**Order Number DPC2020RM-2**  
**NS Package Number M16B**

M16B (REV F)

**Physical Dimensions** inches (millimeters) (Continued)

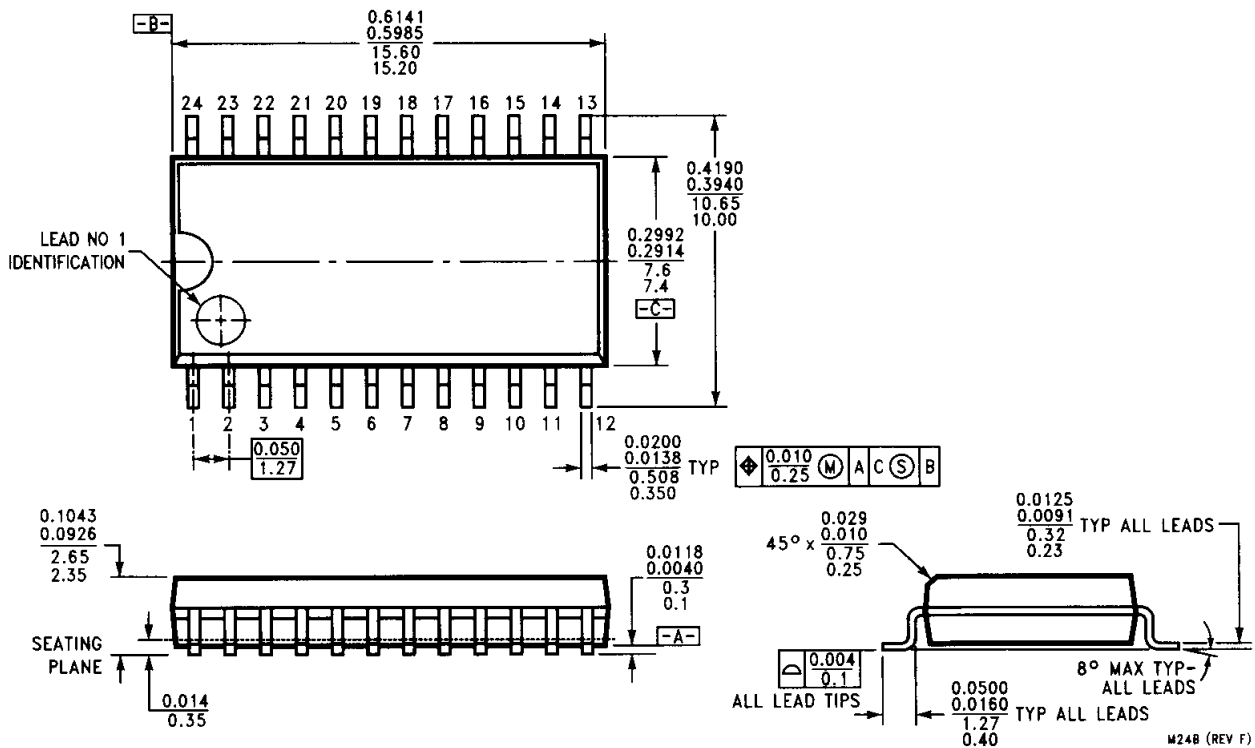


M20B (REV F)

**20-Pin Small Outline Package**  
**Order Number DPC2020RM-4**  
**NS Package Number M20B**

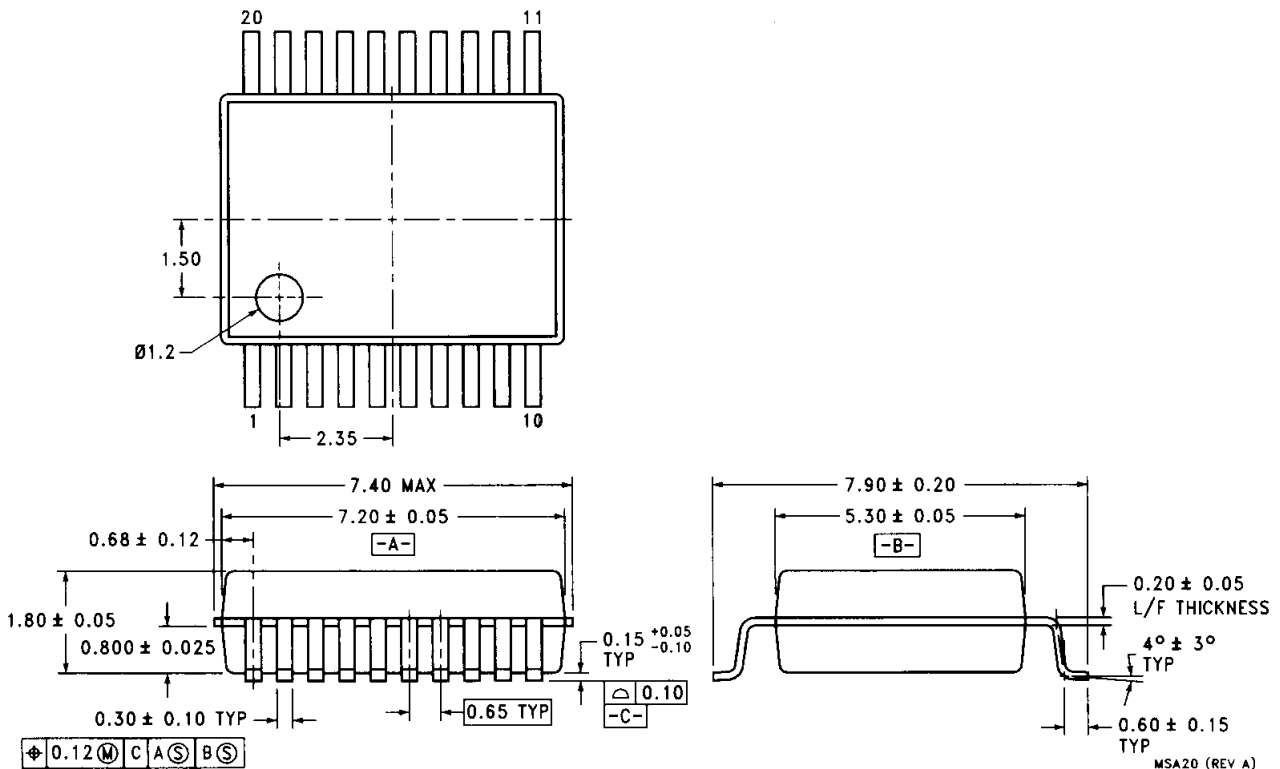


**Physical Dimensions** inches (millimeters) (Continued)



**24-Pin Small Outline Package**  
**Order Number DPC2021RM-4**  
**NS Package Number M24B**

M24B (REV F)



**20-Pin Shrink Small Outline Package**  
**Order Number DPC2020RMS-4**  
**NS Package Number MSA20**

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**National Semiconductor Corporation**  
 2900 Semiconductor Drive  
 P.O. Box 58090  
 Santa Clara, CA 95052-8090  
 Tel: 1(800) 272-9959  
 TWX: (910) 339-9240

**National Semiconductor GmbH**  
 Industriestrasse 10  
 D-82256 Fürstfeldbruck  
 Germany  
 Tel: (0-81-41) 103-0  
 Telex: 527649  
 Fax: (0-81-41) 10-35-06

**National Semiconductor Japan Ltd.**  
 Senseido Bldg. 5F  
 4-15-3 Nishi Shinjuku  
 Shinjuku-Ku,  
 Tokyo 160, Japan  
 Tel: 3-3299-7001  
 FAX: 3-3299-7000

**National Semiconductor Hong Kong Ltd.**  
 13th Floor, Straight Block  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 737-1600  
 Telex: 51292 NSHKL  
 Fax: (852) 736-9960

**National Semiconductores Do Brazil Ltda.**  
 Av. Brig. Faria Lima, 1409  
 6 Andar  
 Cep-01451, Paulistano,  
 Sao Paulo, SP, Brazil  
 Tel: (55-11) 212-5066  
 Telex: 391-1131931 NSBR BR  
 Fax: (55-11) 212-1181

**National Semiconductor (Australia) Pty, Ltd.**  
 16 Business Park Dr.  
 Notting Hill, VIC 3168  
 Australia  
 Tel: (3) 558-9999  
 Fax: (3) 558-9996