

## Description

The DPS1035 is part of a family of power switches optimized for the USB Type-C™ and other hot-swap applications. Through the analog interface, exception status is reported and functions like voltage limiting and output voltage ramp-up rate can be programmed.

This device is designed to operate between 4.5V and 24V. Its built-in fault-handling mechanism includes reverse voltage and current blocking, input over-voltage protection, and thermal shutdown. In addition, the ramp-up time of the output voltage can be adjusted to minimize in-rush current and to ensure system stability. Before any exception condition is notified via the low-active FAULTB signal, glitch of 7ms is applied to prevent false triggering.

The DPS1035 is housed in the low-profile and space-saving V-QFN4040-17 package which is manufactured with environmentally friendly material.

## Features

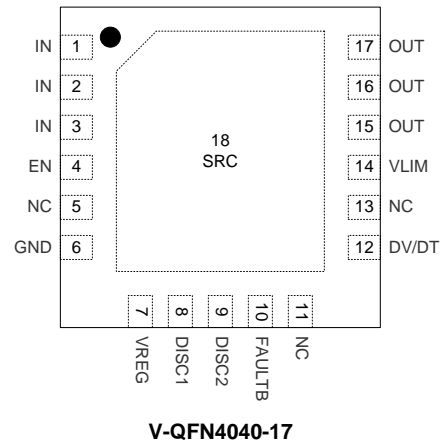
- Wide Operating Voltage Range: 4.5V to 24V
- 1-Channel Power Switch with Built-In Fault Detection and Recovery Mechanisms like Input Under-Voltage Lockout, Reverse-Voltage & Current Blocking, Thermal Shutdown and Input Over-Voltage Protection
- $R_{DS(ON)}$  of Embedded Power MOSFET at 30mΩ
- Adjustable DV/DT Control at Start-Up
- Manual Discharge ON/OFF Control for IN and OUT Ports
- Fault Reporting (FAULTB) with Blanking Time at 7ms Typical
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments

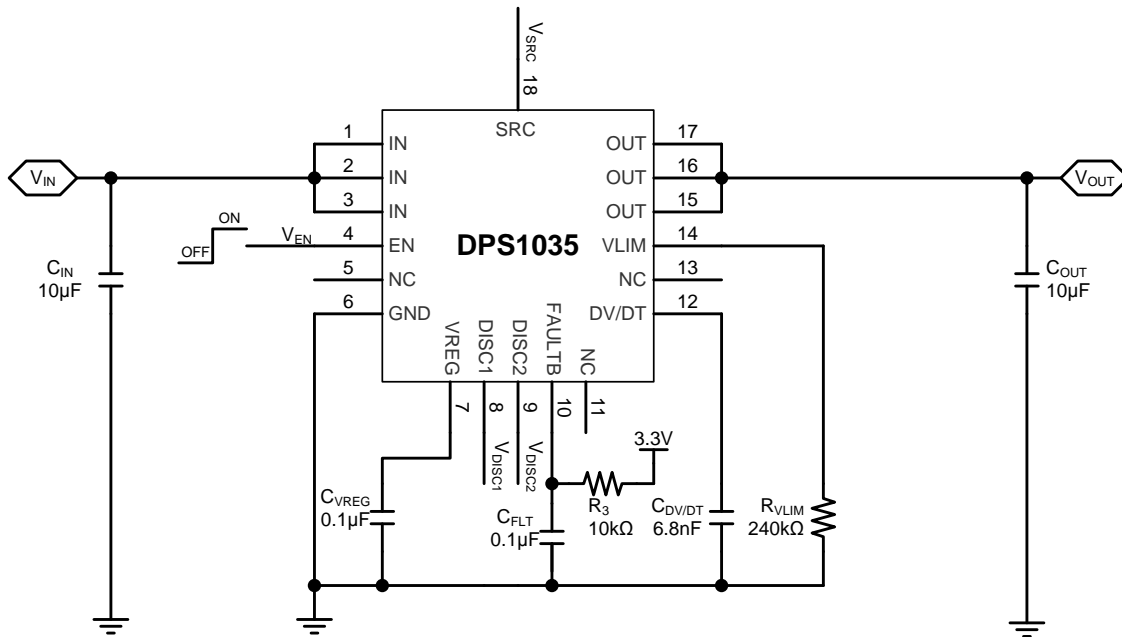
(Top View)



## Applications

- Notebook, Desktop & AIO PCs; Servers and Tablets
- Docking Stations, Universal & Multimedia Hubs
- FPTVs, PC Monitors
- Set-Top-Boxes, Residential Gateways, Storage Devices

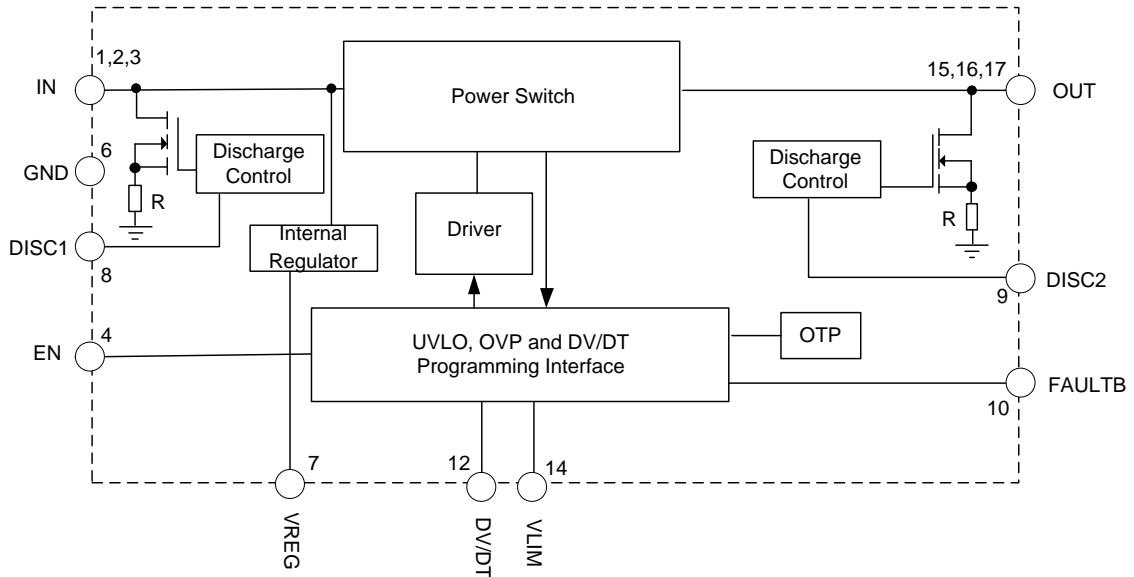
**Typical Application Circuit**



**Pin Descriptions**

Pin Number	Pin Name	Type	Function
1, 2, 3	IN	P	Power Supply and Input Port.
4	EN	I	Enable. '0' = device OFF; '1' = device ON. This pin must not be left floating.
5, 11, 13	NC	—	No Connection. All NC pins must be left floating.
6	GND	GND	Device Ground
7	VREG	I/O	Voltage Regulator. A 0.1µF capacitor is recommended between this pin and ground.
8	DISC1	I	IN Port Discharge Control. '1' = port voltage to be discharged; '0' = disabled.
9	DISC2	I	OUT Port Discharge Control. '1' = port voltage to be discharged; '0' = disabled.
10	FAULTB	O	Fault Status Indicator. An external pull-up resistor is required. This active-low pin shall be tied to GND when not used.
12	DV/DT	I/O	Ramp-up Control. A capacitor between this pin and GND sets the ramp-up rate.
14	VLIM	I/O	Voltage Limit Setting. A resistor between this pin and GND sets the over-voltage limit of the IN port.
15, 16, 17	OUT	O	Output Port.
18 (Exposed Pad)	SRC	I/O	Common Source. The exposed pad of the V-QFN4040-17 package must not be connected to any signal.

**Functional Block Diagram**



**Absolute Maximum Ratings** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
$V_{IN}, V_{OUT}$	Voltage Range of IN and OUT Pins	-0.3 to 30	V
$V_{IO}$	Voltage Range of Others (EN, VREG, DISC1, DISC2, FAULTB, DV/DT and VLIM Pin)	-0.3 to 6	V
$I_{OUT}$	Output Load Current Range	5	A
$T_J$	Operating Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_L$	Lead Temperature	+260	$^\circ\text{C}$
$T_{ST}$	Storage Temperature	-65 to +150	$^\circ\text{C}$
ESD	Human Body Model (HBM), JESD22-A114	2	kV
	Charge Device Model (CDM)	0.5	

Note: 4. These are stress ratings only. Operation outside the absolute maximum ratings may cause device failure. Operation at the absolute maximum rating for extended periods may reduce device reliability.

**Thermal Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.) (Note 5)

Symbol	Parameter	Rating	Unit
$P_D$	Power Dissipation	2.1	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	58.5	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	9.4	$^\circ\text{C/W}$

Note: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1"x1" copper pad layout.

**Recommended Operating Conditions** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Supply Voltage	4.5	24	V
$V_{OUT}$	Output Voltage	0	24	V
$I_{OUT}$	Output Load Current	0	3.5	A
$C_{IN}$	Input Capacitance	1	—	$\mu\text{F}$
$C_{OUT}$	Output Capacitance	1	—	$\mu\text{F}$
$V_{EN}$	Input Voltage on EN	0	5	V
$V_{DISC1}, V_{DISC2}$	Input Voltage on DISC1 and DISC2	0	5.5	V

**Electrical Characteristics**

 (@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 4.5\text{V}$  to  $24\text{V}$ ,  $C_{IN} = C_{OUT} = 10\mu\text{F}$ ,  $V_{EN} = 3.3\text{V}$ ,  $C_{DV}/DT = 1\text{nF}$ ,  $R_{VLIM} = 240\text{k}\Omega$ , unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Bias Supply</b>						
$V_{UVLO}$	$V_{IN}$ Under-Voltage Lockout Threshold	$V_{IN}$ Rising	3.2	3.7	4	V
$V_{UVHY}$	$V_{IN}$ Under-Voltage Lockout Threshold Hysteresis	$V_{IN}$ Falling	—	250	—	mV
$I_{SHDN}$	Shutdown Current (Disabled)	$V_{IN} = 5\text{V}, V_{EN} = 0\text{V}$	—	—	10	$\mu\text{A}$
		$V_{IN} = 12\text{V}, V_{EN} = 0\text{V}$	—	—	25	
		$V_{IN} = 20\text{V}, V_{EN} = 0\text{V}$	—	—	50	
$I_Q$	Quiescent Current (Enabled)	$V_{IN} = 5\text{V}, \text{No Load}$	—	—	3	mA
		$V_{IN} = 12\text{V}, \text{No Load}$	—	—	4	
		$V_{IN} = 20\text{V}, \text{No Load}$	—	—	4.5	
<b>Enable Control</b>						
$V_{ENL}$	EN Threshold Voltage Low	$V_{EN}$ Falling	—	—	0.4	V
$V_{ENH}$	EN Threshold Voltage High	$V_{EN}$ Rising	1.4	—	—	
$I_{EN}$	EN Input Leakage Current	$V_{IN} = 5\text{V}, V_{EN} = 5\text{V}$	—	—	1	$\mu\text{A}$
<b>Over-Voltage Protection</b>						
$I_{VLIM}$	$V_{LIM}$ Sourcing Current	$V_{IN} = 5\text{V}, R_{VLIM} = 57.6\text{k}\Omega$	—	10	—	$\mu\text{A}$
$R_{VLIM\_MAX}$	Maximum $R_{VLIM}$	—	—	—	300	$\text{k}\Omega$
$V_{OVPRTH}$	Input Over-Voltage Threshold, Rising	$R_{VLIM} = 57.6\text{k}\Omega, V_{IN}$ Rising	—	6	—	V
		$R_{VLIM} = 240\text{k}\Omega, V_{IN}$ Rising	—	24	—	
$V_{OVPFTH}$	Input Over-Voltage Threshold, Falling	$R_{VLIM} = 57.6\text{k}\Omega, V_{IN}$ Falling	—	5.6	—	V
		$R_{VLIM} = 240\text{k}\Omega, V_{IN}$ Falling	—	23.6	—	
<b>MOSFET</b>						
$R_{DS(ON)}$	Switch ON Resistance	$V_{IN} = 5\text{V}, I_{OUT} = 1\text{A}$	—	30	40	m $\Omega$
		$V_{IN} = 12\text{V}, I_{OUT} = 1\text{A}$	—	30	40	
		$V_{IN} = 20\text{V}, I_{OUT} = 1\text{A}$	—	30	40	
$I_{LKGSR}$	OUT Leakage Current in OFF State, Sourcing	$V_{EN} = 0\text{V}, V_{OUT} = 0\text{V}$	—	—	1	$\mu\text{A}$
$I_{LKGSK}$	OUT Leakage Current in OFF State, Sinking	$V_{IN} = 3.3\text{V}, V_{EN} = 0\text{V}, V_{OUT} = 5\text{V}$	—	—	1	$\mu\text{A}$
		$V_{IN} = 3.3\text{V}, V_{EN} = 0\text{V}, V_{OUT} = 12\text{V}$	—	—	1	
		$V_{IN} = 3.3\text{V}, V_{EN} = 0\text{V}, V_{OUT} = 20\text{V}$	—	—	1	
<b>Reverse-Voltage Protection</b>						
$V_{RVPFTH}$	$V_{IN} - V_{OUT}$ Threshold Entering into Reverse Protection	$V_{IN} - V_{OUT}$ Falling	—	-40	—	mV
$V_{RVPRTH}$	$V_{IN} - V_{OUT}$ Threshold Exiting from Reverse Protection	$V_{IN} - V_{OUT}$ Rising	-15	0	—	
$t_{RVPTD}$	Reverse Protection Response Time	—	—	—	2	$\mu\text{s}$

**Electrical Characteristics (Cont.)**

 (@T<sub>A</sub> = +25°C, V<sub>IN</sub> = 4.5V to 24V, C<sub>IN</sub> = C<sub>OUT</sub> = 10μF, V<sub>EN</sub> = 3.3V, C<sub>DV/DT</sub> = 1nF, R<sub>VLM</sub> = 240kΩ, unless otherwise specified.)

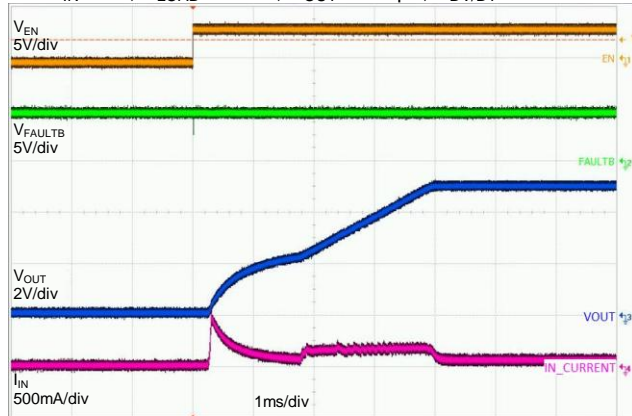
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Output Ramping Control</b>						
I <sub>DV/DT</sub>	DV/DT Sourcing Current	V <sub>DV/DT</sub> = 0V	—	1	—	μA
G <sub>DV/DT</sub>	DV/DT to OUT Gain	ΔV <sub>OUT</sub> / ΔV <sub>DV/DT</sub> , Guaranteed by Design	—	12	—	V/V
<b>Output Timing</b>						
t <sub>DON</sub>	Output Turn-ON Delay Time	V <sub>IN</sub> = 5V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 0V to 2V	—	0.2	—	ms
		V <sub>IN</sub> = 12V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 0V to 2V	—	0.2	—	
		V <sub>IN</sub> = 20V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 0V to 2V	—	0.2	—	
t <sub>R</sub>	Output Turn-ON Rise Time	V <sub>IN</sub> = 5V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 0V to 2V	—	0.3	—	ms
		V <sub>IN</sub> = 12V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 0V to 2V	—	0.8	—	
		V <sub>IN</sub> = 20V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 0V to 2V	—	1.6	—	
t <sub>DOFF</sub>	Output Turn-OFF Delay Time	V <sub>IN</sub> = 5V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 2V to 0V	—	1	—	μs
		V <sub>IN</sub> = 12V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 2V to 0V	—	2	—	
		V <sub>IN</sub> = 20V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 2V to 0V	—	4	—	
t <sub>F</sub>	Output Turn-OFF Fall Time	V <sub>IN</sub> = 5V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 2V to 0V	—	10	—	μs
		V <sub>IN</sub> = 12V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 2V to 0V	—	25	—	
		V <sub>IN</sub> = 20V, C <sub>OUT</sub> = 1μF, V <sub>EN</sub> = 2V to 0V	—	50	—	
<b>Discharge Control on IN/OUT Pins</b>						
R <sub>DISC1/DISC2</sub>	IN/OUT Discharge Resistance	V <sub>DISC1</sub> = 5V, V <sub>DISC2</sub> = 5V	—	70	—	Ω
		V <sub>DISC1</sub> = 3.3V, V <sub>DISC2</sub> = 3.3V	—	82	—	Ω
V <sub>DISC1L</sub> / V <sub>DISC2L</sub>	DISC1/DISC2 Threshold Voltage Low	V <sub>DISC1</sub> /V <sub>DISC2</sub> Falling	—	—	0.4	V
V <sub>DISC1H</sub> / V <sub>DISC2H</sub>	DISC1/DISC2 Threshold Voltage High	V <sub>DISC1</sub> /V <sub>DISC2</sub> Rising	1.4	—	—	V
<b>Fault Flag (FAULTB): Active Low</b>						
R <sub>FAULTB</sub>	FAULTB Pull-Down Resistor	V <sub>IN</sub> = 7V, R <sub>VLM</sub> = 57.6kΩ, I <sub>FAULTB</sub> = 10mA Sinking	—	25	—	Ω
I <sub>LKGFAULTB</sub>	FAULTB Leakage Current	V <sub>IN</sub> = 5V, R <sub>VLM</sub> = 57.6kΩ, V <sub>FAULTB</sub> = 5V	—	—	1	μA
t <sub>BLANKFAULTB</sub>	FAULTB Blanking Time	V <sub>IN</sub> = 5V, R <sub>VLM</sub> = 57.6kΩ, V <sub>FAULTB</sub> = 5V	—	7	—	ms
<b>Thermal Shutdown</b>						
T <sub>SHDN</sub>	Thermal Shutdown Threshold	—	—	+155	—	°C
T <sub>HYS</sub>	Thermal Shutdown Hysteresis	—	—	+20	—	

**Performance Characteristics**

(@T<sub>A</sub> = +25°C, C<sub>IN</sub> = C<sub>OUT</sub> = 10µF, V<sub>EN</sub> = 3.3V, C<sub>DV/DT</sub> = 1nF, R<sub>VLM</sub> = 240kΩ, unless otherwise specified.)

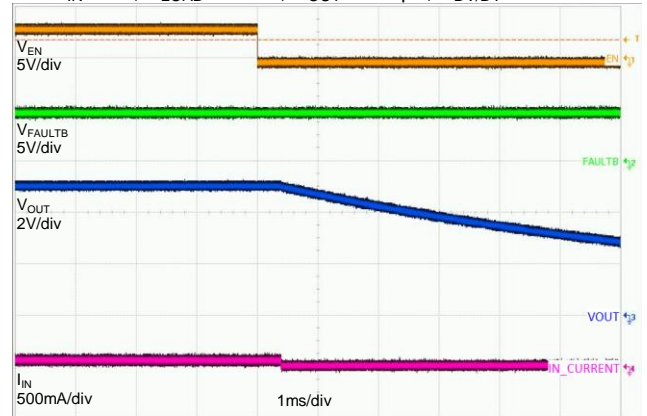
**EN Turn ON and In-rush Current at 5V**

V<sub>IN</sub> = 5V, R<sub>LOAD</sub> = 100Ω, C<sub>OUT</sub> = 100µF, C<sub>DV/DT</sub> = 10nF



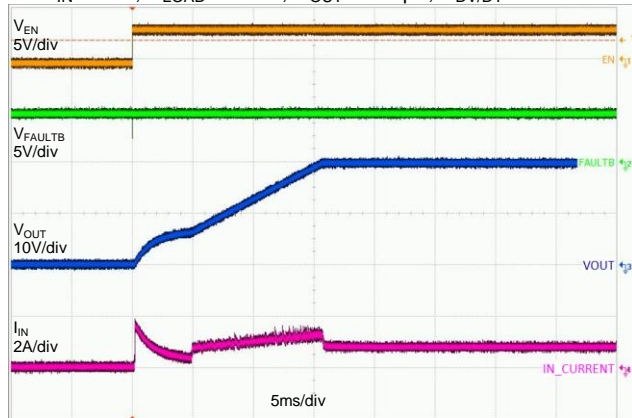
**EN Turn OFF at 5V**

V<sub>IN</sub> = 5V, R<sub>LOAD</sub> = 100Ω, C<sub>OUT</sub> = 100µF, C<sub>DV/DT</sub> = 10nF



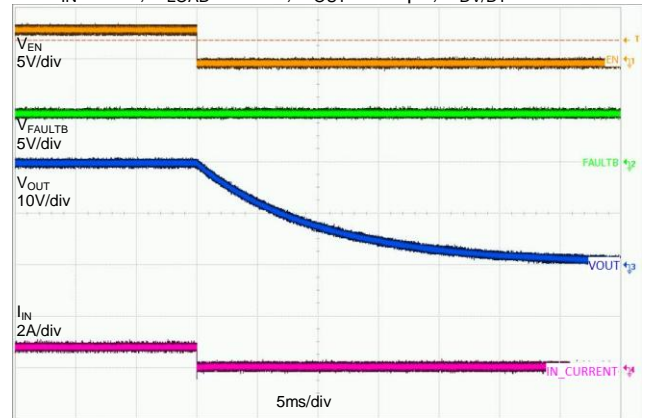
**EN Turn ON and In-rush Current at 20V**

V<sub>IN</sub> = 20V, R<sub>LOAD</sub> = 100Ω, C<sub>OUT</sub> = 100µF, C<sub>DV/DT</sub> = 10nF



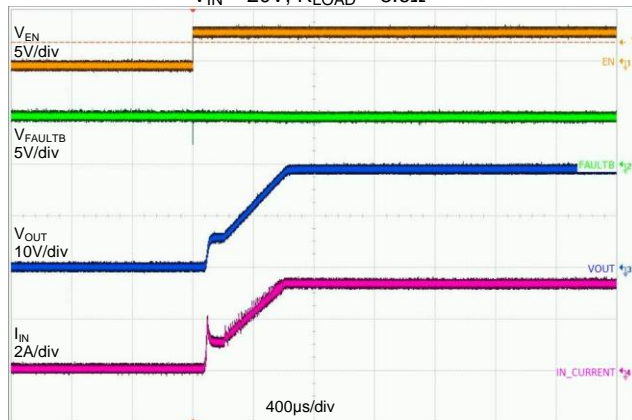
**EN Turn OFF at 20V**

V<sub>IN</sub> = 20V, R<sub>LOAD</sub> = 100Ω, C<sub>OUT</sub> = 100µF, C<sub>DV/DT</sub> = 10nF



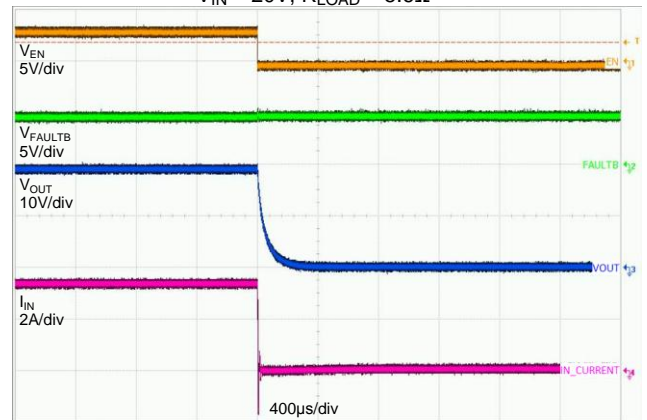
**EN Turn ON with a 5.6Ω Load at 20V**

V<sub>IN</sub> = 20V, R<sub>LOAD</sub> = 5.6Ω



**EN Turn OFF with a 5.6Ω Load at 20V**

V<sub>IN</sub> = 20V, R<sub>LOAD</sub> = 5.6Ω



## Application Information

### General Description

The DPS1035 is an unidirectional power switch designed to meet the input and output voltage/current requirement which is common with many hot-pluggable serial interfaces found in the computing and consumer electronics equipment.

### Ramp-Up Time and In-Rush Current Control

An external capacitor connected from the DV/DT pin to GND defines the slew rate of the output voltage at power-on:

$$dV_{OUT} / dt = (I_{DV/DT} / C_{DV/DT}) \times G_{DV/DT}, \text{ where } I_{DV/DT} = 1\mu\text{A typ. and } G_{DV/DT} = 12$$

The total ramp-up time  $t_{DV/DT}$  of  $V_{OUT}$ , increasing from 0 to  $V_{IN}$ , can be calculated using the following equation:

$$t_{DV/DT} = 8.3 \times 10^4 \times V_{IN} \times C_{DV/DT}$$

The in-rush current at power-up shall be limited by the regulated output voltage ramp.

### Input Over-Voltage Protection (OVP)

The voltage at the IN port is monitored continuously. Whenever voltage at the IN port is found to be larger than the  $V_{OVPRTH}$  value, the built-in over-voltage protection (OVP) fault-handling mechanism is triggered. The internal power MOSFET will be turned OFF to protect the downstream equipment connected. The  $V_{OVPRTH}$  value is determined by:

$$V_{OVPRTH} = 0.1 \times R_{VLIM}, \text{ where the unit of } R_{VLIM} \text{ is } k\Omega \text{ and } 51k\Omega \leq R_{VLIM} \leq 240k\Omega.$$

### Over-Temperature Protection (OTP)

When the junction temperature  $T_J$  reaches the thermal shutdown threshold  $T_{SHDN}$ , the internal power MOSFET would be turned OFF. The internal power MOSFET will be turned ON again once the condition  $[T_J < (T_{SHDN} - T_{HYS})]$  becomes valid.

### Reverse-Voltage Protection (RVP)

The voltage difference,  $[V_{IN} - V_{OUT}]$ , between the IN and OUT ports is monitored continuously. Once the voltage difference drops below the  $V_{RVPFTH}$  level, the device shall immediately turn OFF the internal power MOSFET to prevent the current flowing from the opposite direction. When the reverse-voltage condition is no longer valid, i.e.  $[V_{IN} - V_{OUT}]$  becomes greater than the  $V_{RVPRTH}$  level, the internal power MOSFET shall be turned ON.

### Fault Response

An external pull-up resistor is required. The device generates a warning flag whenever one of the following fault conditions becomes valid: input over-voltage, reversed-voltage, over-temperature. After a de-glitch time-out of 7ms, the low-active FAULTB signal shall be asserted. The FAULTB signal shall remain 'low' and the internal power MOSFET remains OFF until the exception status is no longer valid.

### Discharge Function

To facilitate the various applications envisioned by the system designers, the IN and OUT ports can be discharged via two external controls: DISC1, DISC2. The internal discharge resistor is around 80Ω. The settings are shown in the table below.

DISC1	DISC2	Description
0	0	Discharge function disabled
0	1	OUT Port is being discharged until the pin DISC2 is pulled 'low'
1	0	IN Port is being discharged until the pin DISC1 is pulled 'low'
1	1	Both IN and OUT ports are discharged simultaneously

**Application Information** (Cont.)

**PCB Layout Consideration**

1. Place the input and output capacitors,  $C_{IN}$  and  $C_{OUT}$ , as close as possible to the IN and OUT pins.
2. The power traces, including the power ground, the  $V_{IN}$  trace and the  $V_{OUT}$  trace should be kept direct, short and wide.
3. Place the resistors and capacitors ( $R_{VLIM}$ ,  $C_{DV/DT}$  and  $C_{VREG}$ ) as close as possible to the corresponding device pins.
4. Connect the signal ground to the GND pin, and keep a single connection from GND pin to the power ground behind the input capacitor.
5. For better power dissipation, via holes are recommended to connect the exposed pad's landing area to a large copper polygon on the other side of the printed circuit board. The copper polygons and exposed pad of SRC (common source nodes of internal power MOSFET) shall not be connected to any of the signal and power grounds on the printed circuit board.

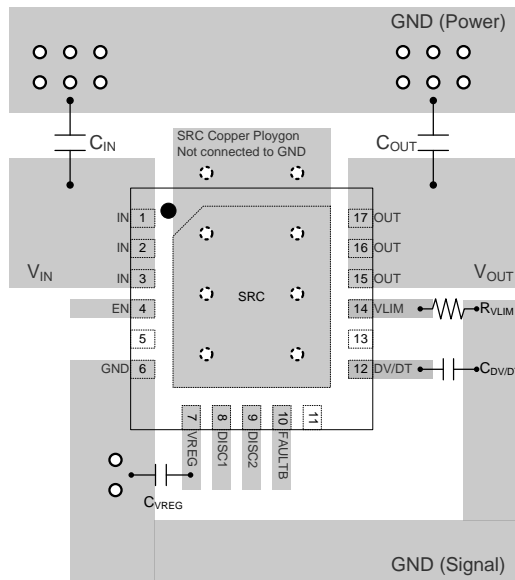
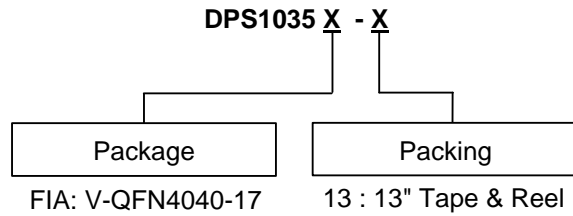


Figure 1 Suggested PCB Layout



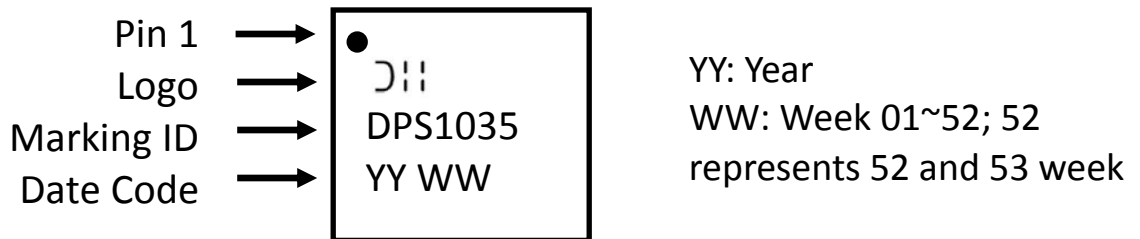
**Ordering Information** (Note 6)



Part Number	Marking ID	Reel Size (inches)	Tape Width (mm)	13" Tape and Reel	
				Quantity	Part Number Suffix
DPS1035FIA-13	DPS1035	13	12	4,000/Tape & Reel	-13

Note: 6. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

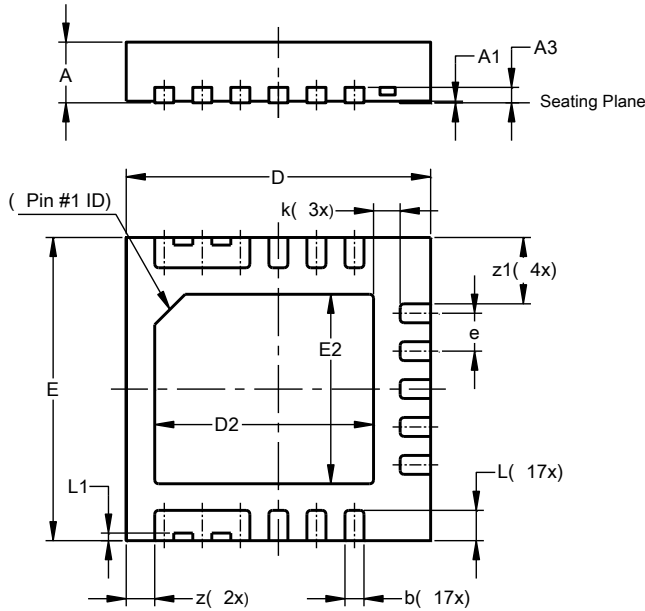
**Marking Information**



**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**V-QFN4040-17**

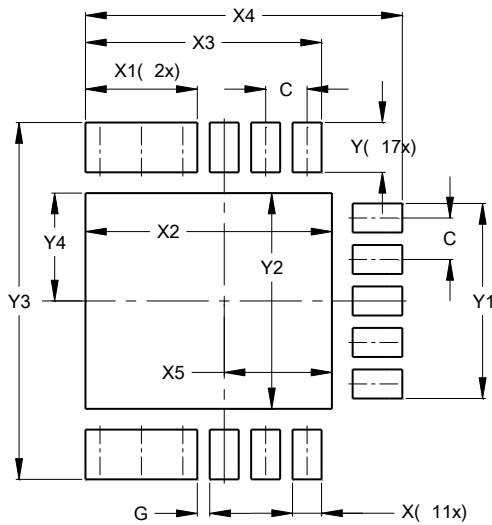


V-QFN4040-17			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.775	2.975	2.875
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
k	-	-	0.35
L1	-	-	0.10
L	0.35	0.45	0.40
z	-	-	0.38
z1	-	-	0.88
<b>All Dimensions in mm</b>			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**V-QFN4040-17**



Dimensions	Value (in mm)
C	0.500
G	0.150
X	0.350
X1	1.350
X2	2.975
X3	2.850
X4	3.825
X5	1.300
Y	0.600
Y1	2.350
Y2	2.600
Y3	4.300
Y4	1.300

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