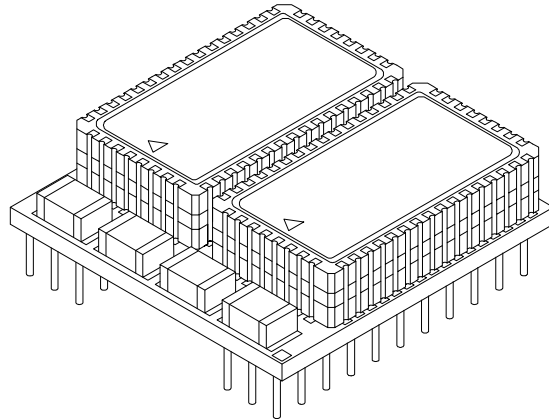


DESCRIPTION:

The DPS128C32BV3 "VERSA-STACK" module is a revolutionary new high speed memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate. It offers 4 Megabits of SRAM in a package envelope of 1.090 x 1.090 x 0.300 inches.

The DPS128C32BV3 contains four individual 128K x 8 SRAMs, packaged in their own hermetically sealed SLCCs making the module suitable for commercial, industrial and military applications.

By using SLCCs, the "Versa-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module, or hybrid techniques.

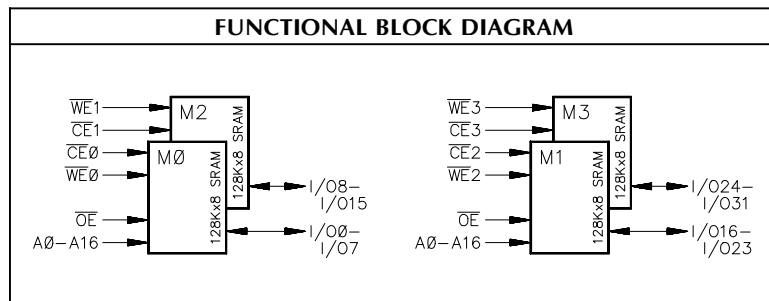


FEATURES:

- Organizations Available:
128K x 32, 256K x 16, or
512K x 8
- Access Times:
20, 25, 30, 35, 45ns
- Fully Static Operation
- No clock or refresh required
- Single +5V Power Supply,
±10% Tolerance
- TTL Compatible
- Common Data Inputs
and Outputs
- Low Data Retention Voltage:
2.0V min.
- 66-Pin PGA "VERSA-STACK"
Package

* Commercial only.

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
CE0 - CE3	Chip Enables
WE0 - WE3	Write Enables
OE	Output Enable
V _{DD}	Power (+5V)
V _{SS}	Ground
N.C.	No Connect



PIN-OUT DIAGRAM																	
I/O8	1	WE1	12	I/O15	23	11	12	23	34	45	56	34	I/O24	45	VDD	56	I/O31
I/O9	2	CE1	13	I/O14	24	1	1	1	1	1	1	35	I/O25	46	CE3	57	I/O30
I/O10	3	VSS	14	I/O13	25	1	1	1	1	1	1	36	I/O26	47	WE3	58	I/O29
A13	4	I/O11	15	I/O12	26	1	1	1	1	1	1	37	A6	48	I/O27	59	I/O28
A14	5	A10	16	OE	27	1	1	1	1	1	1	38	A7	49	A3	60	A0
A15	6	A11	17	N.C.	28	1	1	1	1	1	1	39	N.C.	50	A4	61	A1
A16	7	A12	18	WE0	29	1	1	1	1	1	1	40	A8	51	A5	62	A2
N.C.	8	VDD	19	I/O7	30	1	1	1	1	1	1	41	A9	52	WE2	63	I/O23
I/O0	9	CE0	20	I/O6	31	1	1	1	1	1	1	42	I/O16	53	CE2	64	I/O22
I/O1	10	N.C.	21	I/O5	32	1	1	1	1	1	1	43	I/O17	54	VSS	65	I/O21
I/O2	11	I/O3	22	I/O4	33	11	22	33	44	55	66	44	I/O18	55	I/O19	66	I/O20

RECOMMENDED OPERATING RANGE ³						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage		2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage		-0.5 ²		0.8	V
T _A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	High-Z	Standby
D _{OUT} Disable	L	H	H	High-Z	Active
Read	L	H	L	D _{OUT}	Active
Write	L	L	X	D _{IN}	Active

H = HIGH

L = LOW

X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -4.0mA	2.4		V
V _{OL}	LOW Voltage	I _{OL} = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	°C
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	50	pF	V _{IN} ² = 0V
C _{CE}	Chip Enable	20		
C _{WE}	Write Enable	50		
C _{OE}	Output Enable	50		
C _{I/O}	Data Input/Output	30		

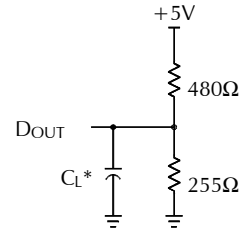
DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-	-20	+20	-20	+20	-20	+20	µA	
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-	-10	+10	-10	+10	-10	+10	µA	
I _{CC}	Operating Supply Current	Cycle=min., Duty=100%, I _{OUT} = 0mA	X8	175		230		245		265	mA
			X16	250		340		350		390	
			X32	400		560		560		640	
I _{SB1}	Full Standby Supply Current (CMOS)	V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V, CE ≥ V _{DD} -0.2V	1.6		20		20		40	mA	
I _{SB2}	Standby Current (TTL)	CE = V _{IH}	100		120		140		140	mA	
I _{DR3}	Data Retention Supply Current (3V)	V _{DR} = 3V, CE ≥ V _{DR} -0.2V	0.28		1.6		2.4		8.0	mA	
I _{DR2}	Data Retention Supply Current (2V)	V _{DR} = 2V, CE ≥ V _{DR} -0.2V	0.14		1.0		1.6		7.2	mA	
V _{OL}	Output Low Voltage	I _{OUT} = 8.0mA	-		0.4		0.4		0.4	V	
V _{OH}	Output High Voltage	I _{OUT} = -4.0mA	-	2.4		2.4		2.4		V	

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

OUTPUT LOAD		
Load	C _L	Parameters Measured
1	30pF	except t _{LZ} , t _{HZ} , t _{OHZ} , t _{OLZ} , and t _{WHZ}
2	5pF	t _{LZ} , t _{HZ} , t _{OHZ} , t _{OLZ} , and t _{WHZ}

Figure 1. Output Load

* Including Probe and Jig Capacitance.



AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE:Over operating ranges													
No.	Symbol	Parameter	20ns**		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t _{AA}	Address Access Time		20		25		30		35		45	ns
3	t _{CO}	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t _{OE}	Output Enable to Output Valid		8		10		15		20		25	ns
5	t _{LZ}	$\overline{CE}$ to Output in LOW-Z ^{4, 5}	3		3		3		3		3		ns
6	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 5}	0		0		0		0		0		ns
7	t _{HZ}	$\overline{CE}$ to Output in HIGH-Z ^{4, 5}		10		12		15		20		25	ns
8	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 5}		8		10		15		20		25	ns
9	t _{OH}	Output Hold from Address Change	3		3		3		3		3		ns

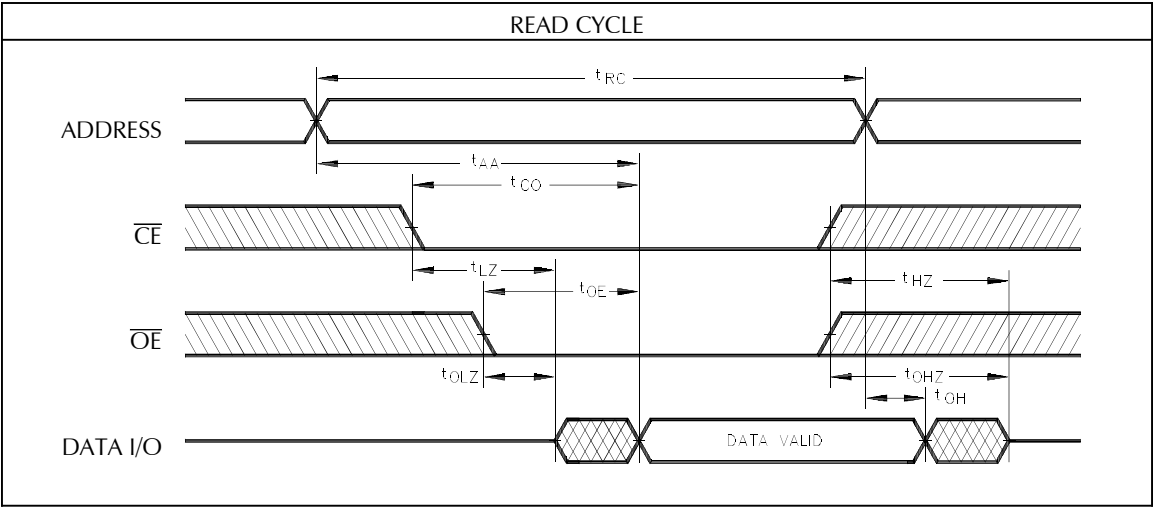
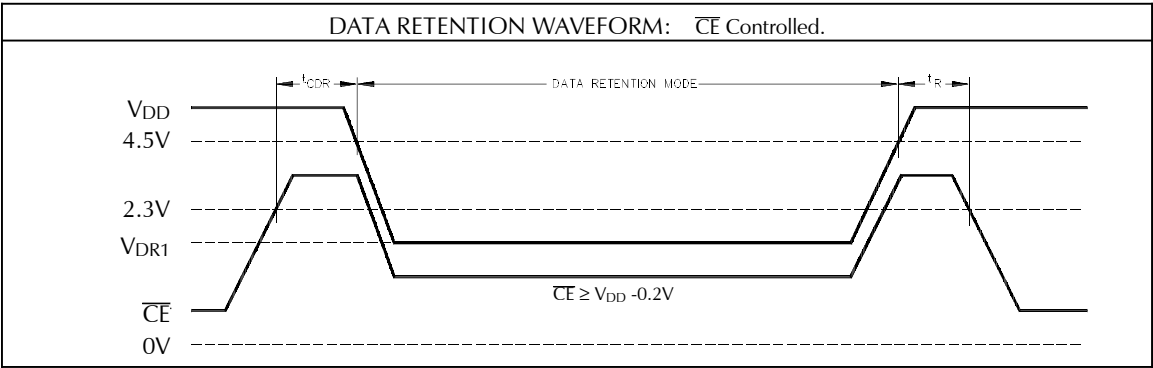
** Available in Commercial Only.

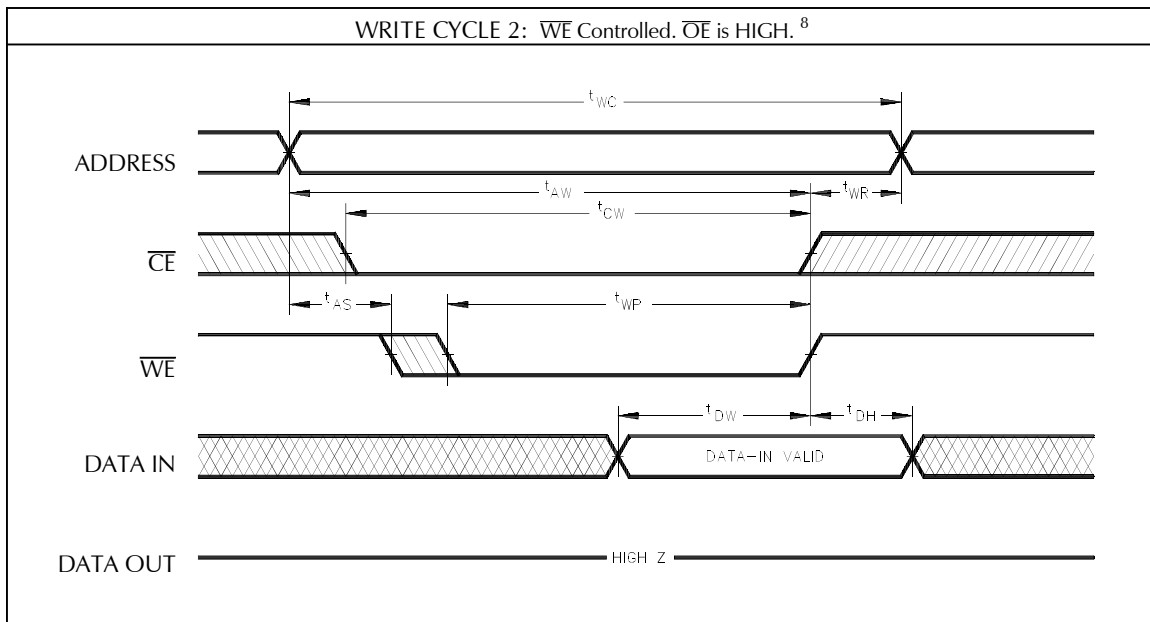
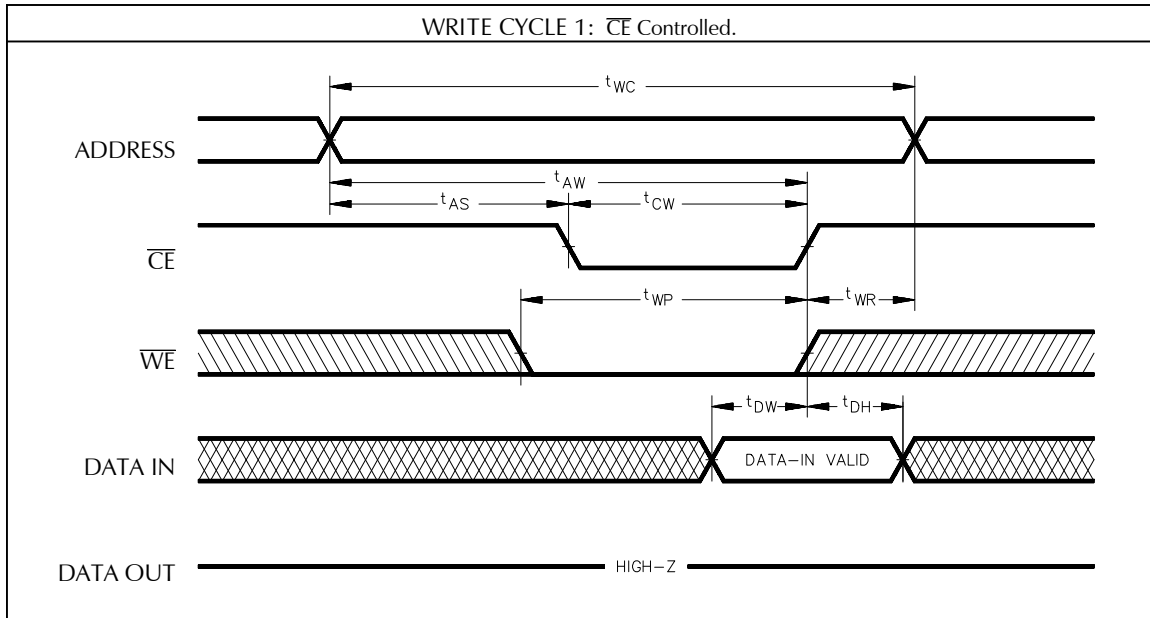
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6, 7} : Over operating ranges													
No.	Symbol	Parameter	20ns**		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	20		25		30		35		45		ns
11	t _{AW}	Address Valid to End of Write	15		20		25		30		40		ns
12	t _{CW}	Chip Enable to End of Write	15		20		25		30		40		ns
13	t _{AS}	Address Set-Up Time ***	0		0		0		0		0		ns
14	t _{WP}	Write Pulse Width	15		20		25		30		35		ns
15	t _{WR}	Write Recovery Time	0		0		0		0		0		ns
16	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 5}		8		10		12		15		20	ns
17	t _{DW}	Data to Write Time Overlap	12		15		15		20		25		ns
18	t _{DH}	Data Hold from Write Time	0		0		0		0		0		ns
19	t _{OW}	Output Active from End of Write	3		3		3		3		3		ns

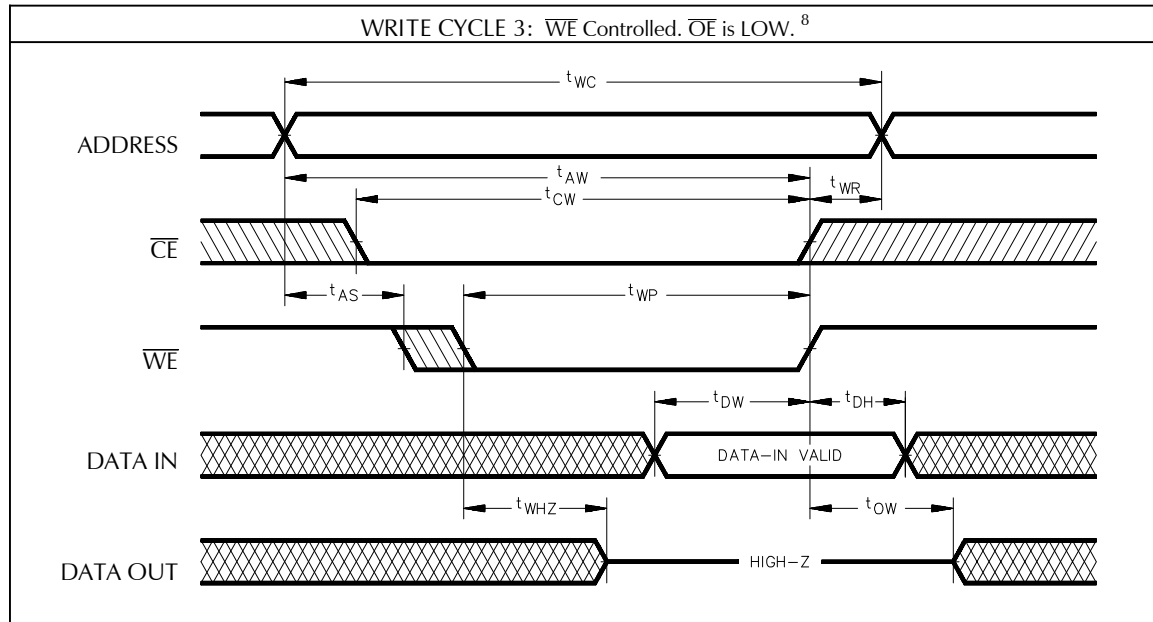
** Available in Commercial Only.

*** Valid for both Read and Write Cycles.

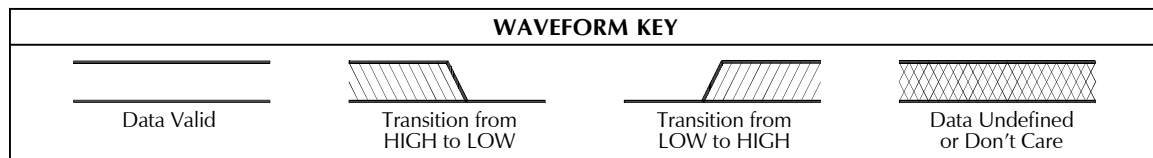
Data Retention AC Characteristics ⁸						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$, $V_{IN} \geq V_{DR} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$	2.0	-	-	V
V _{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t _R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms





**NOTES:**

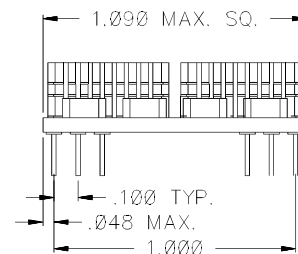
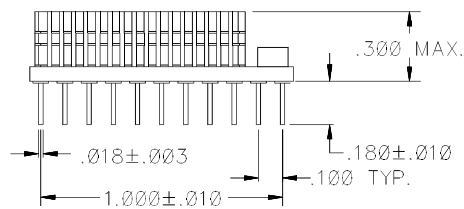
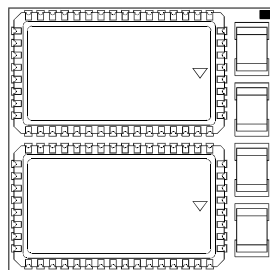
1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of $\pm 500mV$ from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. $\overline{CE}$ and $\overline{WE}$ can initiate and terminate WRITE Cycle.



ORDERING INFORMATION

DP	S128C32B	V3	- XX	X	
PREFIX	DEVICE TYPE	PACKAGE	SPEED	GRADE	
DENSE-PAC					
					C COMMERCIAL 0°C to +70°C
					I INDUSTRIAL -40°C to +85°C
					M MILITARY -55°C to +125°C
					B MIL-PROCESSED -55°C to +125°C
					20 20ns (COMMERCIAL ONLY)
					25 25ns
					30 30ns
					35 35ns
					45 45ns
					66 PIN GRID ARRAY (PGA)/(3-D) VERSA-STACK
					VERY HIGH SPEED CMOS SRAM 128Kx32

MECHANICAL DRAWING

**Dense-Pac Microsystems, Inc.**

7321 Lincoln Way ♦ Garden Grove, California 92841-1431
 (714) 898-0007 (800) 642-4477 (Outside CA) ♦ FAX: (714) 897-1772 ♦ <http://www.dense-pac.com>