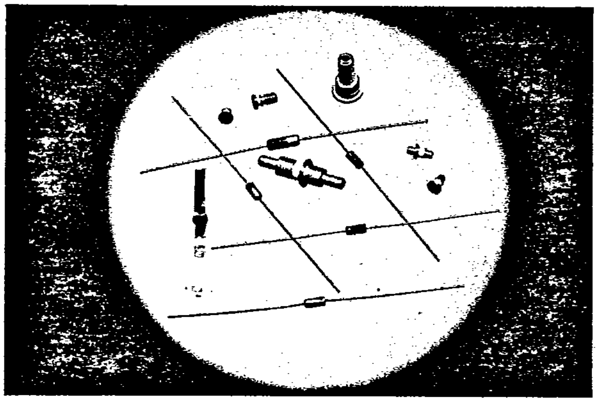


D-1008

PIN/NIP DIODES

SDI MICROWAVE
11 Executive Park Drive
N. Billerica, MA 01862
(617) 667-7700 TLX 95 1592
TWX 710-347-1576

Description

The DP series of PIN diodes and the DN series of NIP diodes are designed to cover a wide range of applications that fall into the general catagories of switching, phase shifting, attenuating and limiting.

With a broad-based product capability and stringent materials control, we can design a diode into your circuit and reliably reproduce it.

Our Sitrox™ passivated diodes are ruggedly constructed using high resistivity epitaxial silicon material. These devices consist typically of a slightly doped layer of semiconducter sandwiched between heavily doped layers of opposite conductivity type (P^+ and N^+ for example) as shown below.

Maximum Ratings

Temperature Range

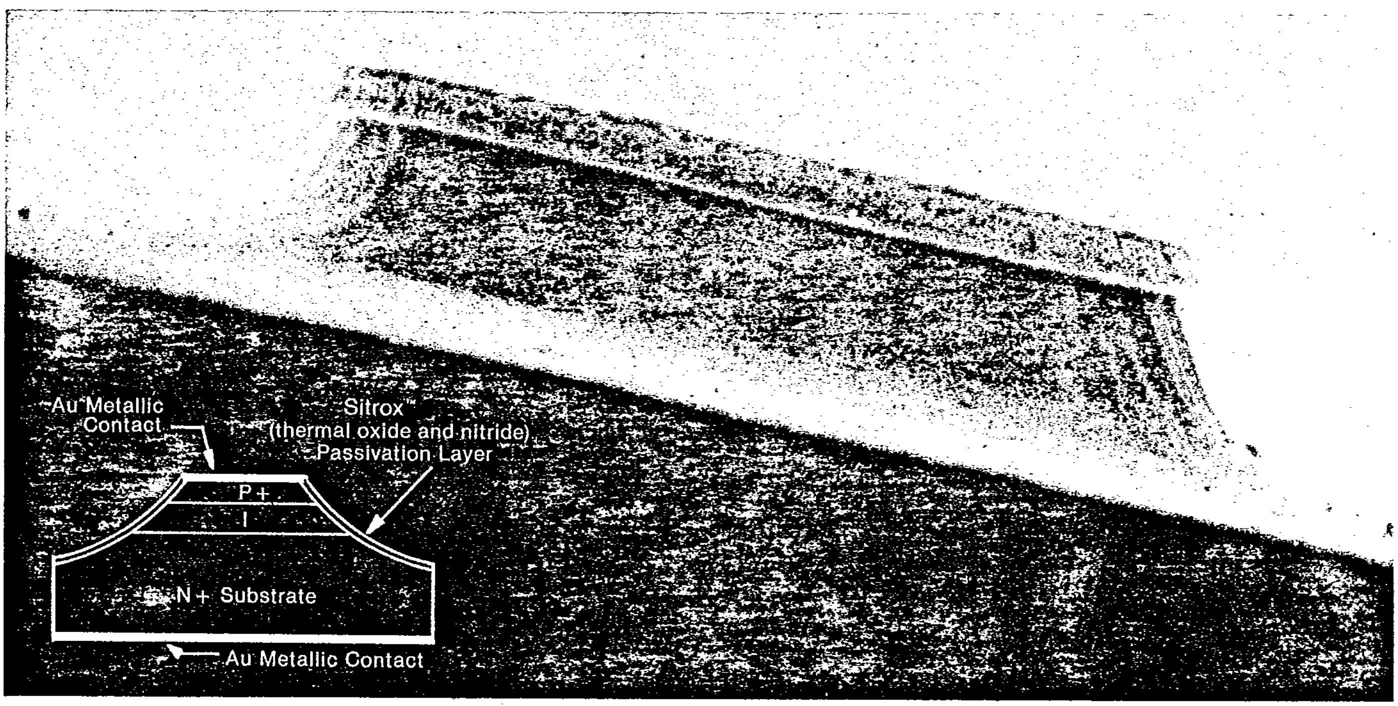
Operating (T_{op})	−65 °C to +175 °C
Storage (T_{st})	−85 °C to +200 °C

Features

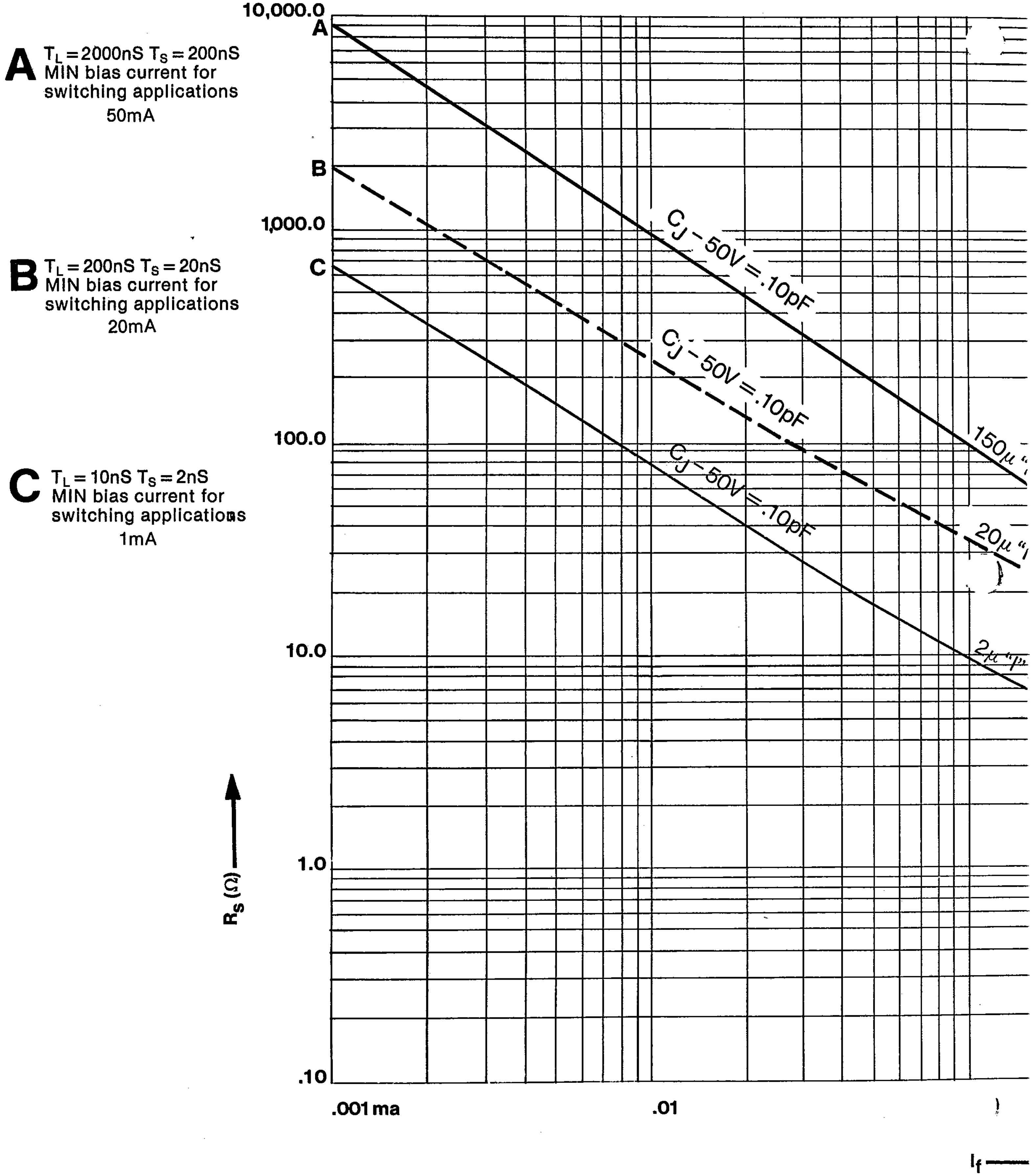
- Widest selection of device types.
- Sitrox™[4] (silicon dioxide and nitride) passivation.
- Complete traceability and lot control is standard for high reproduceability.

Screening Tests

Screening tests equivalent to the most rigorous MIL standards can be provided on request to supplement our standard quality assurance program, see Data page D-6030A. These tests are conducted at our MIL-I-45208A facility in accordance with the latest accepted procedures based on MIL 19500 with methods drawn from MIL-STD-750 and/or your program requirements.

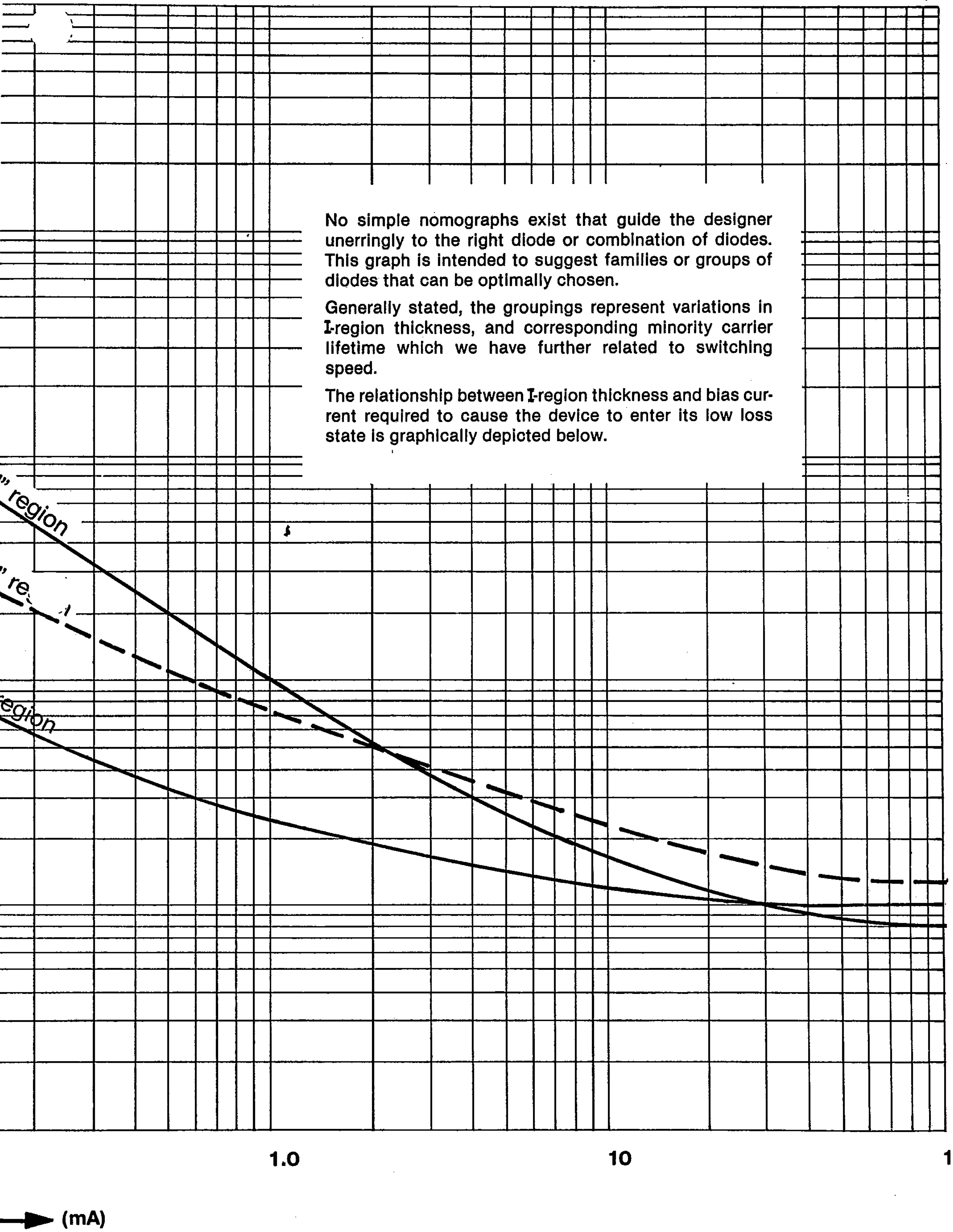


SDI **PIN Sel**



A $T_L = 2000nS$ $T_S = 200nS$ MIN bias current for switching applications 50mA
B $T_L = 200nS$ $T_S = 20nS$ MIN bias current for switching applications 20mA
C $T_L = 10nS$ $T_S = 2nS$ MIN bias current for switching applications 1mA
10,000.0
1,000.0
100.0
10.0
1.0
.10
A
B
C
C_J - 50V = .10pF
C_J - 50V = .10pF
C_J - 50V = .10pF
150μ
20μ
2μ
R_S (Ω)
.001 ma
.01
I_f

ection Guide



No simple nomographs exist that guide the designer unerringly to the right diode or combination of diodes. This graph is intended to suggest families or groups of diodes that can be optimally chosen.

Generally stated, the groupings represent variations in I-region thickness, and corresponding minority carrier lifetime which we have further related to switching speed.

The relationship between I-region thickness and bias current required to cause the device to enter its low loss state is graphically depicted below.

Specifications*

PART NUMBER		V_B, Min. @10μA (V)	C_{J-6} Max (1) (pF)	R_S Max. (2) @20mA (Ω)	R_s (Ω)	T_L Typ. (3) (nS)	T_S (4) 10-90% (nS)	T_S (4) 90-10% (nS)	Θ_{JC} Max. (5) (°C/W)
Ultra Fast Switching Diodes									
DP0300		30	.15	1.5		10	1	5	40
DP0301		30	.20	1.2		10	1	5	40
DP0302		30	.25	1.0		10	1	5	35

Ultra Low-Loss Diodes		V_B	C_{J-10} Max.	R_S Typ. @1mA	R_S Max. @100mA	T_L	T_S	Θ_{JC}
DP0600		60	.06 - .12	2.0	1.0	40	2	65
DP0601		60	.12 - .15	1.75	.6	40	2	55
DP0602		60	.15 - .20	1.5	.5	40	2	45

Fast Switching Diodes		V_B	C_J	R_S Typ. @20mA	R_s	T_L	T_S	Θ_{JC}
DP0700A	DN0700A	70	.05	2.8	2.5	50	5	60
DP0700	DN0700	70	.10	2.0	1.8	50	5	60
DP0701	DN0701	70	.20	1.7	1.5	50	5	50
DP0702	DN0702	70	.30	1.2	1.0	50	5	50
DP1000A	DN1000A	100	.05	2.6	2.0	100	10	50
DP1000	DN1000	100	.10	2.0	1.7	100	10	45
DP1001	DN1001	100	.20	1.5	1.2	100	10	45
DP1002	DN1002	100	.30	1.2	1.0	100	10	40
DP2000	DN2000	200	.10	2.4	1.8	200	20	40
DP2001	DN2001	200	.20	1.4	.9	200	20	35
DP2002	DN2002	200	.30	1.0	.8	200	20	35

Precision Attenuator (6) Diodes	V_B	C_{J-50} Typ.	R_S Min. @.01mA	R_S Typ. @20mA	R_S Max (7) @100mA	T_L Min.	Θ_{JC}
DP1501	150	.06	1000	2.5	2.0	500	25
DP1502	150	.10	600	2.0	1.5	500	20
DP1503	150	.15	500	1.7	1.2	500	15
DP1504	150	.20	400	1.5	1.0	500	12
DP1505	150	.25	350	1.2	.8	500	10
DP1506	150	.30	300	1.0	.6	500	9

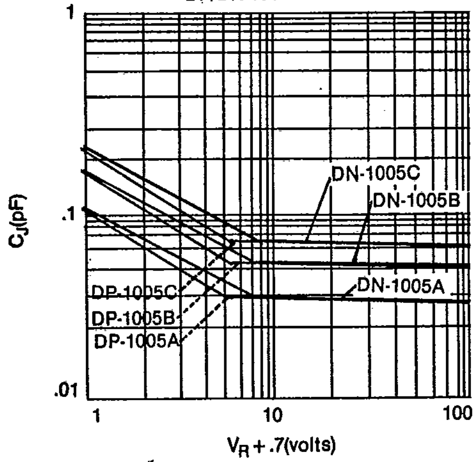
SPIN and SNIP Diodes (8)		V_B	C_{J-10} Max.	R_S Max @20mA	R_S Max. @100mA	T_L	T_S 10-90%	T_S 90-10%	Θ_{JC}
DP1005A	DN1005A	100	.03	3.5	1.8	250	10	50	70
DP1005B	DN1005B	100	.05	2.5	1.5	250	10	50	60
DP1005C	DN1005C	100	.06	1.8	1.2	250	10	50	60
DP1005D	DN1005D	100	.06	1.2	.9	250	10	50	60

Medium Power Switching Diodes		V_B	C_{J-50} Max.	R_S Typ. @20mA	R_S Max. @100mA	T_L Min.	T_S	Θ_{JC}
DP3000A		300	.05	3.5	1.7	600	300	25
	DN3000A	300	.05	3.0	1.7	900	450	25
DP3000		300	.10	2.0	1.2	800	400	20
	DN3000	300	.10	2.0	1.2	1000	500	20
DP3001		300	.30	1.5	.6	1000	500	12
	DN3001	300	.30	1.5	.6	1200	600	12
DP3002		300	.50	1.0	.5	1000	500	10
	DN3002	300	.50	1.0	.5	1200	600	10
DP5000		500	.10	2.0	1.2	1200	600	18
	DN5000	500	.10	2.0	1.2	1500	750	18
DP5001		500	.30	1.5	.6	1200	600	10
	DN5001	500	.30	1.5	.6	1500	750	10
DP5002		500	.50	1.0	.5	1200	600	9
	DN5002	500	.50	1.0	.5	1500	750	9

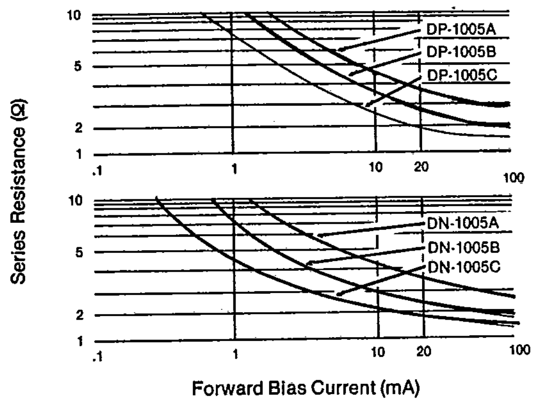
* @ 25°C

(1) Junction capacitance (C_j) is the capacitance of the diode junction not including the package capacitance (C_p). $C_j + C_p = C_t$. Measured on a Boonton capacitance bridge model 75-D or automatic bridge 76-A at 1Mhz
(2) Measured using transmission loss techniques at 1Ghz
(3) $I_F = 10mA$, $I_R = 6mA$, Input pulse is greater than 1nS. Tektronix scope type 564
(4) Refer to data sheet D-1101 or D-2011. Driver outputs = −30mA and +4V, 150 mA spike, with rise time of 10nS.
(5) As measured using ΔV_F vs time in a Sage Theta 100A™ thermal impedance meter — infinite heat sink.
(6) Catagorized by R_S vs I_F
(7) R_S measured at 100Mhz using HP vector impedance meter 4815A.
(8) Supplied with ribbon or wire leads attached - epoxy cap optional - for Series use.
(9) General purpose switching diodes - separate brochure available.

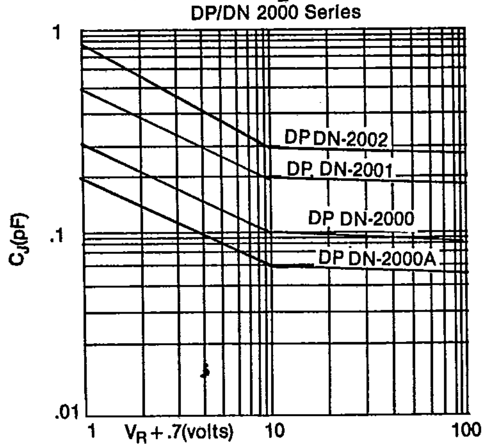
Capacitance/Voltage Characteristics
DP/DN-1005 Series



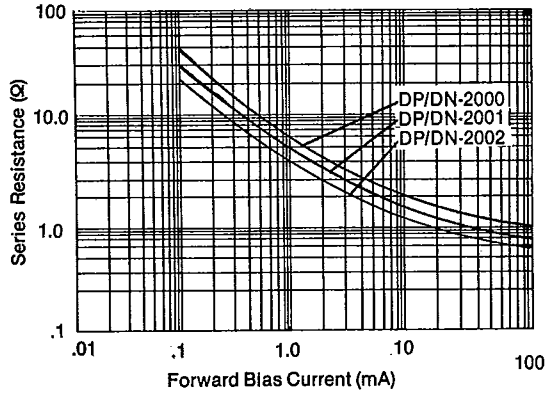
R_S vs. I_F Characteristics



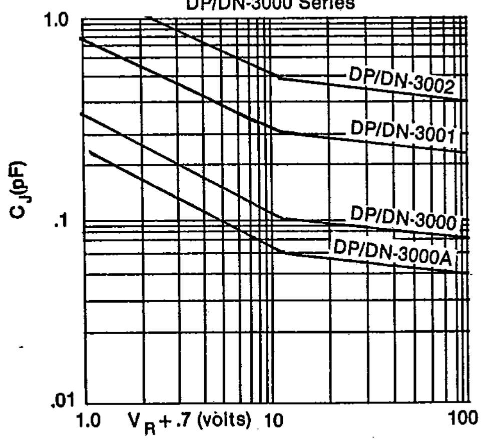
Capacitance/Voltage Characteristics
DP/DN 2000 Series



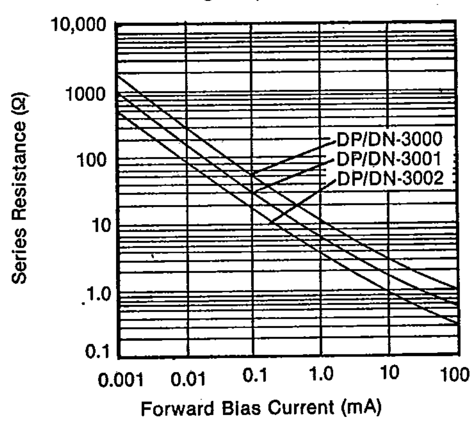
R_S vs. I_F Characteristics



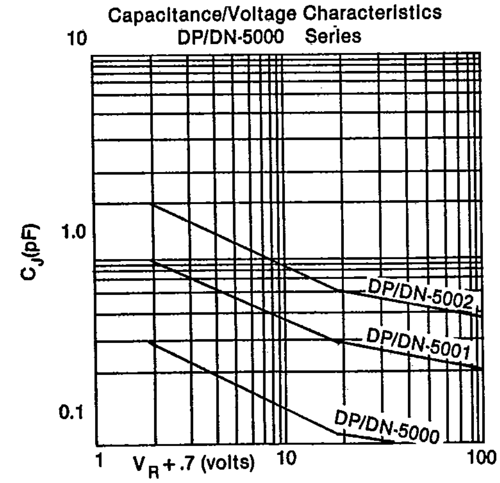
Capacitance/Voltage Characteristics
DP/DN-3000 Series



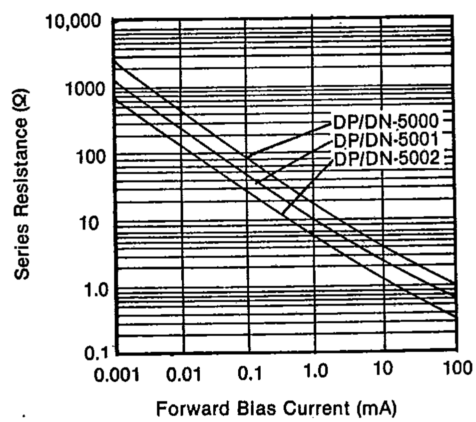
R_S vs. I_F Characteristics



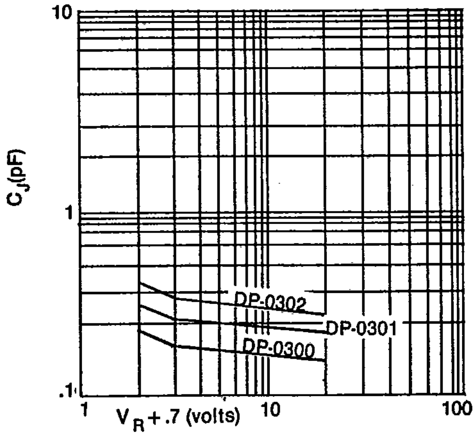
Capacitance/Voltage Characteristics
DP/DN-5000 Series



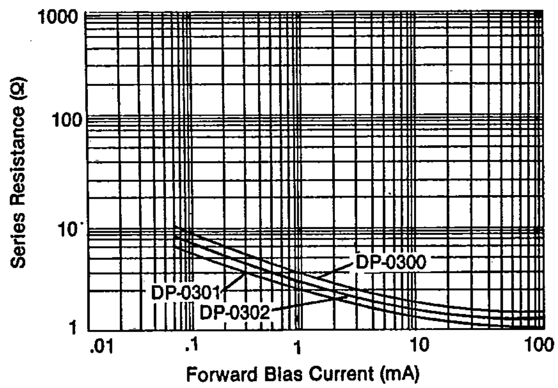
R_S vs. I_F Characteristics



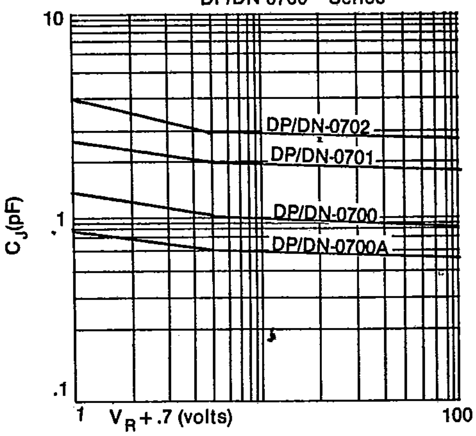
Capacitance/Voltage Characteristics
DP-0300 Series



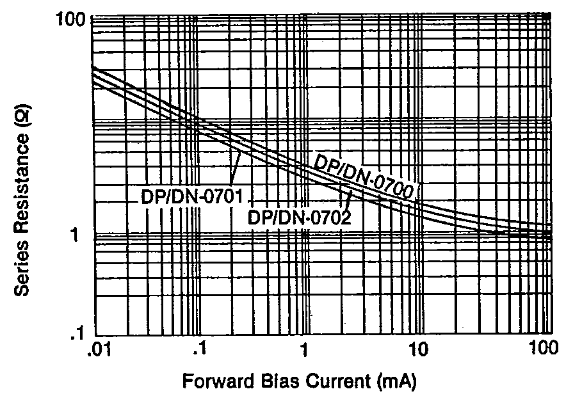
R_S vs I_F Characteristics



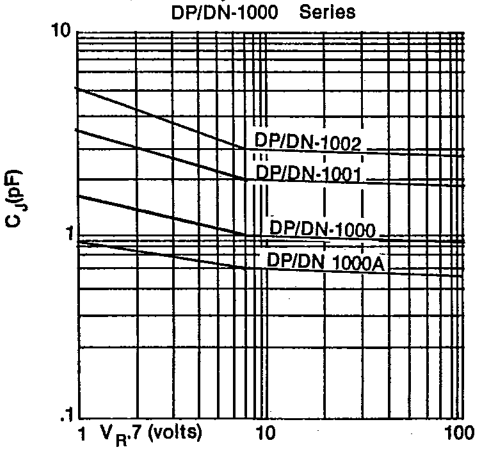
Capacitance/Voltage Characteristics
DP/DN 0700 Series



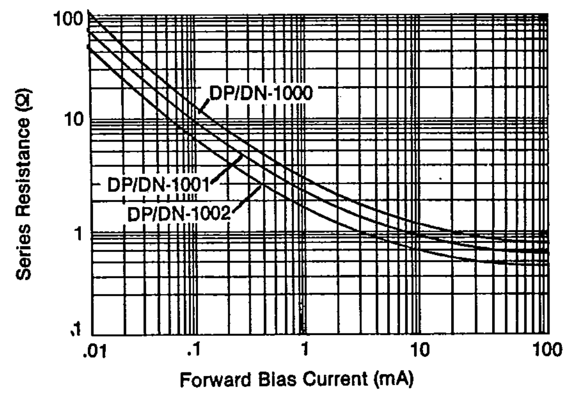
R_S vs I_F Characteristics



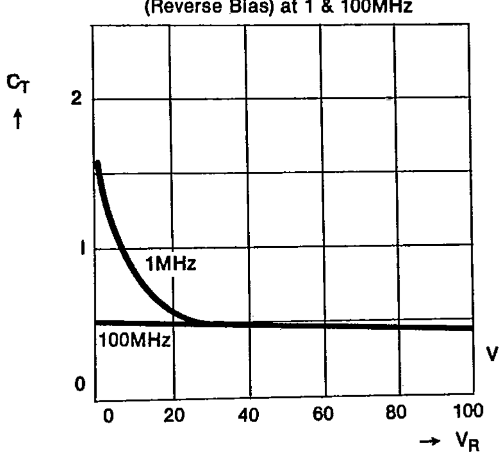
Capacitance/Voltage Characteristics
DP/DN-1000 Series



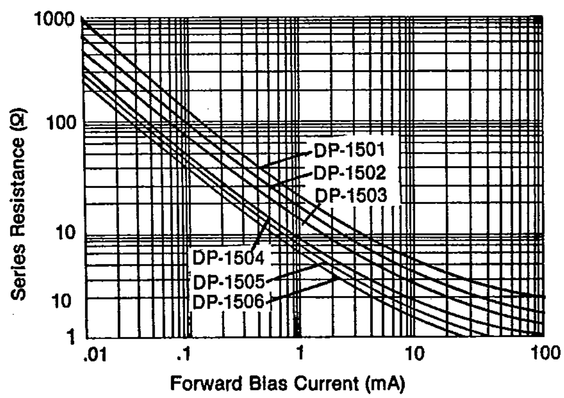
R_S vs I_F Characteristics



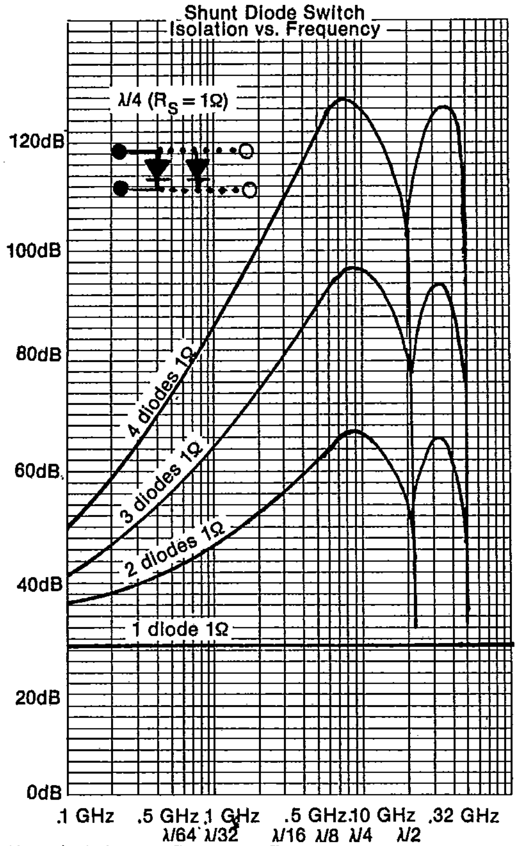
Typical Capacitance vs. V_R
(Reverse Bias) at 1 & 100MHz



R_S vs I_F Characteristics

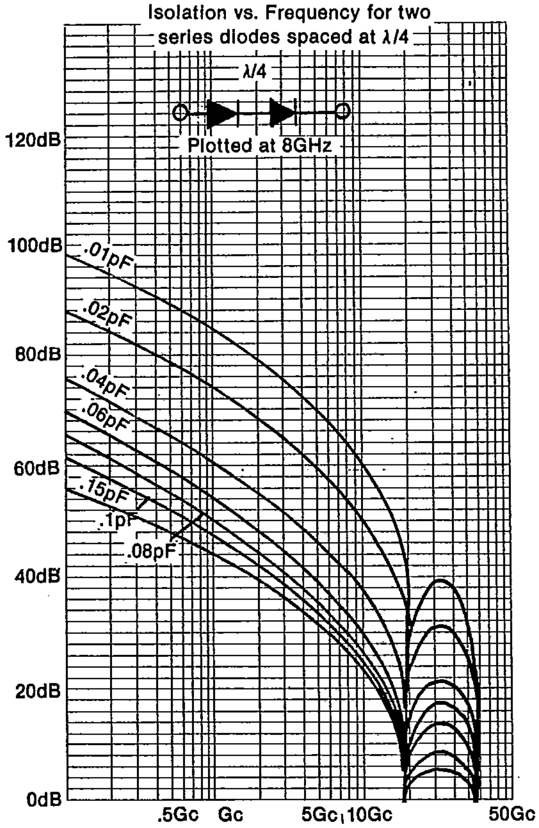


Isolation vs. Diode Spacing

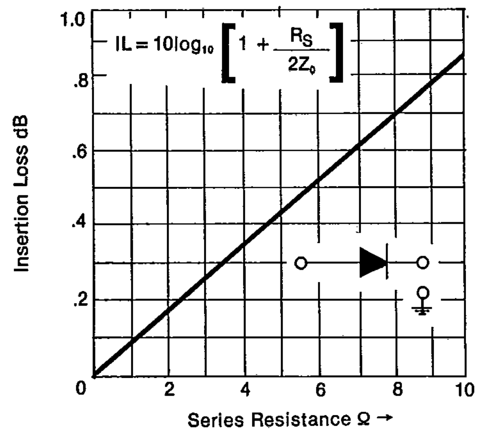


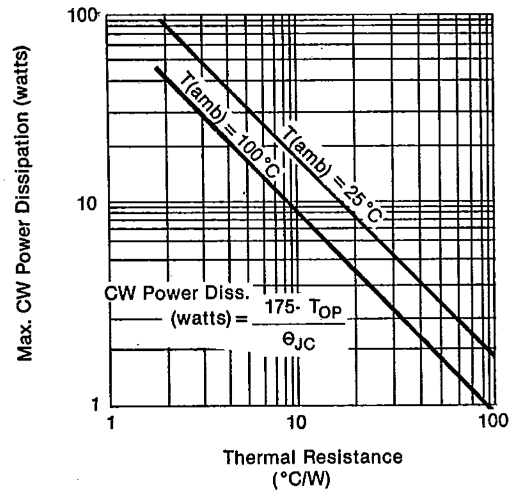
Note: Isolation vs. Frequency. These curves represent a group of /4 attenuators optimized at 8GHz using diodes with R_S = 1 (80% saturation).

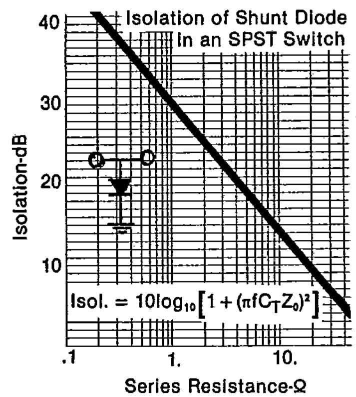
Isolation vs. Diode Spacing. These curves represent the change in isolation at a fixed 8GHz when the spacing of the diodes is varied.

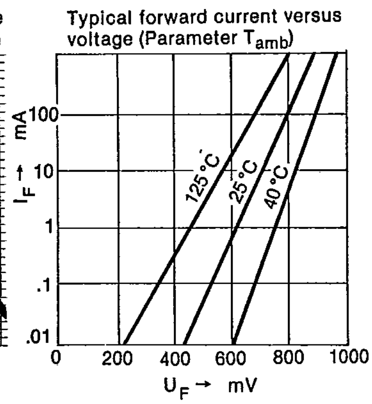


Insertion Loss Vs. Series Resistance

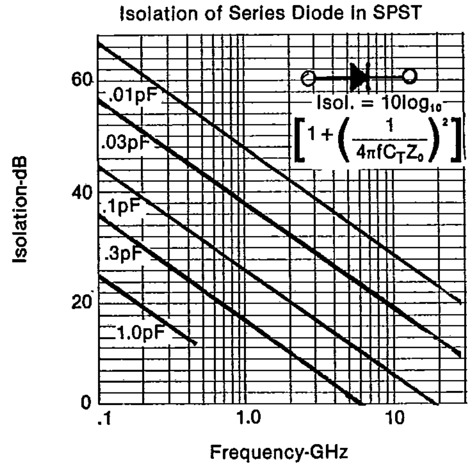








Isolation of Series Diode in SPST

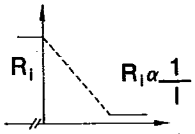


Description (cont.)

The lightly doped "intrinsic" region may physically be of "P" or "N" type material. Metallic contact layers are formed on the outside surface of the P^+ and N^+ layers.

The resistance of the "intrinsic" region material depends primarily on the number of free carriers injected into it from the P^+ and N^+ layers. When there are no injected carriers (i.e., no forward conduction current, I_F), the I-region resistance (R_I) is high. When I_F>10mA, R_I< 1 ohm.

Variable Resistance Characteristics



The resistance and capacitance of the I-region depends on the relationship of the lifetime of injected carriers to the period of the rf current. Lifetime (T_L) determines the minimum useful frequency of a PIN. At low frequencies, where $f \ll T_L$, the PIN behaves as a rectifying element.

At microwave frequencies, $f \gg 1/T_L$ and the PIN rectifies very weakly. Relatively small dc bias current can control very large rf currents. The PIN behaves as a current controlled microwave resistor, due to I-region conductivity modulation.

Conductivity modulation can be produced by:

dc controlled carrier injection, or
rf controlled carrier injection

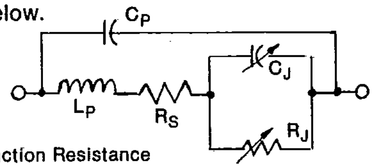
Thus sufficiently high microwave power can modulate R_I. The rule of thumb is:

$$(I_{RF})\left[\frac{1}{2f_{rf}}\right] \ll I_{DC}T_L$$

meaning that the charge stored in the I-region due to dc bias must be much larger than the charge injected by the rf current. Then the PIN behaves as a non-rectifying microwave resistor.

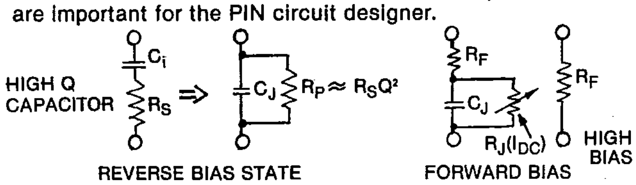
PIN Junction Equivalent Circuit

The general equivalent circuit, useful in conceptualizing PIN junction behavior is shown below.



C_P = Package Capacitance
L_P = Package Inductance
C_J = Junction Capacitance
R_S = Parasitic Series Resistance
R_J = Conductivity Modulated Junction Resistance

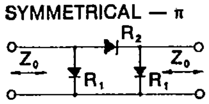
In the reverse biased state, the PIN is a fairly high Q capacitor, whereas in the forward biased state, it is a current controlled resistor, R_S (1) is the single most important parameter of the PIN, and the families of curves are given on the individual PIN data sheets. The forward and reverse biased equivalent circuits are important for the PIN circuit designer.



Attenuators

Attenuation level vs. Bias Current

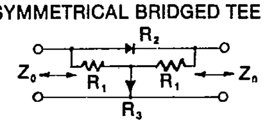
SYMMETRICAL — π



$$R_1 = Z_0\left(\frac{K+1}{K-1}\right)$$

$$R_2 = \frac{Z_0}{2}\left(K - \frac{1}{K}\right)$$

SYMMETRICAL BRIDGED TEE



$$R_1 = Z_0$$

$$R_2 = Z_0(K-1),\ R_3 = \frac{Z_0}{K-1}$$

Based on the forward R_S (1) characteristic of the PIN, two typical attenuator circuits and their design equations are shown. K is the voltage transfer ratio (V_{IN}/V_{OUT}) and Z_0 is the impedance of the source, the load, and their associated transmission lines.

Typical applications of attenuator diodes require linearization of the attenuator circuit power transfer with respect to attenuation level, incident power level and bandwidth. The first two are driver design problems. Frequency response depends on choosing an adequately long lifetime diode so that it does not become nonlinear (start to rectify) at the lower end of the band. Nonlinear distortion is observed as harmonic generation, cross-modulation and intermodulation distortion.

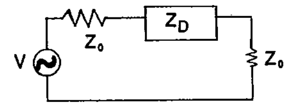
Applications

In specifying a PIN/NIP our applications department will assist you in selecting the proper parameters, thus eliminating the "trial and error" approach.

Series or Shunt Diode Mounting

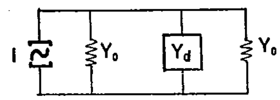
The PIN diode can be mounted either in series with the transmission line or in shunt, and there are certain tradeoffs in switch performance parameters. The PIN equivalent circuit can be reduced to simple series or shunt form, depending on the bias state and frequency. Attenuation between the generator and the load, due to the presence of Z_d (or Y_d) is given by:

Series Diode



$$\alpha = 10\log\frac{P_I}{P_T} = 10\log\left\{\frac{\left(\frac{R_D}{Z_0}+2\right)^2 + \left(\frac{X_D}{Z_0}\right)^2}{4}\right\}$$

Shunt Diode



$$\alpha = 10\log\frac{P_I}{P_T} = 10\log\left\{\frac{\left(\frac{G_D}{Y_0}+2\right)^2 + \left(\frac{B_D}{Y_0}\right)^2}{4}\right\}$$

These equations for attenuation (α) are necessary and sufficient to determine insertion loss, isolation and bandwidth.

At higher microwave frequencies where package parasitics can't be ignored, the packaged device must be analyzed as a resonant circuit to achieve high impedance in the reverse biased state. For average power and peak power, we have

$$P_{av} = \frac{P_D Z_0}{R_S}\left(\frac{1+R_S}{2Z_0}\right)^2 \qquad \frac{P_D Z_0}{4R_S}\left(\frac{1+2R_S}{Z_0}\right)^2$$

$$P_{peak} = \frac{V_B^2}{32Z_0} \qquad \frac{V_B}{8Z_0}$$

P_D is the average power that can be dissipated in the PIN, based on thermal resistance (θ) calculations.

Design Information

All PIN applications need the following as minimum information.

Frequency and Bandwidth
Power Handling (Peak & Average)
Bias Available

Switching

In switch and phase shifter applications, the PIN is either heavily forward biased or highly reverse biased. Switch design parameters are isolation, insertion loss and switching time (t_{rf} and t_{fr}). These design parameters are related to minimum R_S obtainable at the specified driver current and the resistance ratio between the forward and reverse biased states. Switching time is related to amount of stored charge due to the biasing current, the carrier lifetime, and the reverse bias pulse circuit design. Values of I_F, V_R and transmission line Z_0 are chosen so that excessive rf power is not dissipated in the PIN during the switching cycle. Although the PIN may withstand the rf power at bias states I_F and V_R, the PIN can pass through an impedance level ($Z_d \approx Z_0$) during the transition between switching states, that allows it to absorb power. If this switching time is too slow, the diode will heat up, causing it to fail.

For Switches

Series, Shunt or combination?
Isolation
Insertion Loss
VSWR
Speed

For Phase Shifters

Diode matching tolerances

For Limiters

Limiting threshold (flat leakage)
Spike leakage

Limiters are more thoroughly covered on data sheets D-1012and in the solid state section.