SEEQ®
Technology, Incorporated

2817A/2817AH
5517A/5517AH
Timer E^2
16K Electrically Erasable PROMs

August 1992

Features

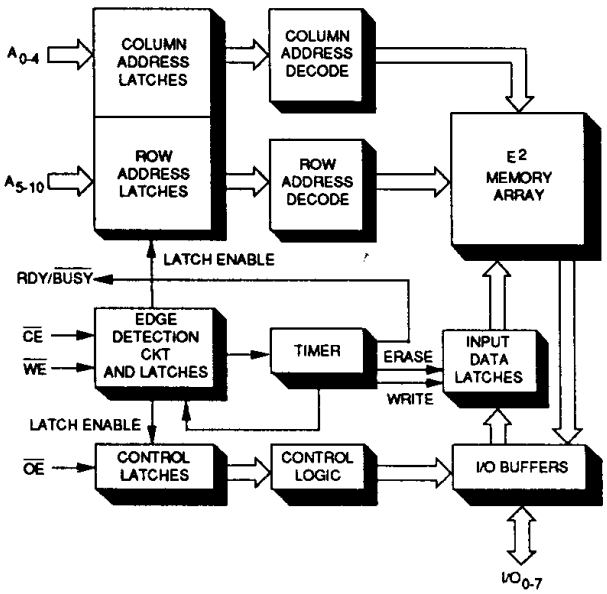
- **Military Extended and Commercial Temperature Range**
  - −55° C to +125° C Operation (Military)
  - −40° C to +85° C Operation (Extended)
  - 0° C to +70° C Operation (Commercial)
- **End of Write Detection**
  - Read $\overline{\text{Busy}}$ Pin
  - Optional $\overline{\text{DATA}}$ Polling Feature
- **High Endurance, Write Cycles**
  - 2817A: 10,000 Cycles/Byte Minimum
  - 5517A: 100K, 400K and 1 Million Cycles/Byte
- **On-Chip Timer**
  - Automatic Byte Erase Before Byte Write
- **5 V± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **150 ns max. Access Time**
- **Low Power Operation**
  - 100 mA Active Current
  - 40 mA Standby Current
- **JEDEC Approved Byte-Wide Pinout**
- **MIL-STD-883 Class B Compliant**

Description

SEEQ's 2817A/5517A are 5V only, 2K x 8 electrically erasable programmable read only memory (EEPROM). They are packaged in 28 pin ceramic DIP and plastic DIP packages and a 32 pin leaded chip carrier, all with a ready/$\overline{\text{busy}}$ pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times which a byte may be written, is 10 thousand (K) cycles for the 2817A or 100K, 400K or 1 million cycles for the 5517A.

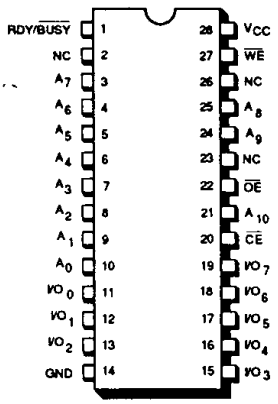
The 2817A has an internal timer that automatically times out the write time. The on-chip timer, along with the input

Block Diagram

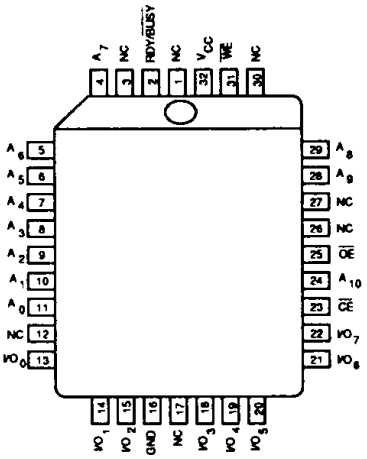


Pin Configuration

DUAL-IN-LINE TOP VIEW



PLASTIC LEADED CHIP CARRIER TOP VIEW



Pin Names

A_0-A_4	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_5-A_{10}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
RDY/$\overline{BUSY}$	DEVICE READY/$\overline{BUSY}$
NC	NO CONNECT

latches, frees the microcomputer system for other tasks during the write time. The standard 2817A/5517A write cycle time is 10 ms over the recommended range, while the 2817AH/5517AH is a fast 2ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for 10 years.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode[1], only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3KΩ pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied 2817A RDY/$\overline{BUSY}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X X	V_{IL} X	X V_{IH}	High Z/D_{OUT} High Z/D_{OUT}	High Z High Z

X: any TTL level

$\overline{DATA}$ Polling (Optional Feature)

$\overline{DATA}$ polling is a method of minimizing write times by determining the actual end-point of a write cycle. If a read is performed to any address while the device is still writing, it will present the ones-complement of the last byte written. When the device has completed its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. Timing for a $\overline{DATA}$ polling read is the same as a normal read.

"COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		2817A/2817AH-150 5517A/5517AH-150	2817A/2817AH-200 5517A/5517AH-200	2817A/2817AH-250 5517A/5517AH-250	2817A/2817AH-300 5517A/5517AH-300
Temperature Range	Commercial	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
	Extended	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C
	Military	–55°C to +125°C	—	–55°C to +125°C	–55°C to +125°C
V_{CC} Supply Voltage		5V±10%	5V±10%	5V±10%	5V±10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance 2817A	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
	5517A	100,000 400,000 1,000,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1033

Notes:
1. Chip Erase is an optional mode.
2. Characterized. Not tested.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... −65°C to +150°C
Under Bias
Military/Extended ..... −65°C to +135°C
Commercial ..... −10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground ..... +6.0 V to −0.5 V
Undershoot/Overshoot pulse of less then 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... (undershoot) −1.0 V
(overshoot) + 7.0 V

Power Up/Down Considerations

The 2817A/5517A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.[2]*
2. *A negative Write Enable ($\overline{WE}$) transition has not occured with V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than specified for a byte write in the Mode Selection table.

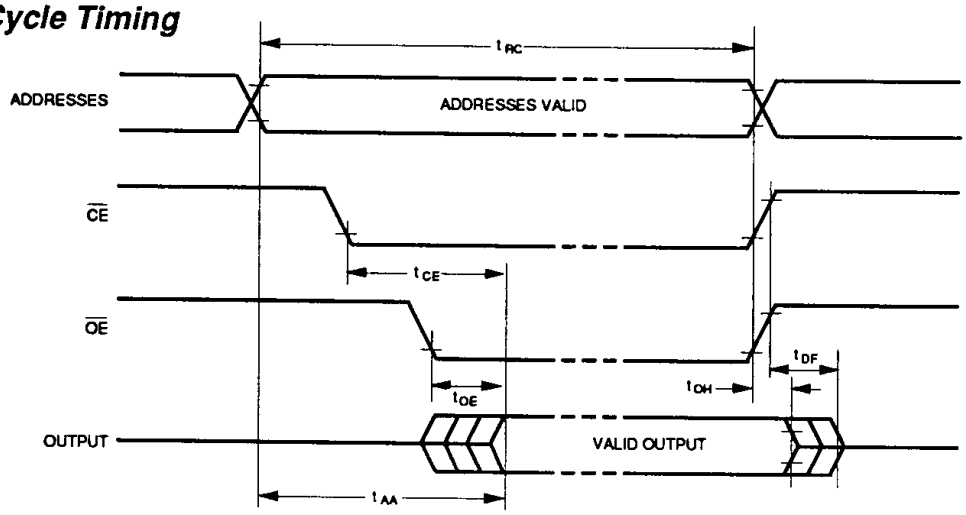
D.C. Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		100	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 5.5 V
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = 5.5 V
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA

A.C. Characteristics *Read Operation* (Over the operating V_{CC} and temperature range)

		Limits									
		2817A/ 2817AH-150 5517A/ 5517AH-150		2817A/ 2817AH-200 5517A/ 5517AH-200		2817A/ 2817AH-250 5517A/ 5517AH-250		2817A/ 2817AH-300 5517A/ 5517AH-300			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	150		200		250		300		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	Chip Enable Access Time		150		200		250		300	ns	$\overline{OE}$ = V_{IL}
t_{AA}	Address Access Time		150		200		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{OE}	Output Enable Access Time		70		90		90		100	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output Enable High to Output Not being Driven		50		60		60		60	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		0		ns	$\overline{CE}$ or $\overline{OE}$ = V_{IL}

Read Cycle Timing



AC Characteristics

Write Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits								Units
		2817A/ 2817AH-150 5517A/ 5517AH-150		2817A/ 2817AH-200 5517A/ 5517AH-200		2817A/ 2817AH-250 5517A/ 5517AH-250		2817A/ 2817AH-300 5517A/ 5517AH-300		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address to Write Set Up Time	10		10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	10		10		10		10		ns
t_{WP}[2]	$\overline{WE}$ Write Pulse Width	100		120		150		150		ns
t_{AH}	Address Hold Time	70		50		50		50		ns
t_{DS}	Data Set Up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		50		ns
t_{DV}[3]	Data Valid Time		1		1		1		1	µs
t_{DB}	Time to Device Busy		120		120		120		120	ns
t_{WR}	Write Recovery Time Before Read Cycle		10		10		10		10	µs
t_{WC}	Byte Write Cycle Time									
	2817A/5517A		10		10		10		10	ms
	2817AH/5517AH		2		2		2		2	ms

NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 µs maximum after the initiation of a write cycle.

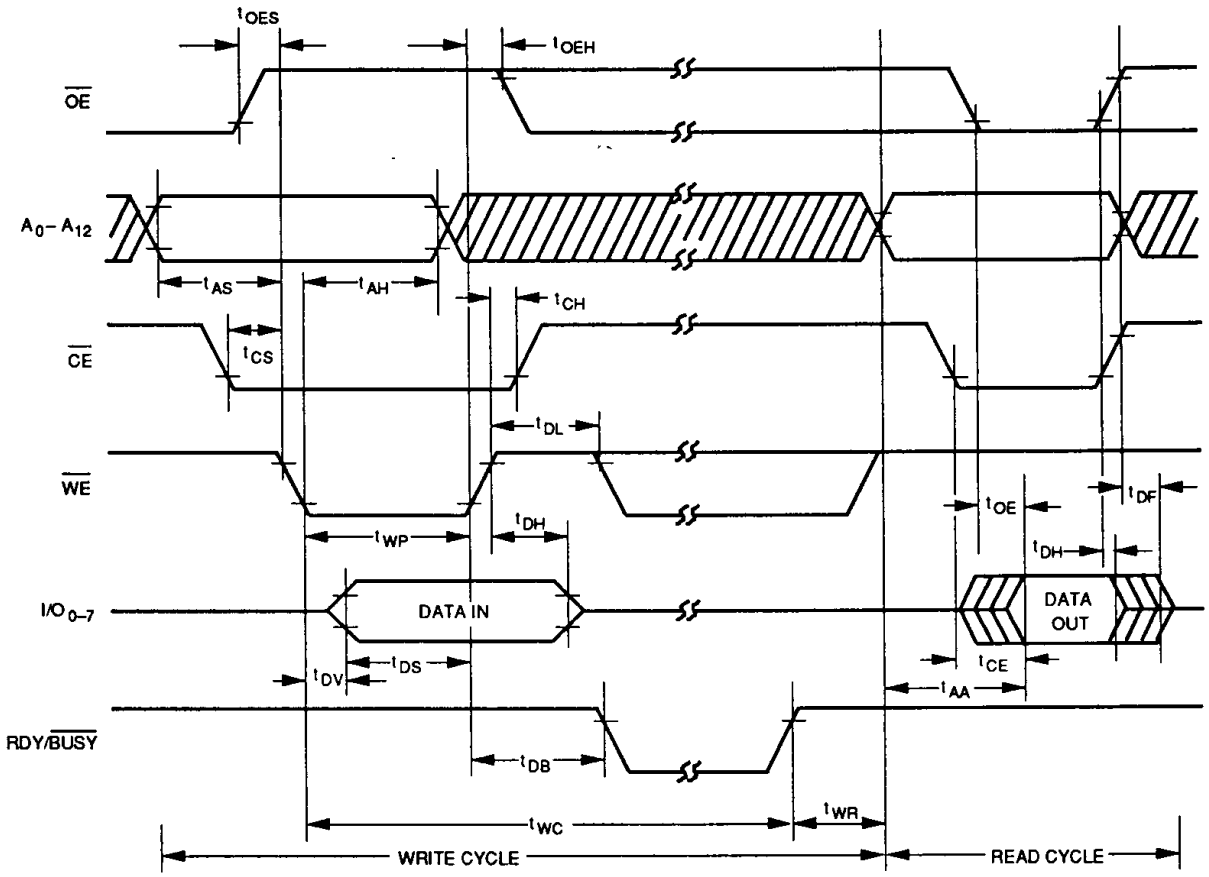
A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: < 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Capacitance [1] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O}$ = 0 V

Write Cycle Timing



Ordering Information