SEEQ®
Technology, Incorporated

2864/2864H

Timer E^2
64K Electrically Erasable PROMs

August 1992

Features

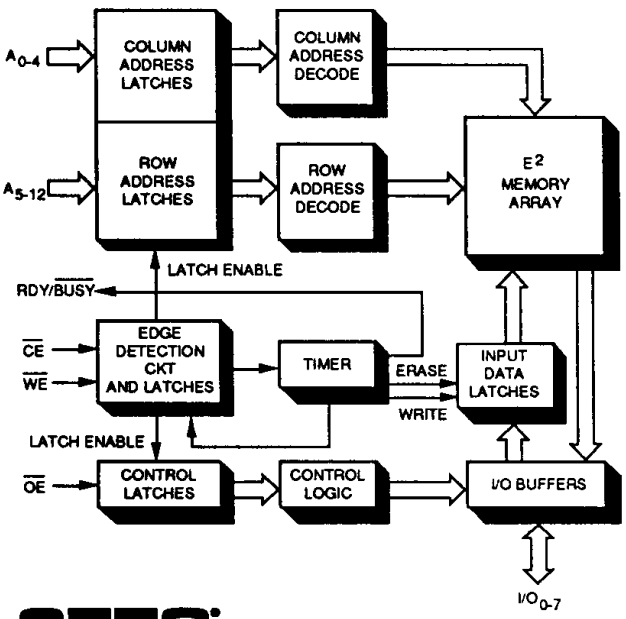
- **Military, Extended and Commercial Temperature Range**
  - –55°C to +125°C Operation (Military)
  - –40°C to +85°C Operation (Extended)
  - 0°C to +70°C Operation (Commercial)
- **End of Write Detection**
  - Ready/$\overline{\text{Busy}}$ Pin
  - Optional $\overline{\text{DATA}}$ Polling Feature
- **High Endurance Write Cycles**
  - 10,000 Cycles/Byte Minimum
- **On-Chip Timer**
  - Automatic Byte Erase Before Byte Write
  - 2 ms Byte Write (2864H)
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **200 ns max. Access Time**
- **MIL-STD-883 Class B Compliant**
  SMD 5962 Compliant

Description

SEEQ's 2864 is a 5 V only, 8K x 8 NMOS electrically erasable programmable read only memory (EEPROM). It is packaged in most popular thru hole and surface mount packages and has a ready/$\overline{\text{busy}}$ pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is a minimum of 10 thousand cycles.

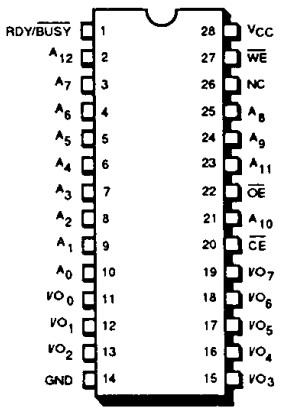
The EEPROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, the 2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has

Block Diagram

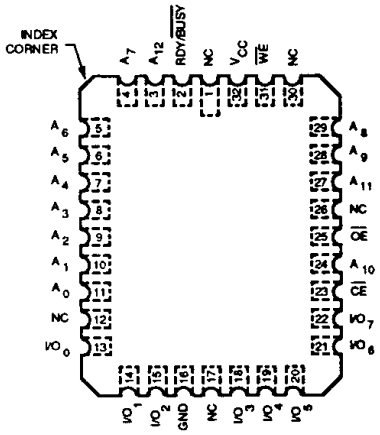


Pin Configuration

DUAL-IN-LINE
TOP VIEW



LEADLESS CHIP CARRIER
TOP VIEW



NOTE: The PLCC has the same pin configuration as the LCC except pins 1 and 17 are don't connects.

Pin Names

A_0-A_4	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_5-A_{12}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
NC	NO CONNECT

been written, the ready/$\overline{busy}$ pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

These two timer EEPROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a 10 ms/2ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins. If RDY/$\overline{BUSY}$ is not used it can be left unconnected.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)	RDY/$\overline{BUSY}$ (1)*
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X X	V_{IL} X	X V_{IH}	High Z/D_{OUT} High Z/D_{OUT}	High Z High Z

*Pin 1 has an open drain output and requires an external 3K resistor to V_{CC}. The resistor value is depent the number of OR-tied RDY/$\overline{BUSY}$ pins.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

$\overline{DATA}$ Polling (Optional Feature)

$\overline{DATA}$ polling is a method of minimizing write times by determining the actual end-point of a write cycle. If a read performed to any address while the device is still writing, it will present the ones-complement of the last byte written. When the device has completed its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.

A $\overline{DATA}$ polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. $\overline{DATA}$ polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a $\overline{DATA}$ polling read is the same as a normal read.

Recommended Operating Conditions

		2864/2864H-200	2864/2864H-250	2864/2864H-300
Temperature Range	Commercial	0°C to +70°C	0°C to +70°C	0°C to +70°C
	Extended	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C
	Military	–55°C to +125°C	–55°C to +125°C	–55°C to +125°C
V_{CC} Supply Voltage		5V±10%	5V±10%	5V±10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

NOTE: 1. Characterized. Not tested.

Power Up/Down Considerations

The 2864 has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable ($\overline{WE}$) transition has not occured when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Absolute Maximum Stress Ratings*

Temperature
Storage ..... −65°C to +150°C
Under Bias
Military/Extended ..... −65°C to +135°C
Commercial ..... −10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground ..... +6.0 V to −0.5 V
Undershoot/Overshoot pulse of less then 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... (undershoot) −1.0 V (overshoot) + 7.0 V

D.C. Operating Characteristics (Over the operating V_{CC} and temperature range)

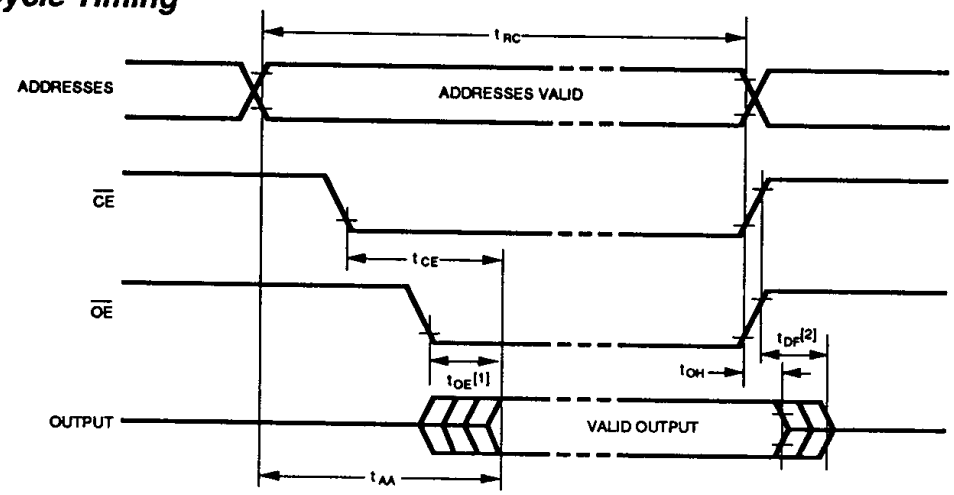
Symbol	Parameter		Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current	Mil./Ext.		120	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}: All I/O Open; Other Inputs = V_{CC} Max.
		Commercial		110		
I_{SB}	Standby V_{CC} Current	Mil./Ext.		50	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = V_{CC} Max.
		Commercial		40		
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{CC} Max.
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{CC} Max.
V_{IL}	Input Low Voltage		−0.1	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} +1	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = −400 µA

A.C. Characteristics

Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits 2864H-200 2864-200 Min.	Limits 2864H-200 2864-200 Max.	Limits 2864H-250 2864-250 Min.	Limits 2864H-250 2864-250 Max.	Limits 2864H-300 2864-300 Min.	Limits 2864H-300 2864-300 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	200		250		300		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	Chip Enable Access Time		200		250		300	ns	$\overline{OE}$ = V_{IL}
t_{AA}	Address Access Time		200		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{OE}	Output Enable Access Time		90		90		100	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	0	60	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE}$ = V_{IL}

Read Cycle Timing



NOTES:
1. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC Characteristics

Write Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter		Limits						Units
			2864H-200 2864-200		2864H-250 2864-250		2864H-300 2864-300		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time/Byte	2864		10		10		10	ms
		2864H		2		2		2	ms
t_{AS}	Address to $\overline{WE}$ Set Up Time		10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time		0		0		0		ns
t_{WP}[2]	$\overline{WE}$ Write Pulse Width		150		150		150		ns
t_{AH}	Address Hold Time		50		50		50		ns
t_{DS}	Data Set Up Time		50		50		50		ns
t_{DH}	Data Hold Time		20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time		0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time		10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time		10		10		10		ns
t_{DL}	Data Latch Time		50		50		50		ns
t_{DV}[3]	Data Valid Time			1		1		1	µs
t_{DB}	Time to Device Busy			200		200		200	ns
t_{WR}	Write Recovery Time Before Read Cycle			10		10		10	µs

NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 µs maximum after the initiation of a write cycle.

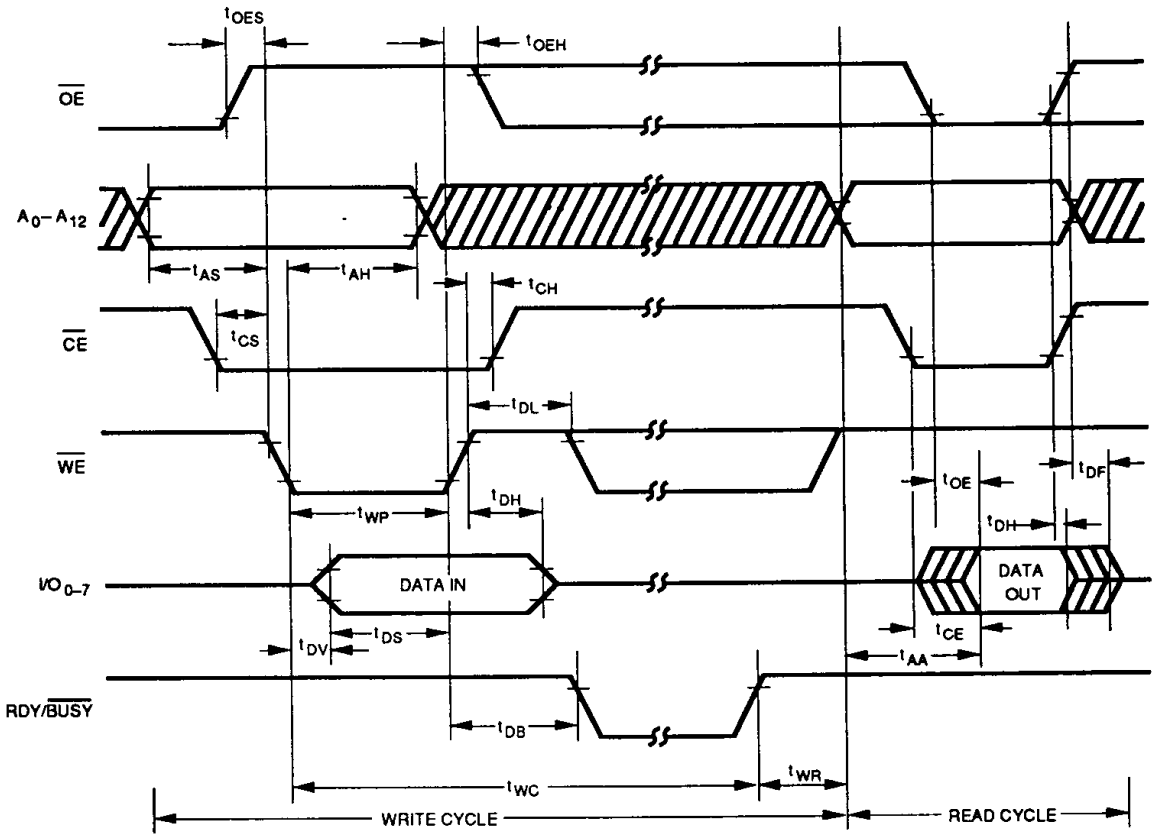
Capacitance T_A[1] = 25°C, f = 1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O}$ = 0 V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: < 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Write Cycle Timing



Ordering Information