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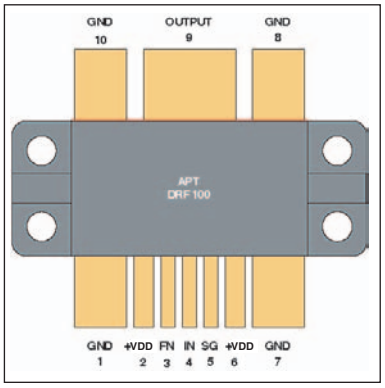
ADVANCED POWER TECHNOLOGY®

15V, 8A, 30MHz

High Speed MOSFET Driver

The DRF100 is a High-Speed Power MOSFET driver with a unique anti-ring function. It is intended to drive the gate of a power MOSFET ≥3nF, gate capacitance to an 18V maximum, at frequencies up to 30MHz. It can produce output currents ≥8A RMS, while dissipating 100W.



FEATURES

- **Switching Frequency: DC TO 30MHz**
- **Switching Speeds 3-4ns 50Ω Load**
- **Low Pulse Width Distortion**
- **Single Power Supply**
- **3V CMOS Schmitt Trigger Input 1V Hysteresis**
- **Output Capable of ≥ 8A RMS**
- **Power Dissipation Capability >100W**

TYPICAL APPLICATIONS

- **MOSFET Drivers**
- **Switch Mode Power Amplifiers**
- **Digital Output Amplifiers**
- **Pulse Generators**
- **Laser Diode Drivers**
- **Ultrasound Transducer Drivers**
- **Acoustic Optical Modulators**

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	18	V
V_{IN}	Input Single Voltage	5.5	

Specifications

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Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	8		18	V
I_{OUT} [5]	Output Current			8	A
V_{IN}	Input Voltage		3		V
$V_{IN(R)}$ [6]	Input Voltage Rising Edge	1.8		2.2	ns
$V_{IN(F)}$ [6]	Input Voltage Falling Edge	8		1.2	
I_{DDQ}	Quiescent Current		200		µA
I_O	Max Output Current		8		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance		3		
V_{IL}	Input Low	0.8		1.0	V
V_{IH}	Input High	1.9		2.2	
V_{DLY}	Time Delay (throughput)		38		ns

Thermal Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.71	°C/W
T_J	Operating Junction Temperature			175	°C
P_D	Maximum Power Dissipation			>100	W
P_{DC}	Total Power Dissipation @ T_C = 25°C			210	

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Driver Specifications T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typical RL	Typical CL	Max	Unit
t_r	Rise Time [2,3]	$15V_{DD}$		3.1	7.5		ns
t_f	Fall Time [2,3]	$15V_{DD}$		2.8	7.5		
T_D	Prop. Delay [2,4]	15V		33	38		
	Symmetry [1]	$15V_{DD}$ [3]		1.2			%

Driver Output Characteristics T_J = 25°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
C_{out}	Output Capacitance [2,5]		2500		pF
R_{out}	Output Resistance [2,5]		1		Ω
L_{out}	Output Inductance [2,5]	2	3	4	nH
F_{MAX}	Operating Frequency			30	MHz

Test curcuit show on page 3.
All measurements were made with the Anti-Ring circuit activated unless noted.
① Symmetry is the percent difference in high and low FWHM times with a 50% duty cycle square wave input.
② R_L = 50Ω, C_L = 3000pF
③ 10% - 90% See Test Circuit
④ 50% - 50%, see Test Circuit
⑤ V_{DD} = 18V, C_L = 3000pF, F = 10MHz
⑥Performance specified with this input.

APT reserves the right to change, without notice, the specifications and information contained herein.

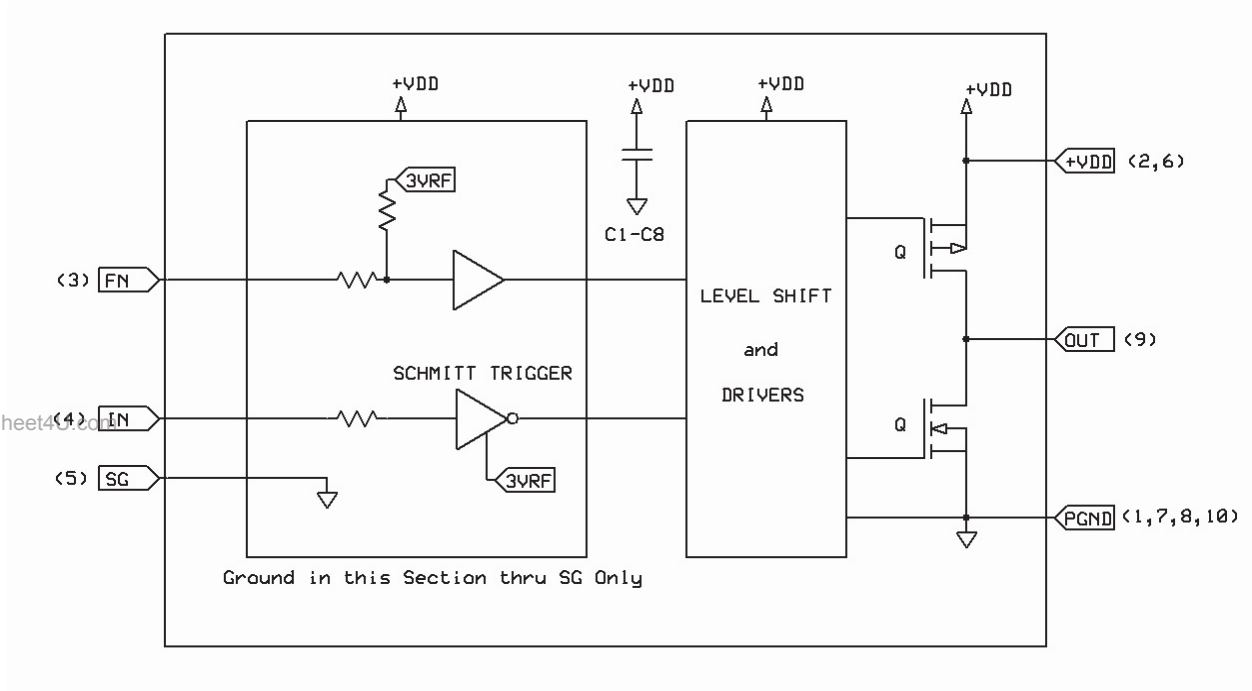

Figure 1, DRF100 Simplified Ciruit Diagram

A Simplified DRF100 Circuit Diagram is illustrated above. By including the driver high speed by-pass capacitors (C1-C8), their contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This, coupled with the tight geometry of the hybrid, allows optimum drive to the gate of the MOSFET. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground (4,5) and the Anti-Ring Function, provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency applications

The IN pin (4) is applied to a Schmitt Trigger. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. The P channel and N channel power drivers provide the high current to the OUT pin (9).

The FUNCTION, FN, pin (3) is used to disable the Anti-Ring function. It is recommended that the device be operated with this function enabled. Func. = Hi (+5V or Float) Anti-Ring on, Func. = Low (0V or GND.) Anti-ring off.

Driver Control Logic

In (4) HIGHDriver	Output (9) LOW
In (4) LOWDriver	Output (9) HIGH

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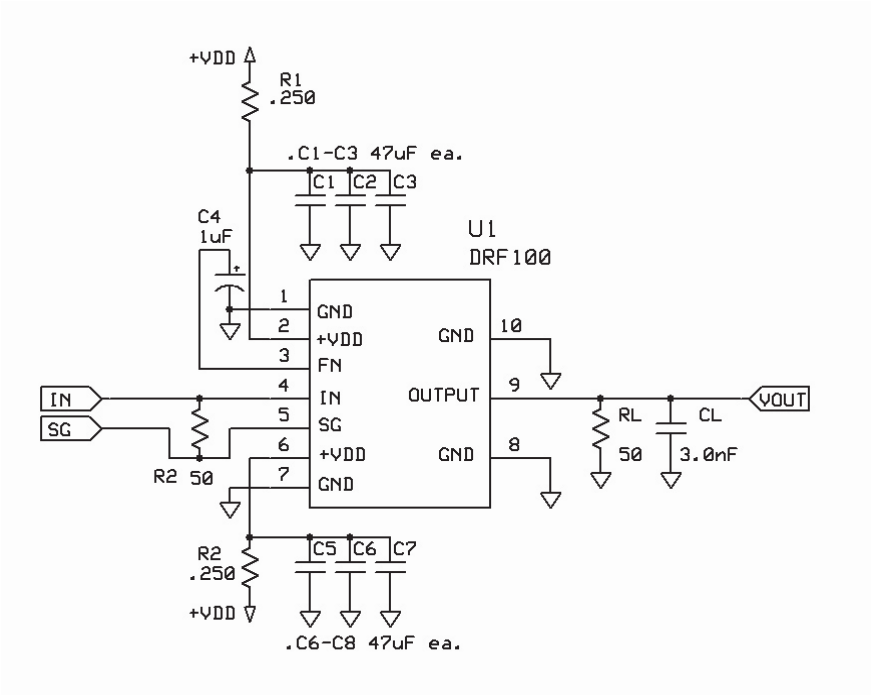

Figure 2, Test Circuit

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The Test Circuit illustrated above was used to evaluate the DRF100 (available as an evaluation Board DRF-100EVAL). The input control signal is applied to the DRF100 via the IN(4) and SG(5) pins via RG188. This provides excellent noise immunity and control of the signal ground currents.

The FN pin is off and unwanted signals can cause erratic behavior, Therefore FN pin is heavily by-passed on the Evaluation board, see FN (3) above.

The +Vcc inputs (2,6) are heavily By-Passed (C1-C3, C5-C7), this is in addition to the internal bypassing mentioned previously. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the load.

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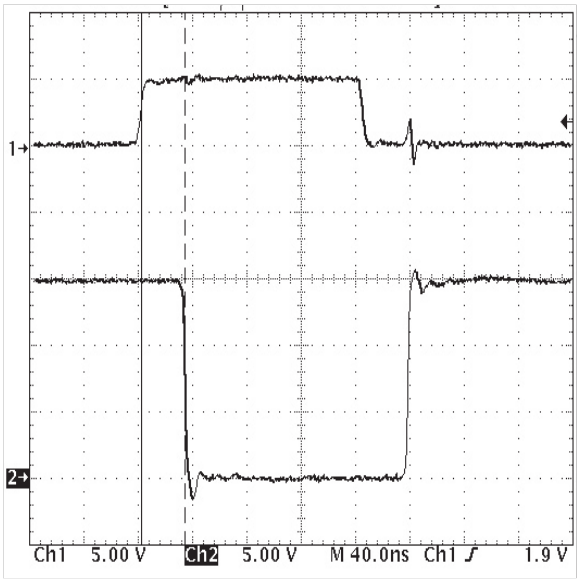

Figure 3, Leading Edge throughput Delay ≅ 32ns

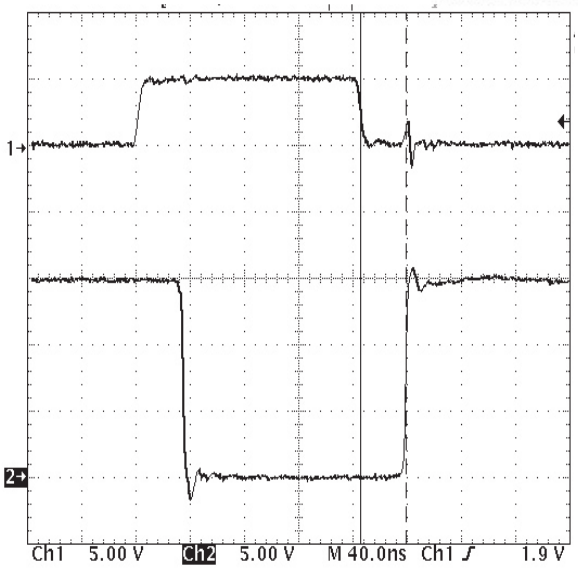

Figure 4, Trailing Edge throughput Delay ≅ 33ns

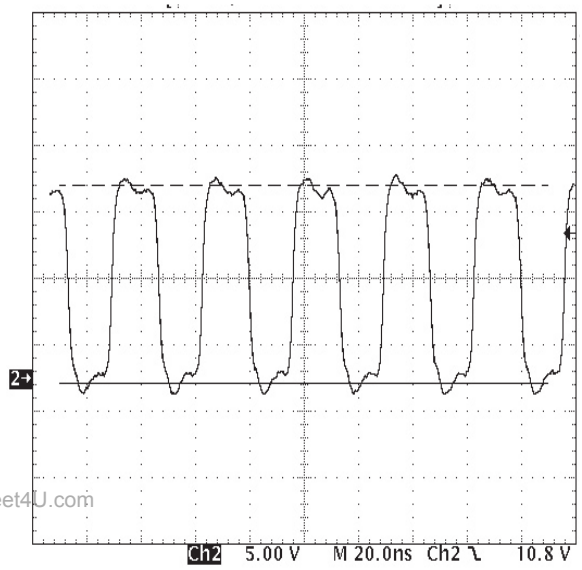

Figure 5, 30MHz Output into 50Ω

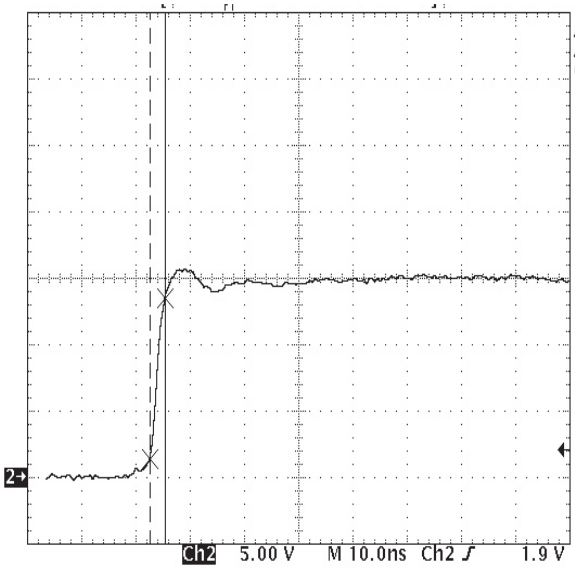

Figure 6, Output Rise Time = 2.8ns

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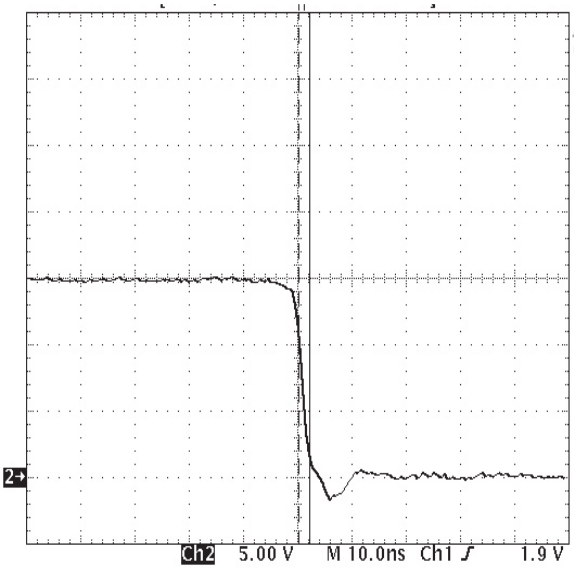

Figure 7, Output Fall Time = 2.0ns

All waveforms on this page, Figures 3 thru 7, were taken using the test circuit of Figure 1, with the following test conditions:

1. +VDD = 15V
2. Control input 5.0V/50Ω
3. Load = 50Ω

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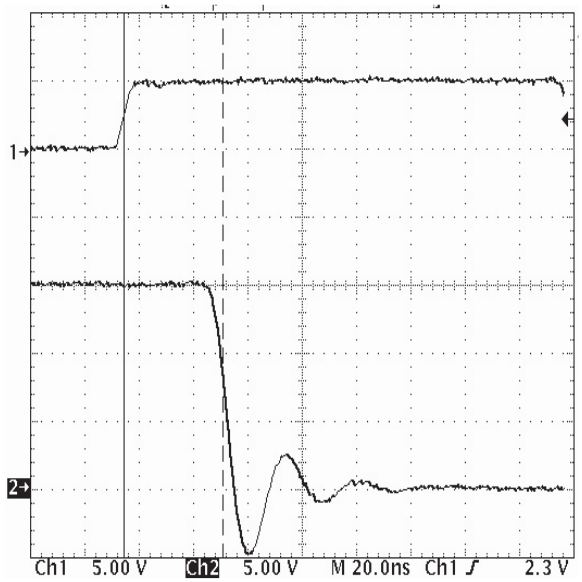

Figure 8, Leading Edge throughput Delay ≅ 37ns

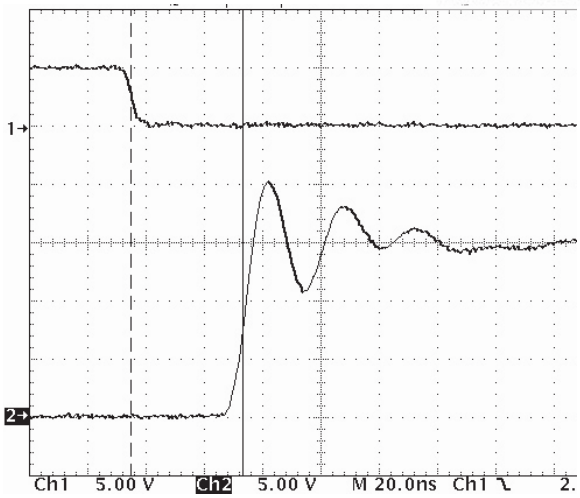

Figure 9, Trailing Edge throughput Delay ≅ 37ns

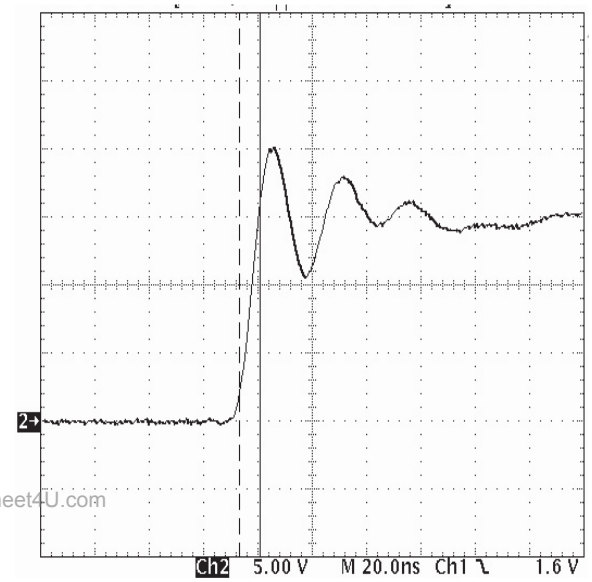

Figure 10, Output Rise Time = 7.2ns

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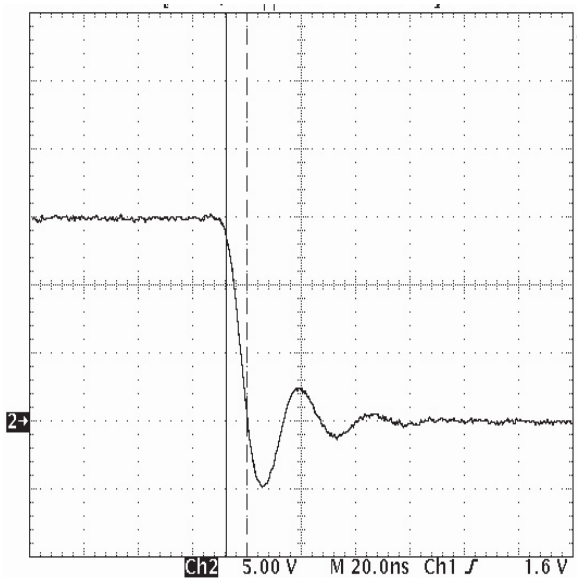

Figure 11, Output Fall Time = 7.2ns

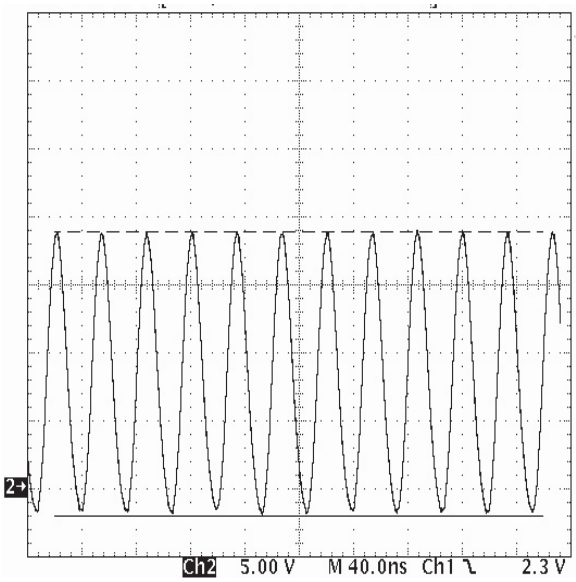

Figure 12, DRF-100 Output @ 30MHz in to 50Ω +3nF

All waveforms on this page, Figures 8 thru 12, were taken using the test circuit of Figure 3, with the following test conditions:

4. +VDD = 15V
5. Control input 5.0V/50Ω
6. Load = 50Ω+3nF

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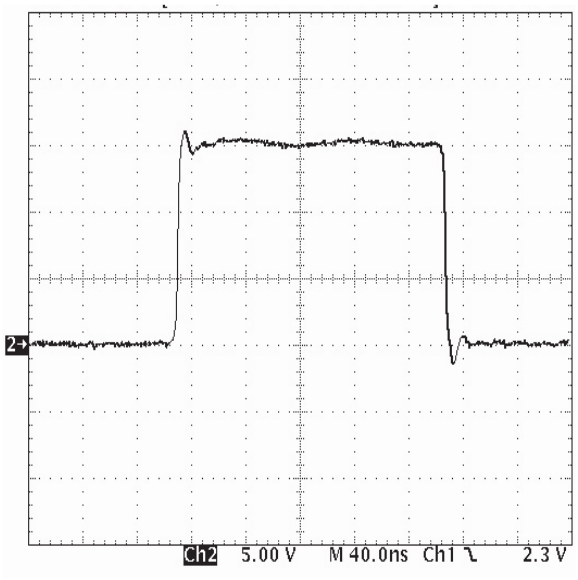

Figure 13, Anti-Ring ON

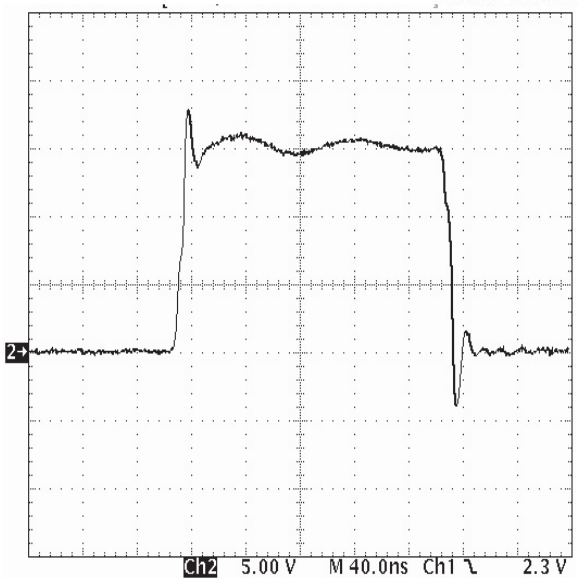

Figure 14, Anit-RIng OFF

The output waveform with the Anti-Ring function ON is illustrated in Figure 13 and the Anti-Ring function OFF is illustrated in Figure 14. The load is 50Ω with no load capacitance, other than the output capacitance of the driver.

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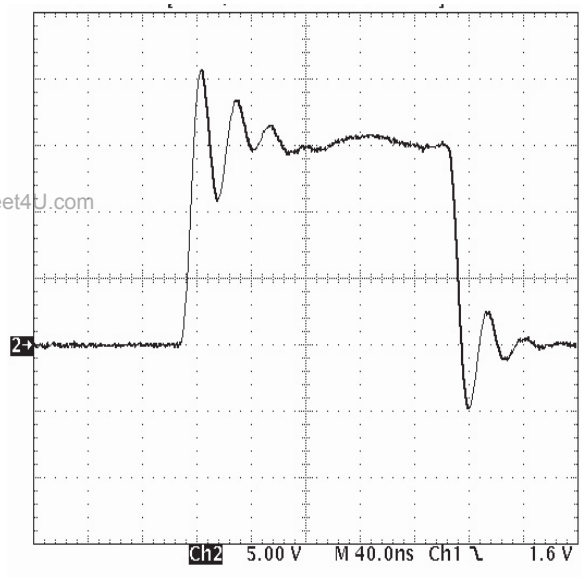

Figure 15, Anti-Ring ON

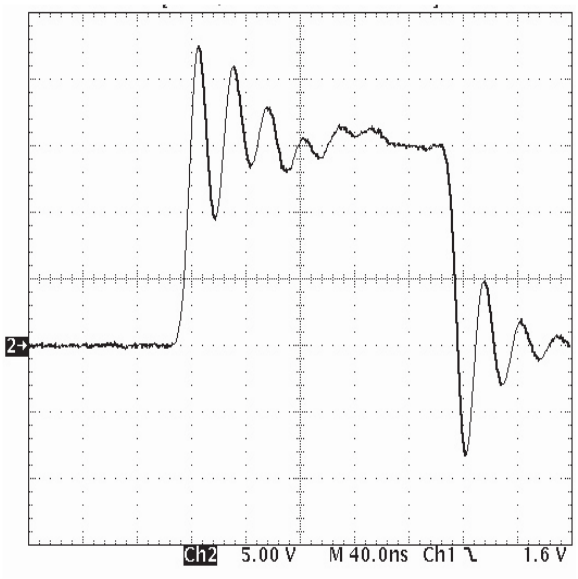

Figure 16, Anit-RIng OFF

The output waveform with the Anti-Ring function ON is illustrated in Figure 15 and the Anti-Ring function OFF is illustrated in Figure 16. The load is 50Ω + 3nF of capacitance. The ring amplitude in Figure 15 is clearly above the 2-4V threshold voltage of most power MOSFETs, while In Figure 16 we see that the ring peak is at ≅2V, also see Figure 13. It is most likely that the wave form of Figure 16 will cause a cross conduction in a Bridge or push pull topology.

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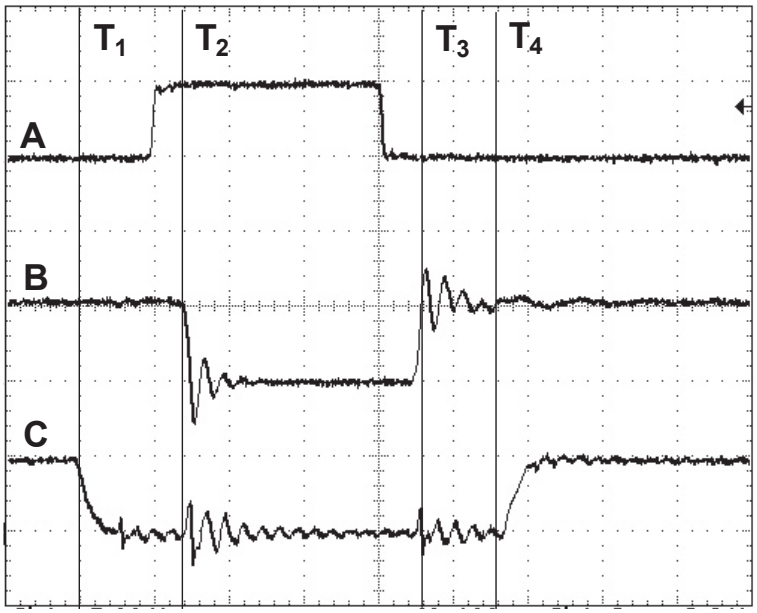

Figure 17

The real time gating of the FN function is illustrated in Figure 17. At T_1 the FN trace (**C**) is deactivated and at T_4 it is reactivated.

The output is shown as trace (**B**), There is significant ringing on both the leading and tailing edges. Trace (**A**) is the input control signal

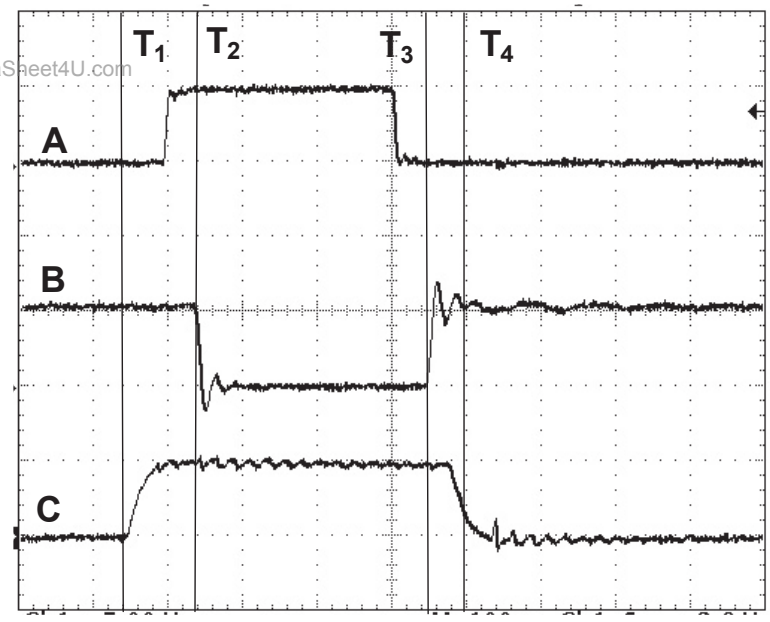

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Figure 18

In Figure 18, trace (**B**) shows the anti-ring function active during the pulse. In trace (**B**) we see the output with a greatly reduced ring amplitude.

Note: load = 50Ω + 3nF, series inductance is estimated at 3nH. A typical MOSFET can exceed this value.

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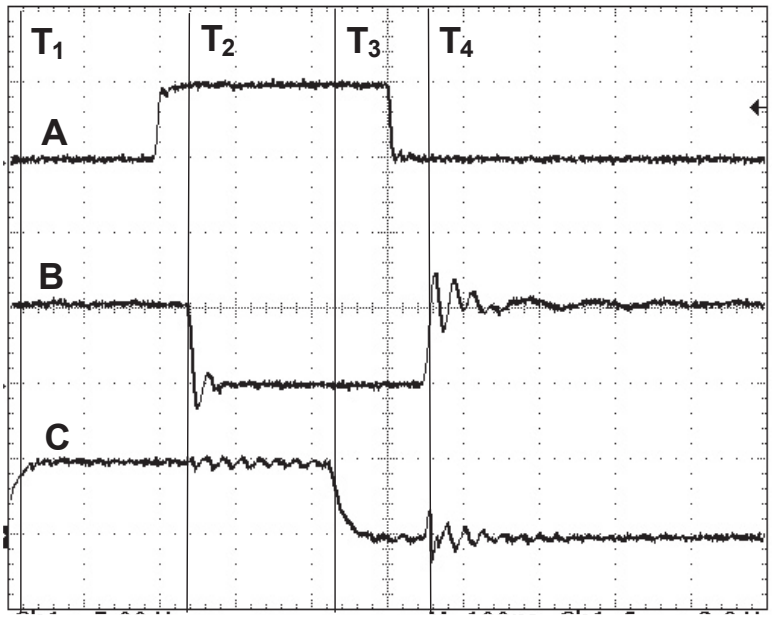

Figure 19

In Figure 19, we see the anti-ring function FN active for the leading edge only, T_2. Figure 20, illustrates the anti-ring function active on the trailing edge only.

Note: load = 50Ω + 3nF, series inductance is estimated at 3 nH, A typical MOSFET can exceed this value.

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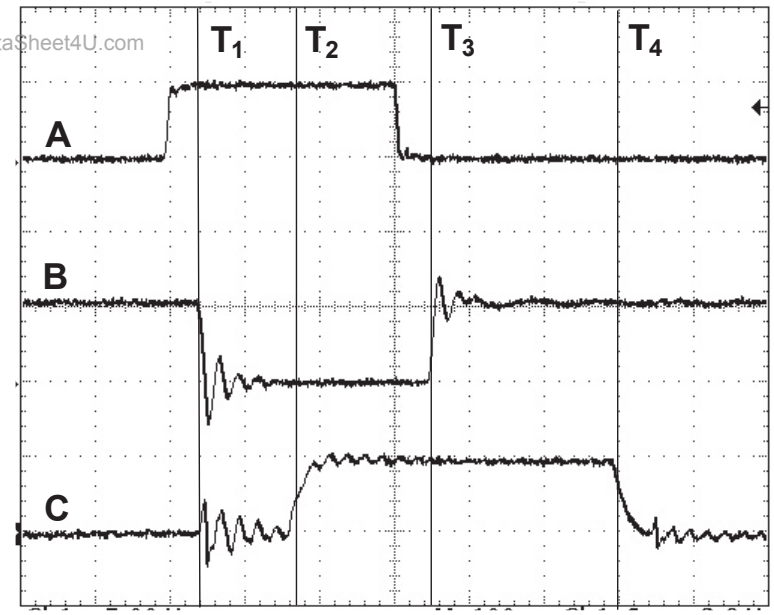

Figure 20

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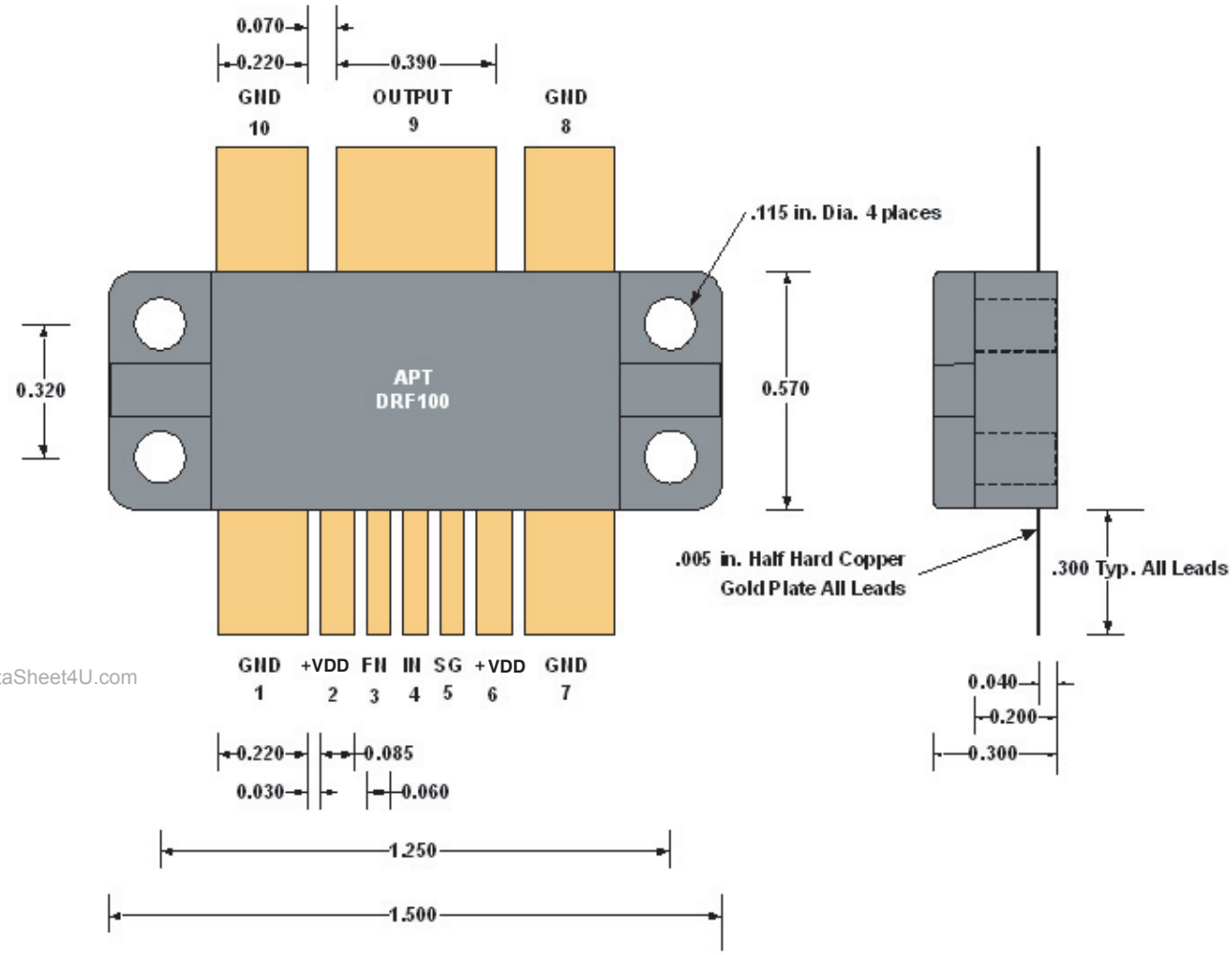

Figure 21, DRF100 Mechanical Outline

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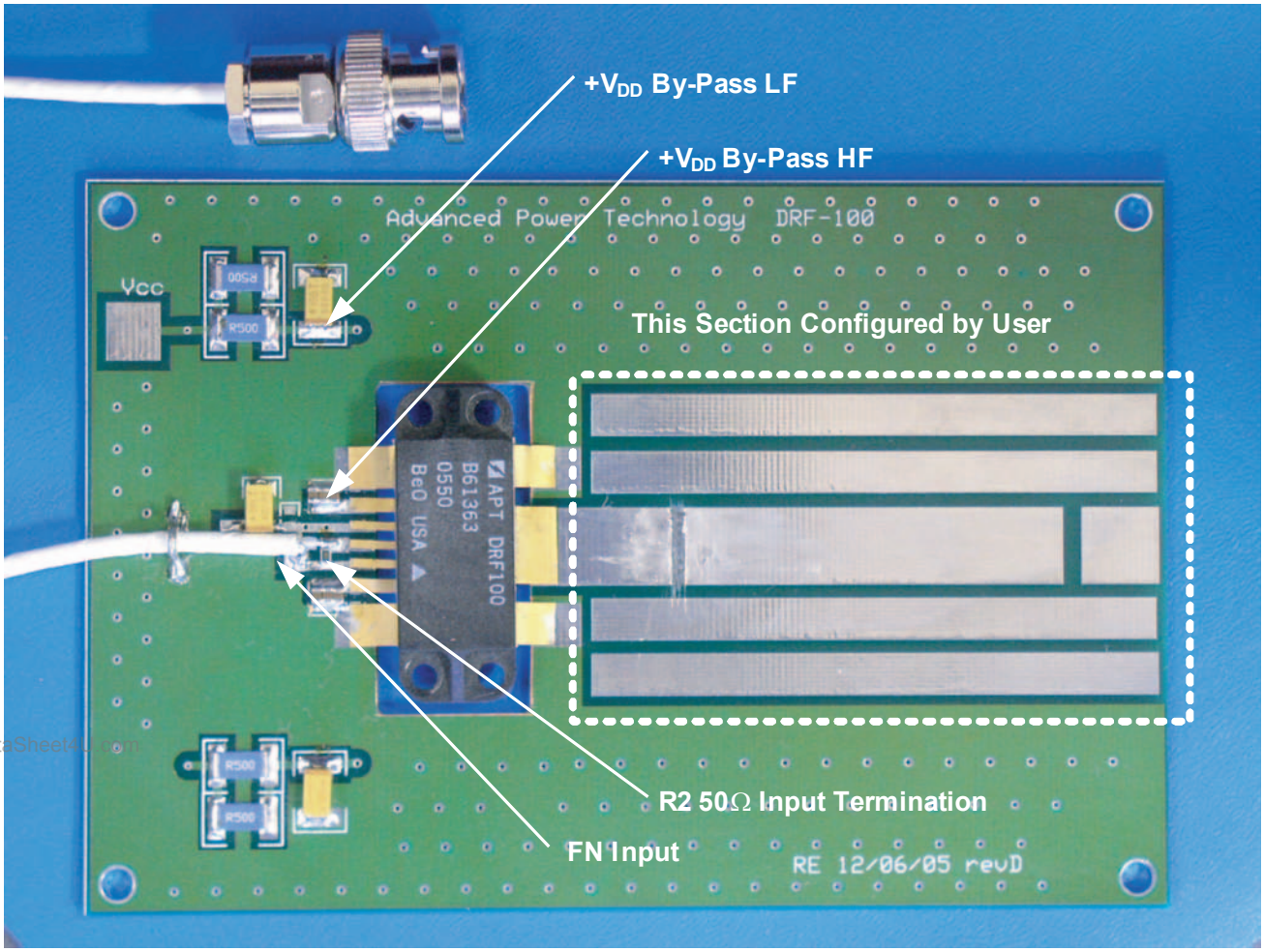

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Figure 22, DRF100 Eval Board

The DFR100 is a high power device and must have adequate cooling for full power operation

Evaluation Boards are provided to facilitate the circuit design process by allowing the end user to quickly evaluate the performance of our components under a specific and single set of conditions. They are not intended to be used as a sub assembly in any final product(s). Care has been taken to insure that the Evaluation Boards are assembled to correctly represent the test circuit included in the component data sheet. There is no warranty of these Evaluation Boards beyond workmanship and materials.

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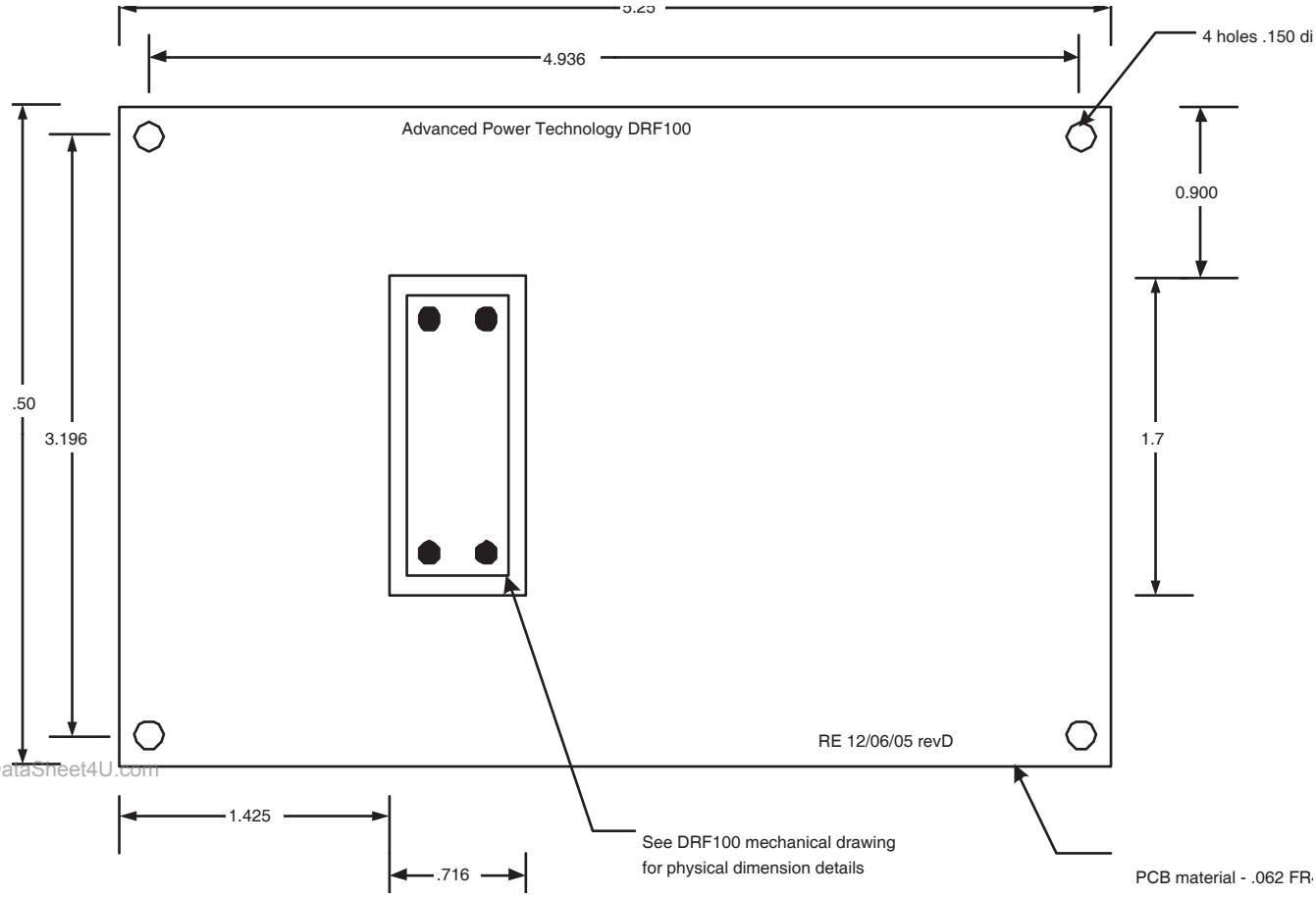

Figure 23, DRF100 Eval Board Mechanical

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Mounting instructions for Flangeless Packages

Heat sink mounting of any device in the Flangeless Package family follows the same process details outlined in this document.

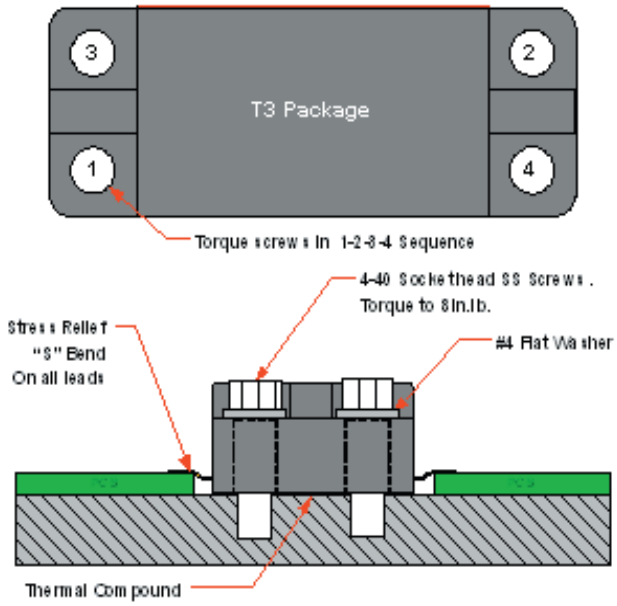

Figure 24, Top and Side View of a T3 device

Heat Sink Surface:

1. The heat sink surface should be smooth, free of nicks and burs; in addition it should be flat to ≤.001in./in TIR, (Total Indicator Run out) and be finished to ~ 68µ CLA, (Center Line Average).
2. Must be free of solder balls, metal shavings and any foreign objects or material.

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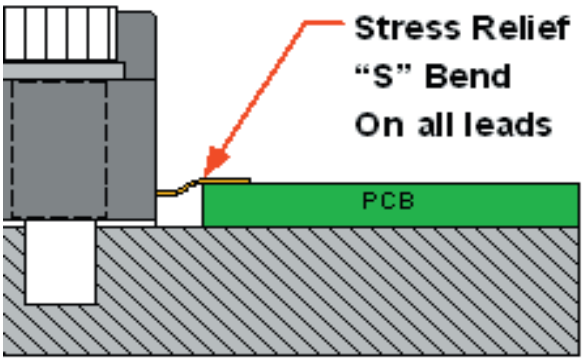

Figure 25, Stress Relief bend

Device Preparation:

1. The leads should be prepared with an "s" bend, as shown in Figure 25 prior to mounting on the heat sink.
2. The BeO surface of the device must be free of any foreign objects or material.
3. The BeO surface must be coated with a thin and uniform film of thermal compound.
4. For commercial manufacturing the suggested method for thermal compound application is to apply the compound using a screen printer. This process insures consistent and repeatable performance with minimum effort.

Mechanical Attachment:

1. The four screws (1-2-3-4), as shown in Figure 24, should be installed and seated, then torqued to one-half the specification, in the sequence shown. First screw 1 then screw 2, 3 and 4.
2. Then complete the process by tightening to the full specification in the same manner.
3. The torque spec is 8in.lb. ± 1lb. (0.9Nm)

Lead Attachment:

1. The leads may now be soldered to the PCB
2. Maximum lead temperature must not exceed 300oC for 10s.
3. For lead free use 96.5 % tin, 3% silver, and 0.5% copper.
4. Non-lead Free use 2% Silver, 62% Tin, 36% lead (sn62).