

## DRV8806 Quad Serial Interface Low-Side Driver IC

### 1 Features

- 4-Channel Protected Low-Side Driver
  - Four NMOS FETs With Overcurrent Protection
  - Integrated Inductive Clamp Diodes
  - Serial Interface
  - Open/Shorted Load Detection
- 2-A (Single Channel On)/1-A (All Channels On) Maximum Drive Current per Channel (at 25°C)
- 8.2-V to 40-V Operating Supply Voltage Range
- Thermally-Enhanced Surface Mount Package

### 2 Applications

- Relay Drivers
- Unipolar Stepper Motor Drivers
- Solenoid Drivers
- General Low-Side Switch Applications

### 3 Description

The DRV8806 provides a 4-channel low-side driver with overcurrent protection. It has built-in diodes to clamp turnoff transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

The DRV8806 can supply up to 2-A (single channel on) or 1-A (all channels on) continuous output current (with adequate PCB heatsinking at 25°C).

A serial interface is provided to control the output drivers. Fault status can be read through the serial interface. Multiple DRV8806 devices can be chained together to use a single serial interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature, and faults are indicated by a fault output pin.

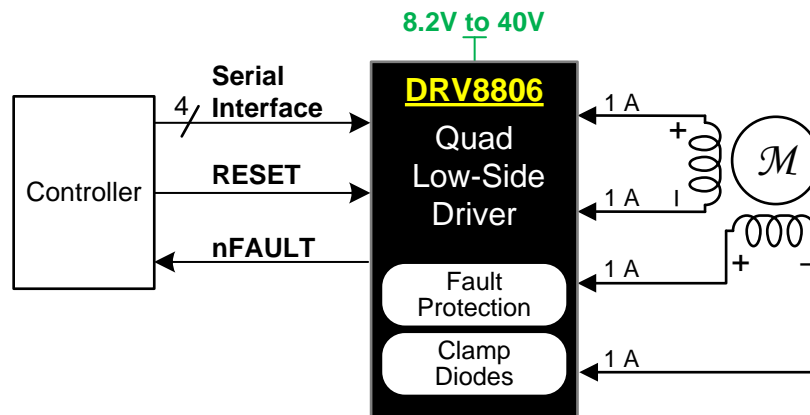
The DRV8806 is available in a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8806	HTSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



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## 4 Revision History

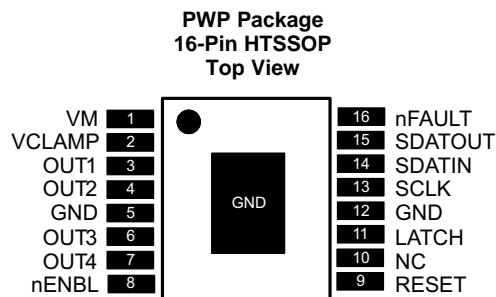
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (December 2013) to Revision C</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .....</li> </ul>	<b>1</b>

<b>Changes from Revision A (November 2013) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed (OPEN-DRAIN to PUSH-PULL in the elec chara table section SDATAOUT OUTPUT .....</li> </ul>	<b>5</b>
<ul style="list-style-type: none"> <li>Added another row below <math>V_{OH}</math> - merge the first two columns together (<math>V_{OH}</math> and Output high voltage). The second row should have test condition "I<sub>o</sub> = 100 <math>\mu</math>A, V<sub>M</sub> = 8.2 V" and be specified as 2.5 V MIN .....</li> </ul>	<b>5</b>
<ul style="list-style-type: none"> <li>Added two new rows, I<sub>SRC</sub> and I<sub>SNK</sub> in elec chara table, section SDATAOUT OUTPUT.....</li> </ul>	<b>5</b>
<ul style="list-style-type: none"> <li>Changed NO. 6 in Timing Requirements table .....</li> </ul>	<b>6</b>
<ul style="list-style-type: none"> <li>Added a sentence in second paragraph below Figure 2: A pullup resistor.....1 kohm is recommended. ....</li> </ul>	<b>10</b>

<b>Changes from Original (June 2012) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added comment to Timing Requirements section.....</li> </ul>	<b>6</b>
<ul style="list-style-type: none"> <li>Changed Functional Block Diagram at SDATOUT.....</li> </ul>	<b>8</b>
<ul style="list-style-type: none"> <li>Changed <a href="#">Figure 6</a> at SDATOUT.....</li> </ul>	<b>10</b>
<ul style="list-style-type: none"> <li>Changed SDATOUT description in Serial Interface Operation section .....</li> </ul>	<b>10</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
<b>POWER AND GROUND</b>				
GND	5, 12, PowerPAD™	—	Device ground	All pins must be connected to GND.
VM	1	—	Device power supply	Connect to motor supply (8.2 V - 40 V).
<b>CONTROL</b>				
LATCH	11	I	Latch input	Rising edge latches shift register to output stage, falling edge latches fault data into output shift register – internal pull-down
nENBL	8	I	Enable input	Active low enables outputs – internal pull-down
RESET	9	I	Reset input	Active-high reset input initializes internal logic – internal pull-down
SCLK	13	I	Serial clock	Serial clock input – internal pull-down
SDATIN	14	I	Serial data input	Serial data input – internal pull-down
SDATOUT	15	OD	Serial data output	Serial data output; push-pull structure; see serial interface section for details
<b>STATUS</b>				
nFAULT	16	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent, open load) - open-drain output
<b>OUTPUT</b>				
OUT1	3	O	Output 1	Connect to load 1
OUT2	4	O	Output 2	Connect to load 2
OUT3	6	O	Output 3	Connect to load 3
OUT4	7	O	Output 4	Connect to load 4
VCLAMP	2	—	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>M</sub>	Power supply voltage	-0.3	43	V
V <sub>OUTx</sub>	Output voltage	-0.3	43	V
V <sub>CLAMP</sub>	Clamp voltage	-0.3	43	V
SDATOUT, nFAULT	Output current		20	mA
	Peak clamp diode current <sup>(3)</sup>		2	A
	DC or RMS clamp diode current <sup>(3)</sup>		1	A
	Digital input pin voltage	-0.5	7	V
SDATOUT, nFAULT	Digital output pin voltage	-0.5	7	V
	Peak motor drive output current, t < 1 μs		Internally limited	A
	Continuous total power dissipation <sup>(3)</sup>		See <a href="#">Thermal Information</a>	
T <sub>J</sub>	Operating virtual junction temperature <sup>(3)</sup>	-40	150	°C
T <sub>stg</sub>	Storage temperature	-60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Power dissipation and thermal limits must be observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±6000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>M</sub>	Power supply voltage	8.2		40	V
V <sub>CLAMP</sub>	Output clamp voltage <sup>(1)</sup>	0		40	V
I <sub>OUT</sub>	Continuous output current, single channel on, T <sub>A</sub> = 25°C <sup>(2)</sup>			2	A
	Continuous output current, four channels on, T <sub>A</sub> = 25°C <sup>(2)</sup>			1	A

- (1) V<sub>CLAMP</sub> is not a power supply input pin - it only connects to the output clamp diodes.
- (2) Power dissipation and thermal limits must be observed.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DRV8806	
		PWP (HTSSOP)	
		16 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	39.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	24.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	20.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	20.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

T<sub>A</sub> = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES</b>						
I <sub>VM</sub>	VM operating supply current	V <sub>M</sub> = 24 V		1.6	3	mA
V <sub>UVLO</sub>	VM undervoltage lockout voltage	V <sub>M</sub> rising			8.2	V
<b>LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)</b>						
V <sub>IL</sub>	Input low voltage				0.8	V
V <sub>IH</sub>	Input high voltage		2			V
V <sub>HYS</sub>	Input hysteresis			0.45		V
I <sub>IL</sub>	Input low current	V <sub>IN</sub> = 0	-20		20	μA
I <sub>IH</sub>	Input high current	V <sub>IN</sub> = 3.3 V			100	μA
R <sub>PD</sub>	Pulldown resistance			100		kΩ
<b>nFAULT OUTPUT (OPEN-DRAIN OUTPUT)</b>						
V <sub>OL</sub>	Output low voltage	I <sub>O</sub> = 5 mA			0.5	V
I <sub>OH</sub>	Output high leakage current	V <sub>O</sub> = 3.3 V			1	μA
<b>SDATOUT OUTPUT (PUSH-PULL OUTPUT WITH INTERNAL PULLUP)</b>						
V <sub>OL</sub>	Output low voltage	I <sub>O</sub> = 5 mA		0.5		V
V <sub>OH</sub>	Output high voltage	I <sub>O</sub> = 100 μA, V <sub>M</sub> = 11 V - 60 V, peak			6.5	V
		I <sub>O</sub> = 100 μA, V <sub>M</sub> = 11 V - 60 V, steady state	3.3	4.5	5.6	V
		I <sub>O</sub> = 100 μA, V <sub>M</sub> = 8.2 V - 11 V, steady state	2.5			V
I <sub>SRC</sub>	Output source current	V <sub>M</sub> = 24 V			1	mA
I <sub>SNK</sub>	Output sink current	V <sub>M</sub> = 24 V			5	mA
<b>LOW-SIDE FETS</b>						
R <sub>DS(ON)</sub>	FET on resistance	V <sub>M</sub> = 24 V, I <sub>O</sub> = 700 mA, T <sub>J</sub> = 25°C		0.5		Ω
		V <sub>M</sub> = 24 V, I <sub>O</sub> = 700 mA, T <sub>J</sub> = 85°C		0.75	0.8	
I <sub>OFF</sub>	Open load detect current		0	25	50	μA
<b>HIGH-SIDE DIODES</b>						
V <sub>F</sub>	Diode forward voltage	V <sub>M</sub> = 24 V, I <sub>O</sub> = 700 mA, T <sub>J</sub> = 25°C		0.9		V
I <sub>OFF</sub>	Off state leakage current	V <sub>M</sub> = 24 V, T <sub>J</sub> = 25°C	-50		50	μA
<b>OUTPUTS</b>						
t <sub>R</sub>	Rise time	V <sub>M</sub> = 24 V, I <sub>O</sub> = 700 mA, Resistive load	50		300	ns
t <sub>F</sub>	Fall time	V <sub>M</sub> = 24 V, I <sub>O</sub> = 700 mA, Resistive load	50		150	ns
<b>PROTECTION CIRCUITS</b>						
I <sub>OC</sub>	Overcurrent protection trip level		3		5	A

### Electrical Characteristics (continued)

T<sub>A</sub> = 25°C, over recommended operating conditions (unless otherwise noted)

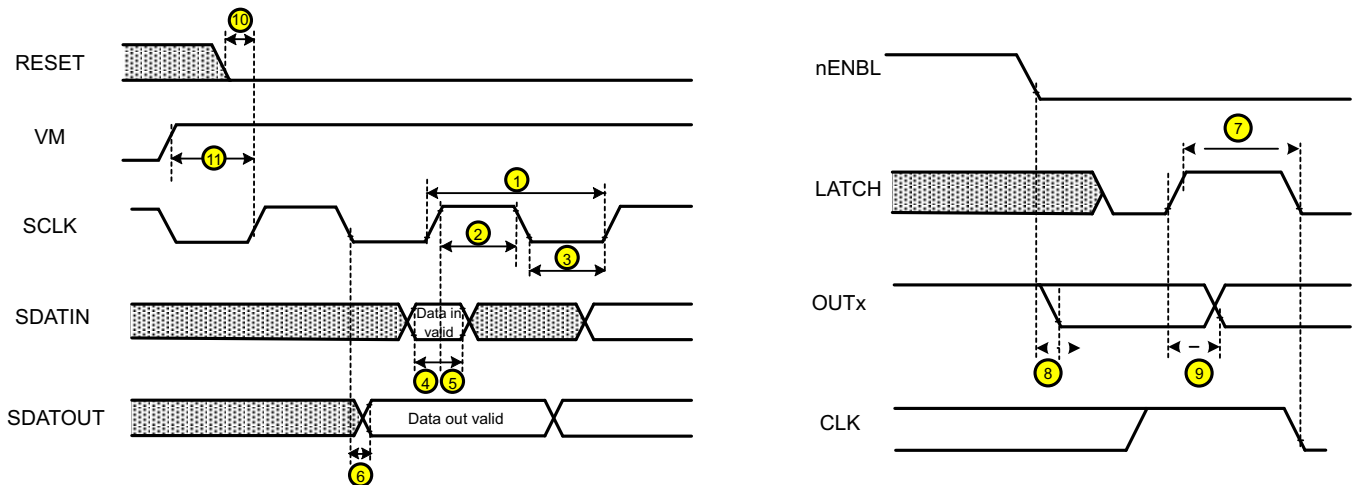
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>OCP</sub>	Overcurrent protection deglitch time		3.5		μs	
t <sub>OL</sub>	Open load detect deglitch time		15		μs	
t <sub>RETRY</sub>	Overcurrent protection re-try time		1.2		ms	
T <sub>TSD</sub>	Thermal shutdown temperature	Die temperature	150	160	180	°C

### 6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	NOM	MAX	UNIT
1 t <sub>CYC</sub> Clock cycle time	62			ns
2 t <sub>CLKH</sub> Clock high time	25			ns
3 t <sub>CLKL</sub> Clock low time	25			ns
4 t <sub>SU(SDATIN)</sub> Setup time, SDATIN to SCLK	5			ns
5 t <sub>H(SDATIN)</sub> Hold time, SDATIN to SCLK	1			ns
6 t <sub>D(SDATOUT)</sub> Delay time, SCLK to SDATOUT, no external pullup resistor, C <sub>OUT</sub> = 100 pF		50	100	ns
7 t <sub>W(LATCH)</sub> Pulse width, LATCH	200			ns
8 t <sub>OE(ENABLE)</sub> Enable time, nENBL to output low		60		ns
9 t <sub>D(LATCH)</sub> Delay time, LATCH to output change		200		ns
— t <sub>RESET</sub> RESET pulse width	20			μs
10 t <sub>D(RESET)</sub> Reset delay before clock	20			μs
11 t <sub>STARTUP</sub> Start-up delay VM applied before clock	55			μs

(1) Not production tested.



More than 400 ns of delay should exist between the final SCLK rising edge and the LATCH rising edge. This ensures that the last data bit is shifted into the device properly.

Figure 1. DRV8806 Timing Requirements

## 6.7 Typical Characteristics

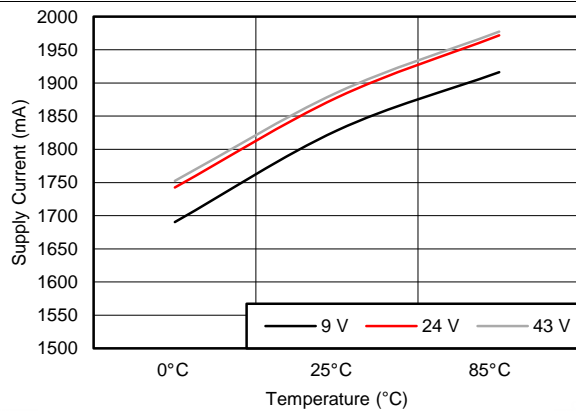


Figure 2. Supply Current vs Temperature

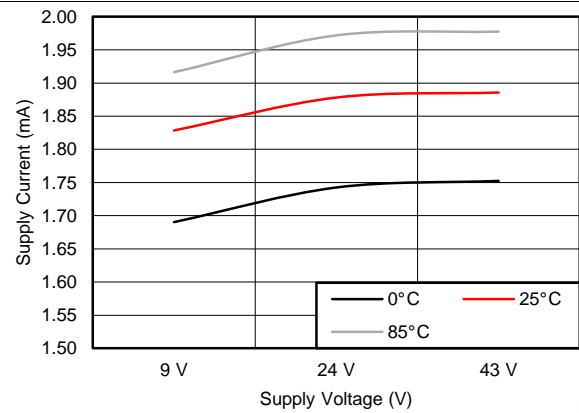


Figure 3. Supply Current vs Supply Voltage

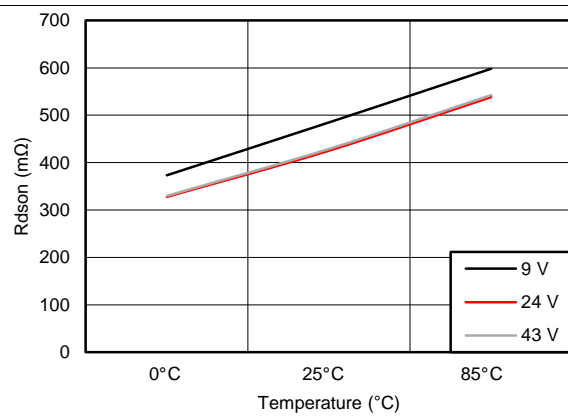


Figure 4.  $R_{DS(ON)}$  vs Temperature

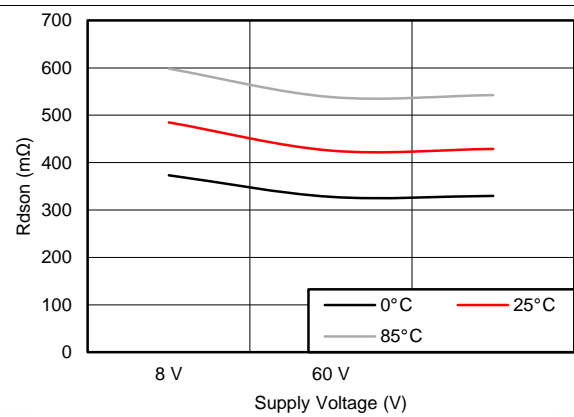


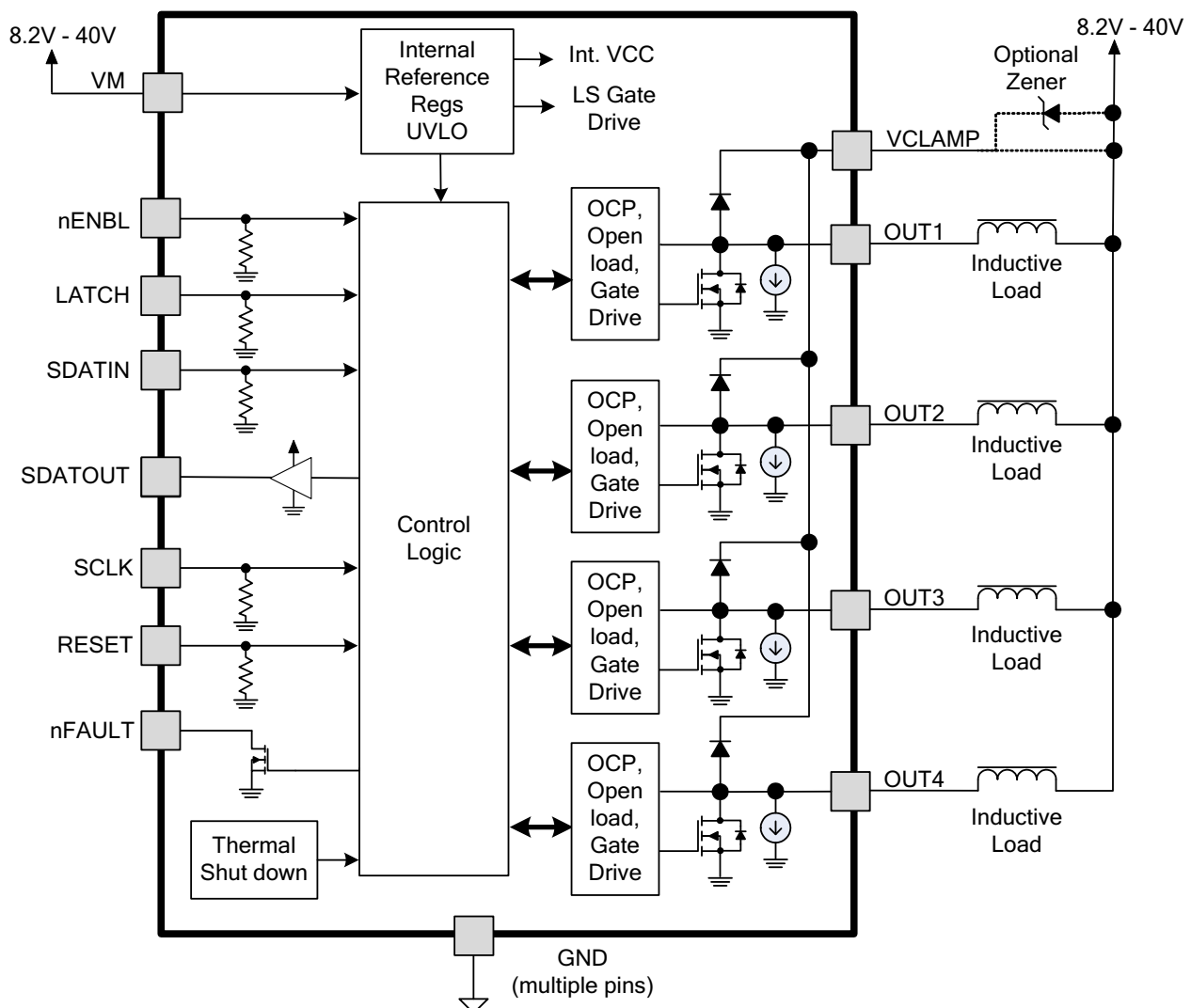
Figure 5.  $R_{DS(ON)}$  vs Supply Voltage

## 7 Detailed Description

### 7.1 Overview

The DRV8806 is an integrated 4-channel low-side driver controlled using a serial interface to change the state of the low-side driver outputs. The low-side driver outputs consist of four N-channel MOSFETs that have a typical  $R_{DS(ON)}$  of 500 m $\Omega$ . A single motor supply input VM serves as device power and is internally regulated to power the low-side gate drive. Data is shifted into a temporary data register in the device through the SDATIN pin, one bit at each rising edge of SCLK, while LATCH is held low. The outputs of the device can be disabled by pulling nENBL logic high. Several safety features are integrated in the device including overcurrent protection, thermal shutdown, undervoltage lockout, and open load protection. The overcurrent protection and open load faults share a fault bit per channel that is set when one of these conditions occurs.

### 7.2 Functional Block Diagram





## 7.3 Feature Description

### 7.3.1 Output Drivers

The DRV8806 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage,  $V_M$ . It can also be connected to a Zener or TVS diode to  $V_M$ , allowing the switch voltage to exceed the main supply voltage  $V_M$ . This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

### 7.3.2 Protection Circuits

The DRV8806 is fully protected against undervoltage, overcurrent and overtemperature events.

#### 7.3.2.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the  $t_{OCP}$  deglitch time (approximately 3.5  $\mu$ s), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the  $t_{RETRY}$  retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or  $V_M$  is removed and reapplied.

#### 7.3.2.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

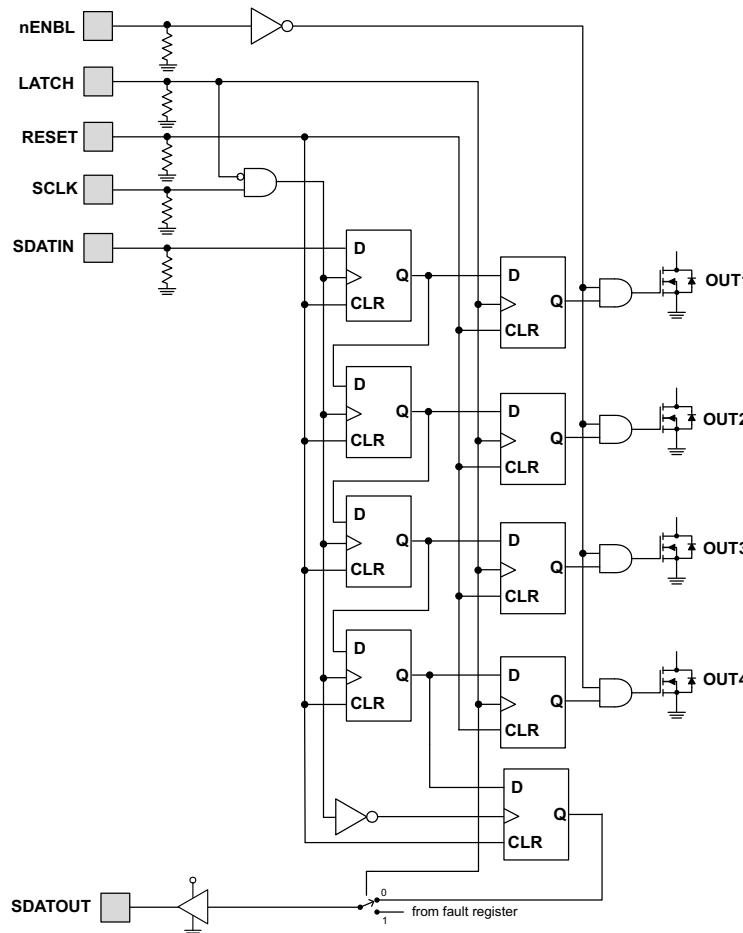
#### 7.3.2.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the  $V_M$  pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when  $V_M$  rises above the UVLO threshold.

## 7.4 Device Functional Modes

### 7.4.1 Serial Interface Operation

The DRV8806 is controlled with a simple serial interface. Logically, the interface is shown in [Figure 6](#).



**Figure 6. Serial Interface Operation**

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin, while LATCH is low. Data is shifted from the last bit to the SDATOUT pin, so multiple devices may be daisy-chained together using a single serial interface.

Note that the SDATOUT pin has a push-pull driver, which can support driving another DRV8806 SDATIN pin at clock frequencies of up to 1 MHz without an external pullup. A pullup resistor can be used between SDATOUT and an external 5-V logic supply to support higher clock frequencies. TI recommends a resistor value of approximately 1 k $\Omega$ . The SDATOUT pin is capable of approximately 1-mA source and 5-mA sink. To supply logic signals to a lower-voltage microcontroller, use a resistor divider from SDATOUT to GND.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

## Device Functional Modes (continued)

### 7.4.2 Fault Output Register

The DRV8806 contains circuitry to detect open or shorted loads. The status of the loads can be read through the serial interface. The logic is shown in Figure 7.

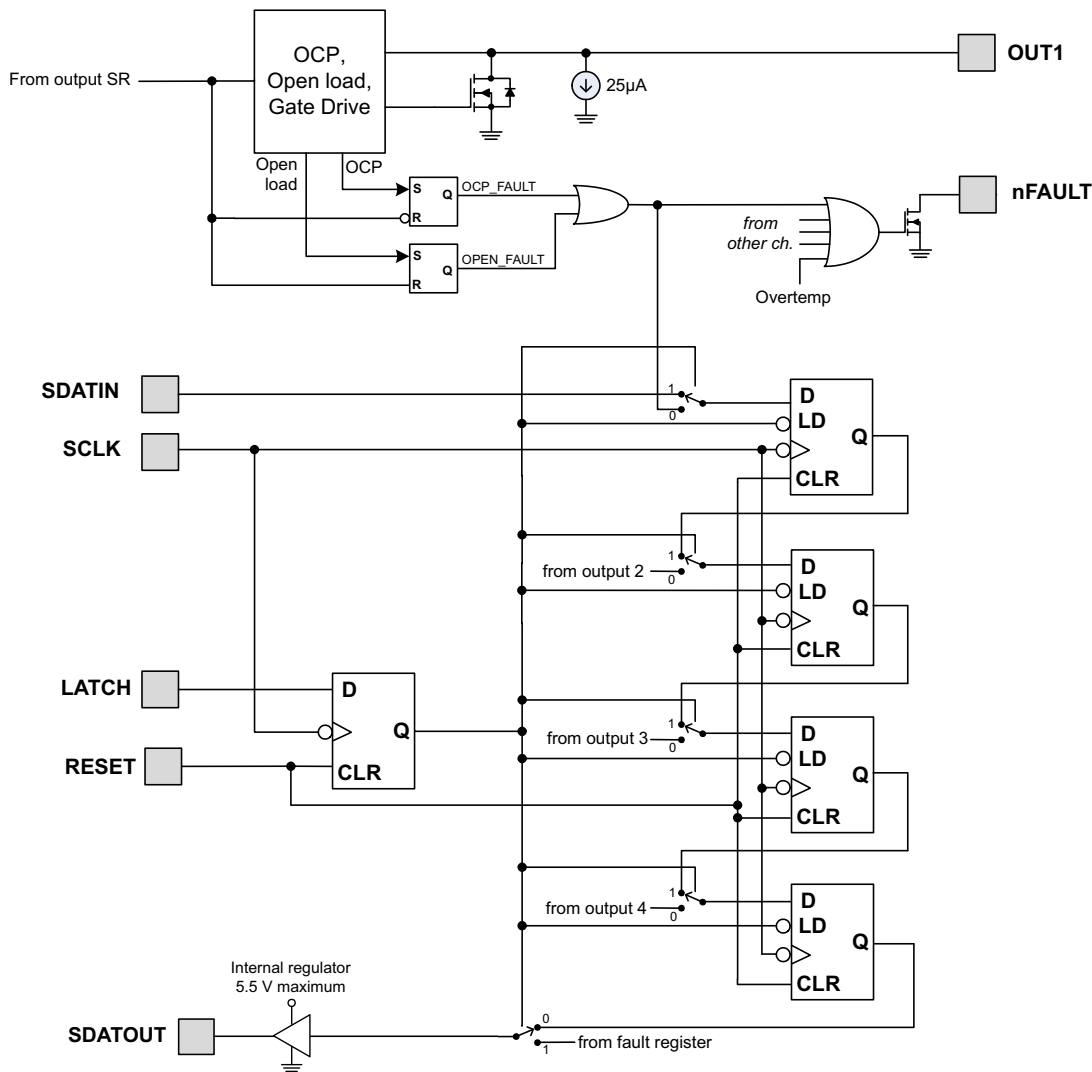


Figure 7. Fault Output

To overcome any leakage currents to accurately sense an open load, a small current source is connected to each output pin. This source pulls approximately 25-µA of current to ground. The voltage on the output pin is sensed during the time that the output is off, and if the voltage on the pin is less than 1.2 V (indicating that there is no load connected) after the open load deglitch time, the OPEN\_FAULT latch is set. This latch is cleared whenever the output bit is set.

When the output is turned on, if an overcurrent (OCP) fault is detected, the channel will be turned off and the OCP\_FAULT latch is set. This latch will be cleared whenever the output bit is cleared.

The state of the OCP\_FAULT and OPEN\_FAULT signals is combined into a single fault bit per channel, and loaded into a shift register while the LATCH pin is low. When the LATCH pin is taken high, the fault data is latched into the shift register at the first falling edge of SCLK. Data may then be shifted out on the SDATOUT pin on each falling edge of the SCLK pin.

Note that the LATCH signal must be high for a minimum of 200 ns before valid data can be clocked out.

### Device Functional Modes (continued)

The nFAULT pin will be driven active low whenever any of the OCP\_FAULT or OPEN\_FAULT latches are set, as well as whenever there is an overtemperature condition.

#### 7.4.3 Daisy-Chain Connection

Two or more DRV8806 devices may be connected together to use a single serial interface. The SDATOUT pin of the first device in the chain is connected to the SDATIN pin of the next device. The SCLK, LATCH, RESET, and nFAULT pins are connected together.

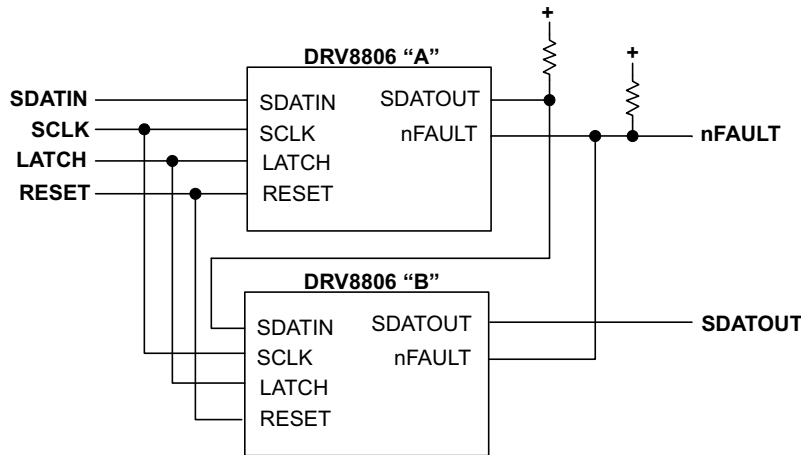


Figure 8. Daisy-Chain Connection

Figure 9 shows an example of a serial transaction, writing the output bits, and then reading the fault status bits, using two devices connected together in a daisy-chain.

Note that the LATCH signal must be high for a minimum of 200 ns before valid data can be clocked out.

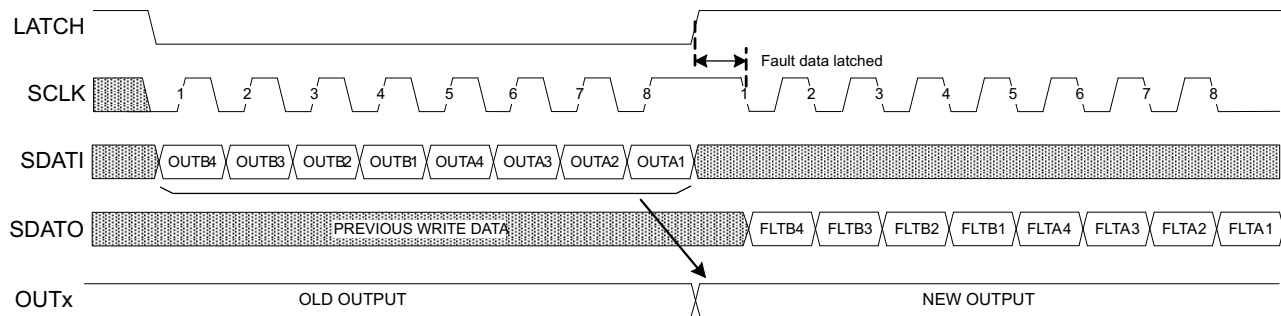


Figure 9. Daisy-Chain Serial Transaction

#### 7.4.4 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power up.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DRV8806 can be used to drive one unipolar stepper motor.

### 8.2 Typical Application

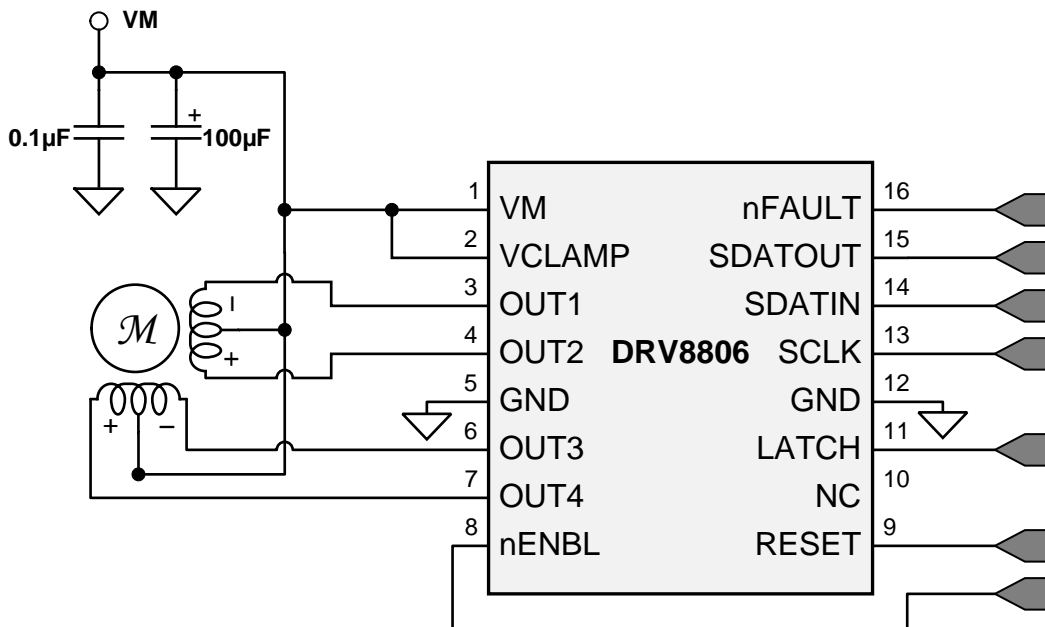


Figure 10. DRV8806 Typical Application

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, $V_M$	24 V
Motor winding resistance, $R_L$	7.4 $\Omega$ /phase
Motor full step angle, $\theta_{step}$	1.8°/step
Motor rated current, $I_{RATED}$	0.75 A
SCLK frequency, $f_{SCLK}$	1 MHz

#### 8.2.2 Detailed Design Procedure

##### 8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

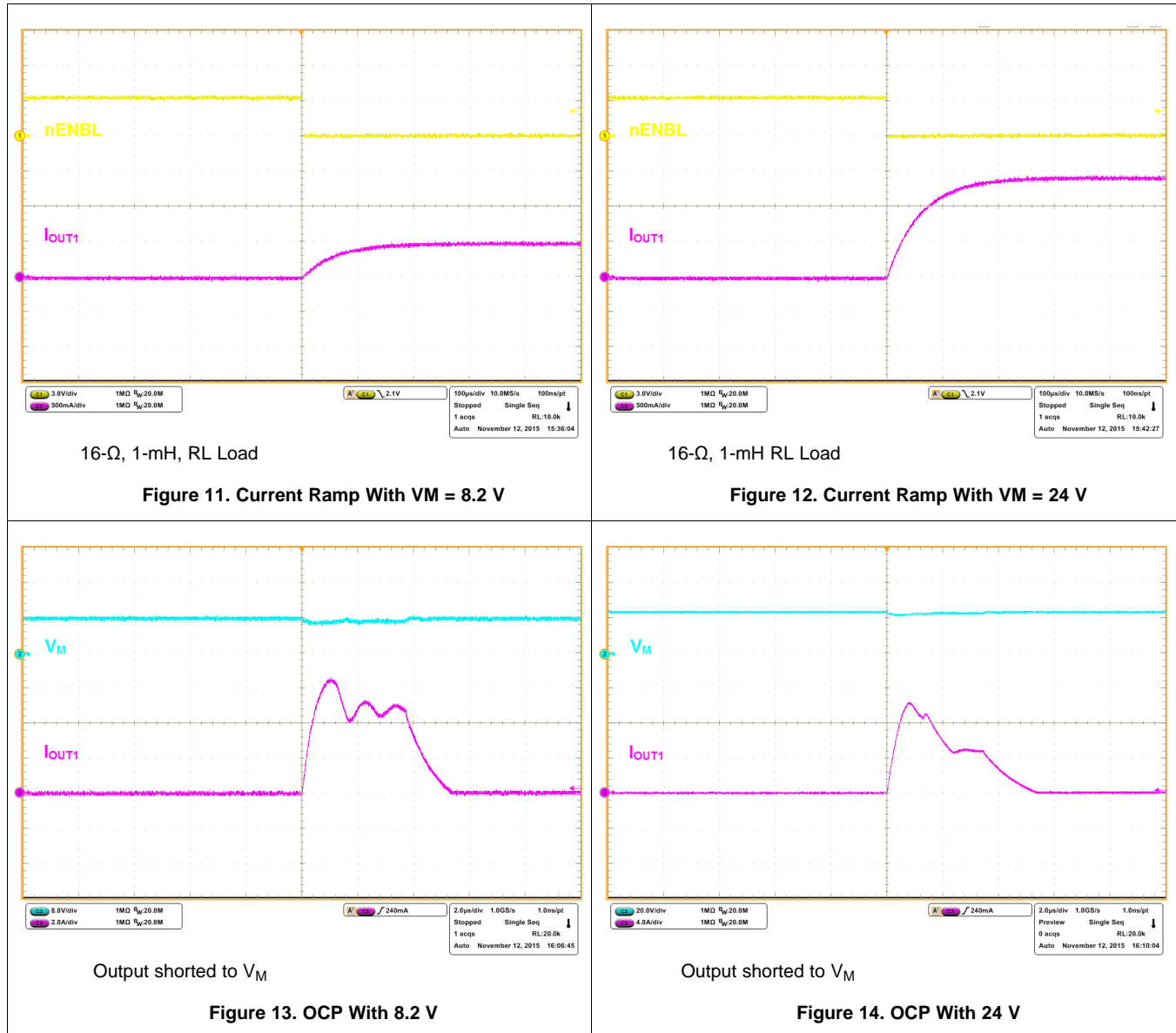
### 8.2.2.2 Drive Current

The current path starts from the supply  $V_M$ , moves through the inductive winding load, and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

$$P = I^2 \times R_{DS(on)} \tag{1}$$

The DRV8806 has been measured to be capable of 2-A Single Channel or 1-A Four Channels in a HTSSOP package at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

### 8.2.3 Application Curves



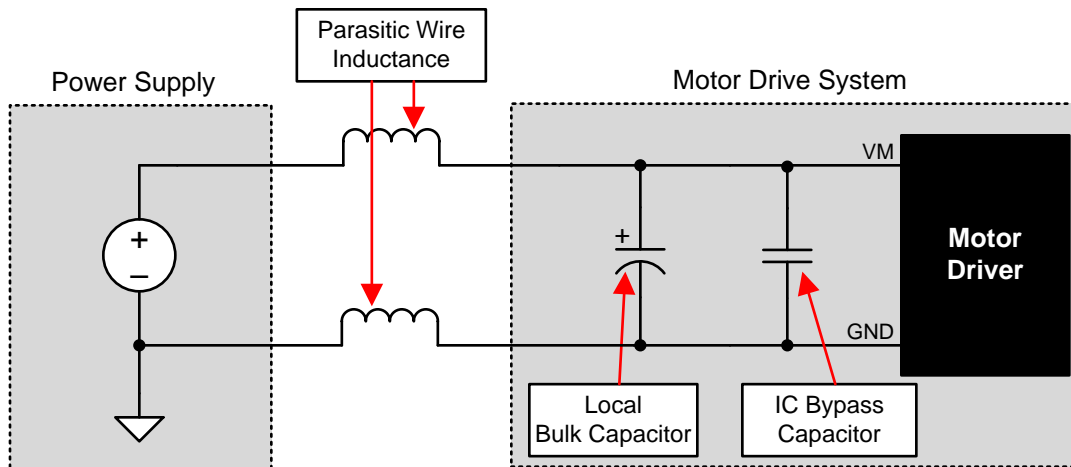
## 9 Power Supply Recommendations

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance needed depends on a variety of factors, including

- Highest current required by the motor system
- Power supply's capacitance and ability to source current
- Amount of parasitic inductance between the power supply and motor system
- Acceptable voltage ripple
- Type of motor used (Brushed DC, Brushless DC, Stepper)
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.



**Figure 15. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

## 10 Layout

### 10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the  $I^2 \times R_{DS(on)}$  heat that is generated in the device.

### 10.2 Layout Example

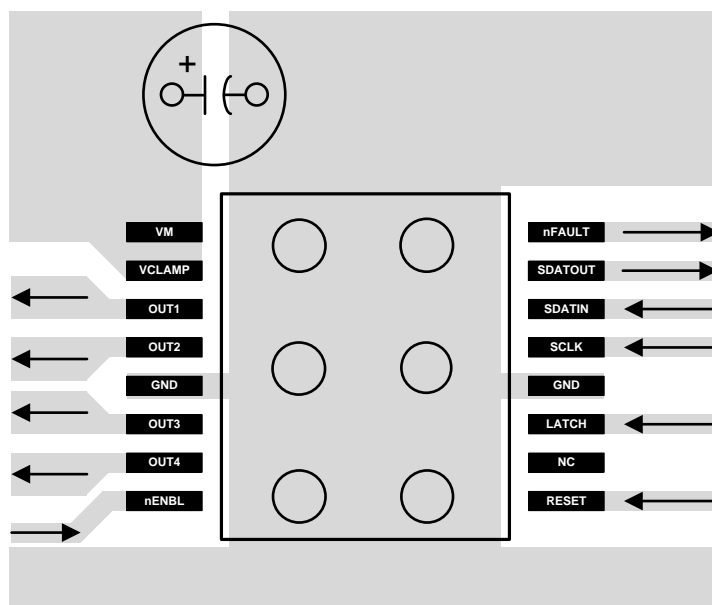


Figure 16. Layout Recommendation

### 10.3 Thermal Considerations

The DRV8806 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

#### 10.3.1 Power Dissipation

Power dissipation in the DRV8806 is dominated by the power dissipated in the output FET resistance, or  $R_{DS(ON)}$ . Average power dissipation of each FET when running a static load can be roughly estimated by Equation 2:

$$P = R_{DS(ON)} \cdot (I_{OUT})^2$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$  is the resistance of each FET
- $I_{OUT}$  is equal to the average current drawn by the load

(2)



## Thermal Considerations (continued)

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be considered. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that  $R_{DS(ON)}$  increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### 10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at [www.ti.com](http://www.ti.com).

In general, the more copper area that can be provided, the more power can be dissipated.

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package* [SLMA002](#)
- *PowerPAD™ Made Easy* [SLMA004](#)

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8806PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8806	<a href="#">Samples</a>
DRV8806PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8806	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

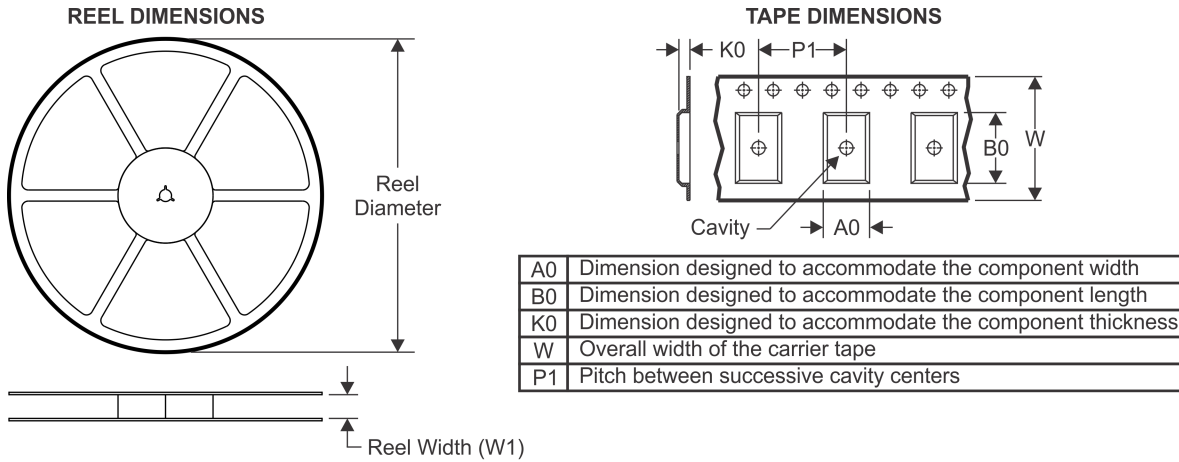
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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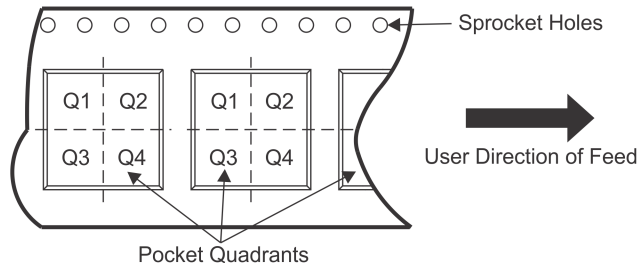
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



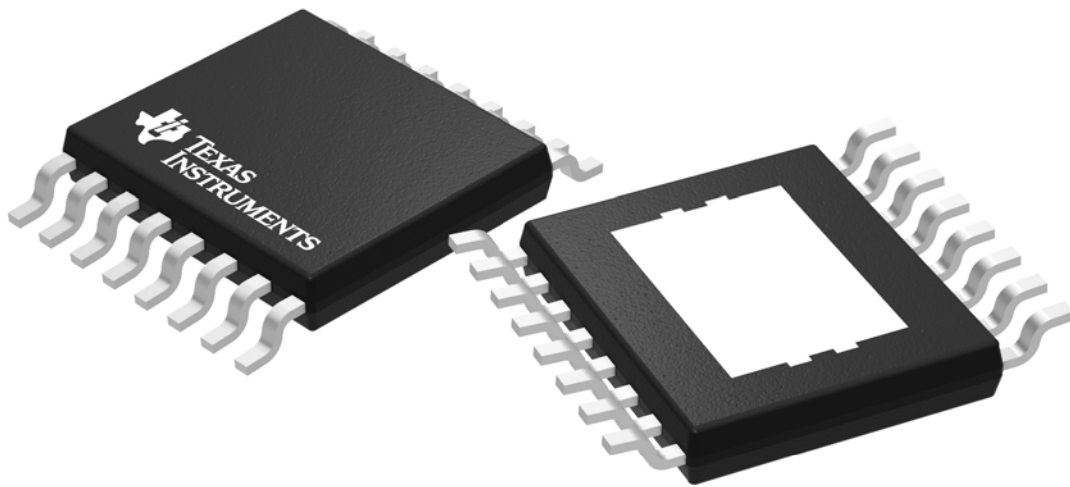
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8806PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

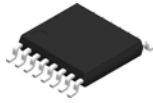

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8806PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

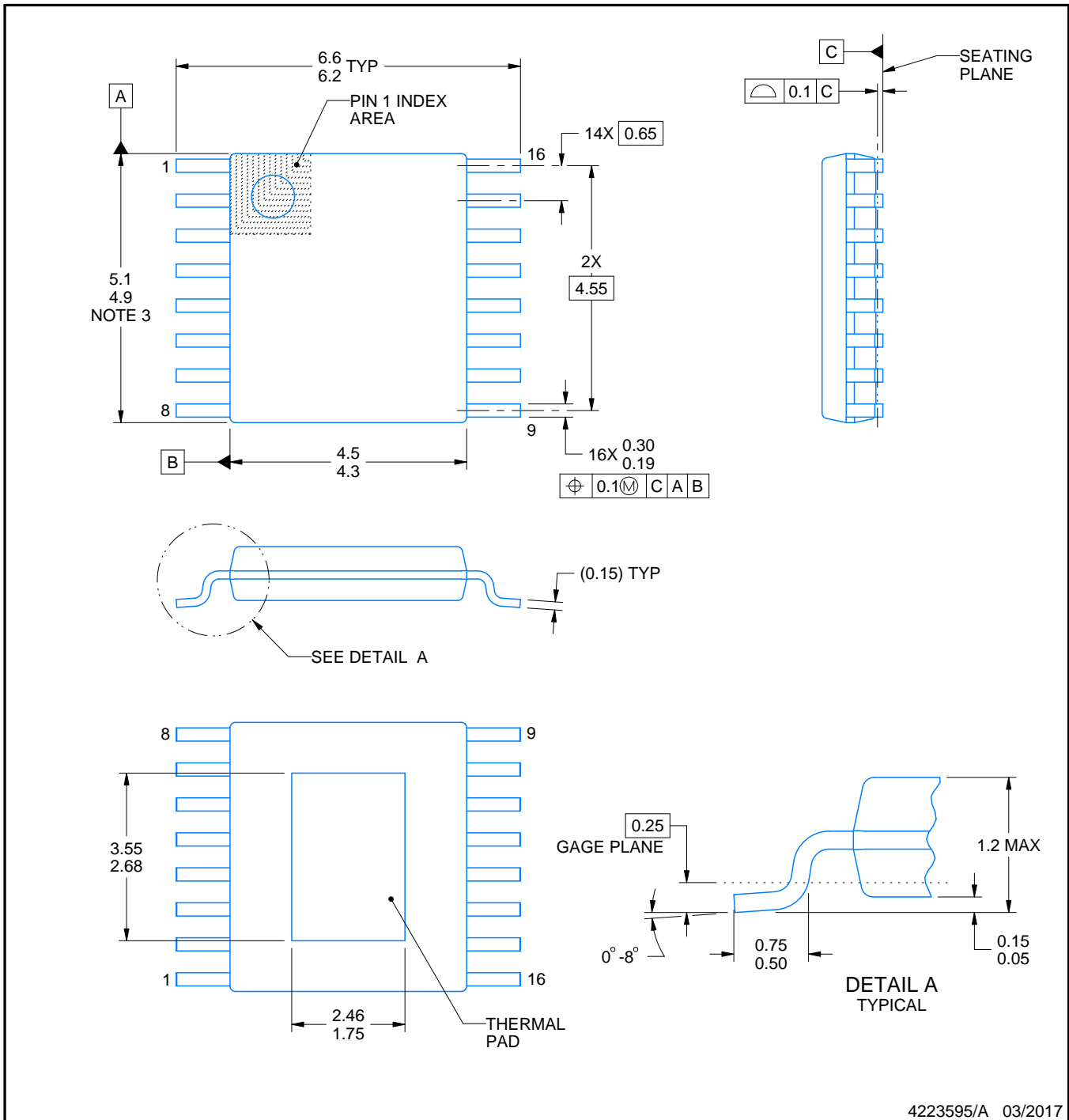
PWP0016J



# PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

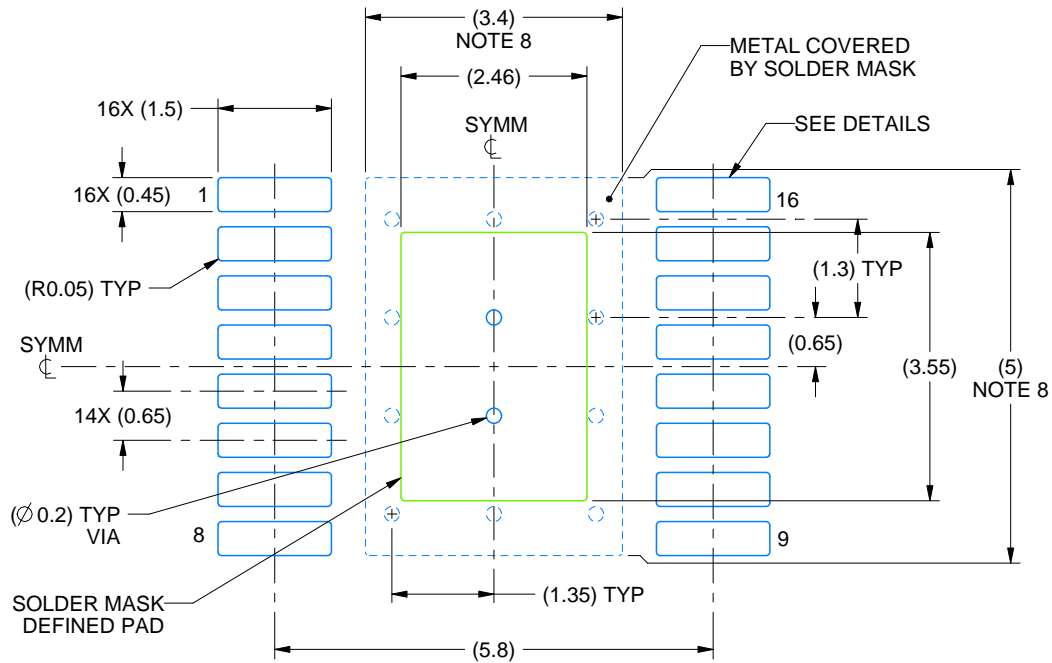


# EXAMPLE BOARD LAYOUT

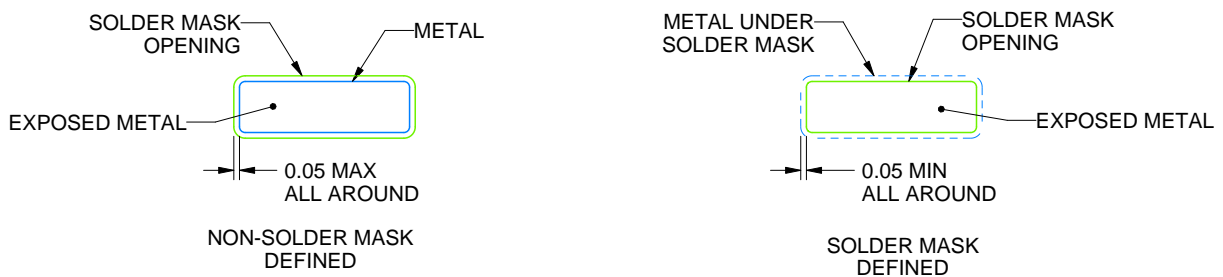
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

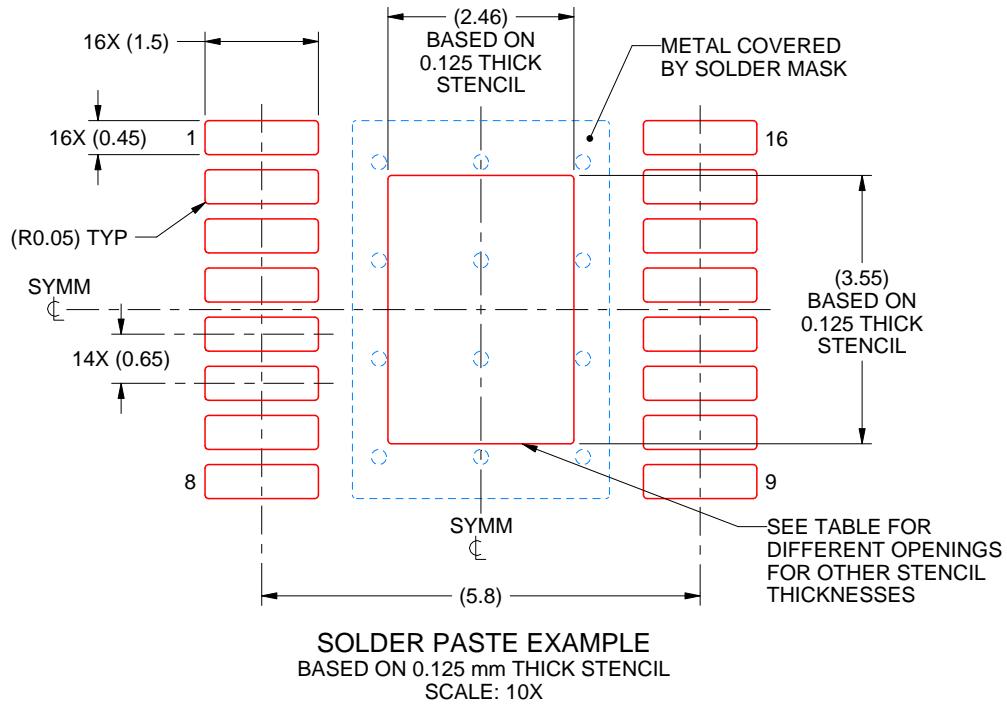
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

- 10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 11. Board assembly site may have different recommendations for stencil design.

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