DRV8808 Combination Motor Driver With DC-DC Converter

1 Features

- Three DC Motor Drivers
  - Up to 2.5-A Current Chopping
  - Low Typical ON Resistance (R_{DSON} = 0.5 Ω at T_J = 25°C)
- Three Integrated DC-DC Converters
  - ON/OFF Selectable Using CSELECT Pin and Serial Interface
  - Outputs Configurable With External Resistor Network From 1 V to 90% of V_M Capability for All Three Channels
  - 1.35-A Output Capability for All Three Channels
- One Integrated LDO Regulator
  - Output Configurable With External Resistor Network from 1 V to 2.5 V
  - 550-mA Output Capability
- 7-V to 40-V Operating Range
- Serial Interface for Communications
- Thermally Enhanced Surface-Mount Package 48-Pin HTSSOP With PowerPAD™ (Eco-Friendly: RoHS and No Sb/Br)
- Power-Down Function (Deep-Sleep Mode)
- Reset Signal Output (Active Low)
- Reset (All Clear) Control Input

2 Applications

- Printers
- Document Scanners
- POS
- Copiers

3 Description

The DRV8808 device provides the integrated motor driver solution for printers. The chip has three full H-bridges and three buck DC-DC converters.

The output driver block for each consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings. The device can be configured to use internal or external current sense for winding current control.

The SPI input pins are 3.3-V compatible and have inputs that are 5-V tolerant.

The DRV8808 has three DC-DC switched-mode buck converters to generate a programmable output voltage from 1 V up to 90% of V_M, with up to 1.35-A load current capability.

The device is configured using the CSELECT terminal at start-up, and serial interface during run time.

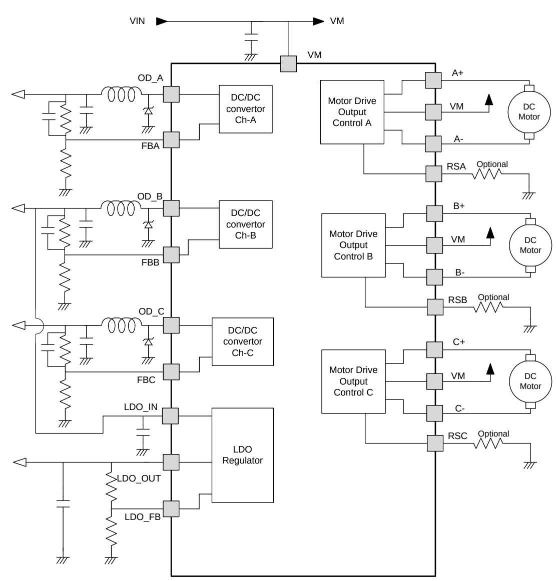
An internal shutdown function is provided for overcurrent protection, short-circuit protection, undervoltage lockout, and thermal shutdown. Also, the device has the reset function at power on, and the input on the nReset pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8808	HTSSOP (48)	12.50 mm x 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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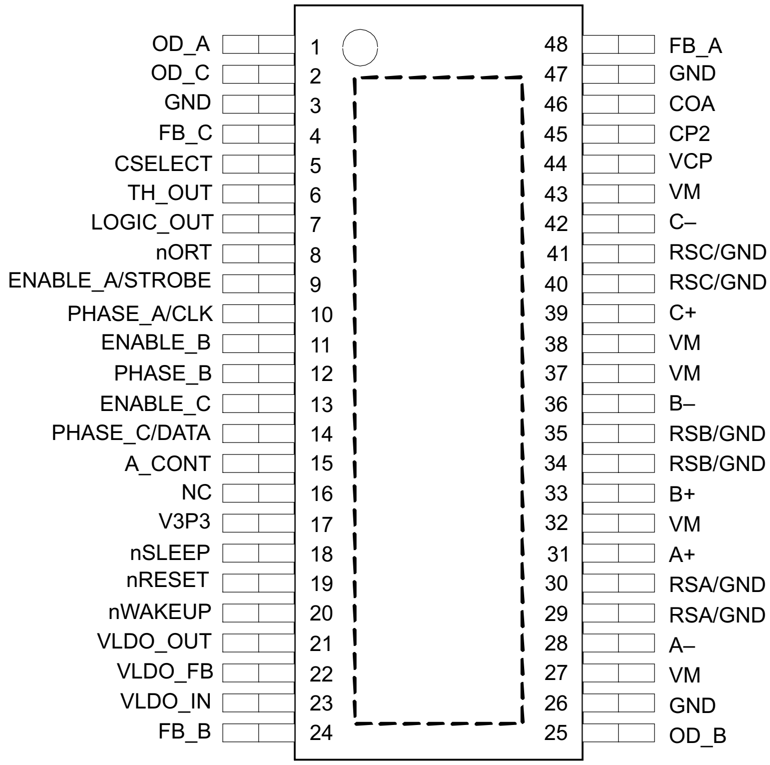
4 Revision History

Changes from Revision A (August 2011) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

5 Pin Configuration and Functions

DCA Package
48-Pins HTSSOP
Top View



Pin Functions

PIN		I/O	PU/PD	SHUNT R	DESCRIPTION
NAME	NO.				
A-	28	O	—	—	Motor drive output for winding A-
A+	31	O	—	—	Motor drive output for winding A+
A_CONT	15	I	Down	100k	DC-DC A converter control (L = Enable)
B-	36	O	—	—	Motor drive output for winding B-
B+	33	O	—	—	Motor drive output for winding B+
C-	42	O	—	—	Motor drive output for winding C-
C+	39	O	—	—	Motor drive output for winding C+
CP1	46	O	—	—	Charge pump bucket capacitor output (low side)
CP2	45	O	—	—	Charge pump bucket capacitor output (high side)
CSELECT	5	I	Up	200k	DC-DC converter startup selector
ENA / STB	9	I	Down	100k	Enable input for DC motor A control / SPI STROBE
ENB	11	I	Down	100k	Enable input for DC motor B control
ENC	13	I	Down	100k	Enable input for DC motor C control
FB_A	48	I	—	—	Feedback signal for DC-DC converter A
FB_B	24	I	—	—	Feedback signal for DC-DC converter B
FB_C	4	I	—	—	Feedback signal for DC-DC converter C
GND	3	—	—	—	Ground
GND	26	—	—	—	Ground
GND	47	—	—	—	Ground

Pin Functions (continued)

PIN		I/O	PU/PD	SHUNT R	DESCRIPTION
NAME	NO.				
LOGIC_OUT	7	O	—	—	Information monitoring output (open drain)
NC	16	NC	—	—	Do not connect
nORT	8	O	—	—	Reset output (open drain)
nReset	19	I	Up	200k	Reset input (L: reset, H/open: normal operation)
nSLEEP	18	I	Down	100k	Enable/disable, SPI selector
nWAKEUP	20	I	Up	200k	Wake-up pin for DeepSleep mode (L = WAKEUP)
OD_A	1	O	—	—	Output for DC-DC switch mode regulator A
OD_B	25	O	—	—	Output for DC-DC switch mode regulator B
OD_C	2	O	—	—	Output for DC-DC switch mode regulator C
PHA / CLK	10	I	Down	100k	Phase input for DC motor A control / SPI CLOCK
PHB	12	I	Down	100k	Phase input for DC motor B control
PHC / DATA	14	I	Down	100k	Phase input for DC motor C control / SPI DATA
RSA / GND	30	O	—	—	Motor drive current sensing resistor A / GND power
RSKA / GND	29	I	—	—	Motor drive current sensing resistor A / GND Kelvin
RSB / GND	35	O	—	—	Motor drive current sensing resistor B / GND power
RSKB / GND	34	I	—	—	Motor drive current sensing resistor B / GND Kelvin
RSC / GND	41	O	—	—	Motor drive current sensing resistor C / GND power
RSKC / GND	40	I	—	—	Motor drive current sensing resistor C / GND Kelvin
TH_OUT	6	O	—	—	Temperature warning output (open drain)
V3p3	17	O	—	—	Bypass for internal 3.3-V regulator
VCP	44	O	—	—	Charge pump output
VLDO_FB	22	I	—	—	LDO voltage regulator feed back
VLDO_IN	23	I	—	—	LDO voltage regulator input
VLDO_OUT	21	O	—	—	LDO voltage regulator output
VM	27	—	—	—	Voltage supply for motors and regulators
VM	32	—	—	—	Voltage supply for motors and regulators
VM	37	—	—	—	Voltage supply for motors and regulators
VM	38	—	—	—	Voltage supply for motors and regulators
VM	43	—	—	—	Voltage supply for motors and regulators

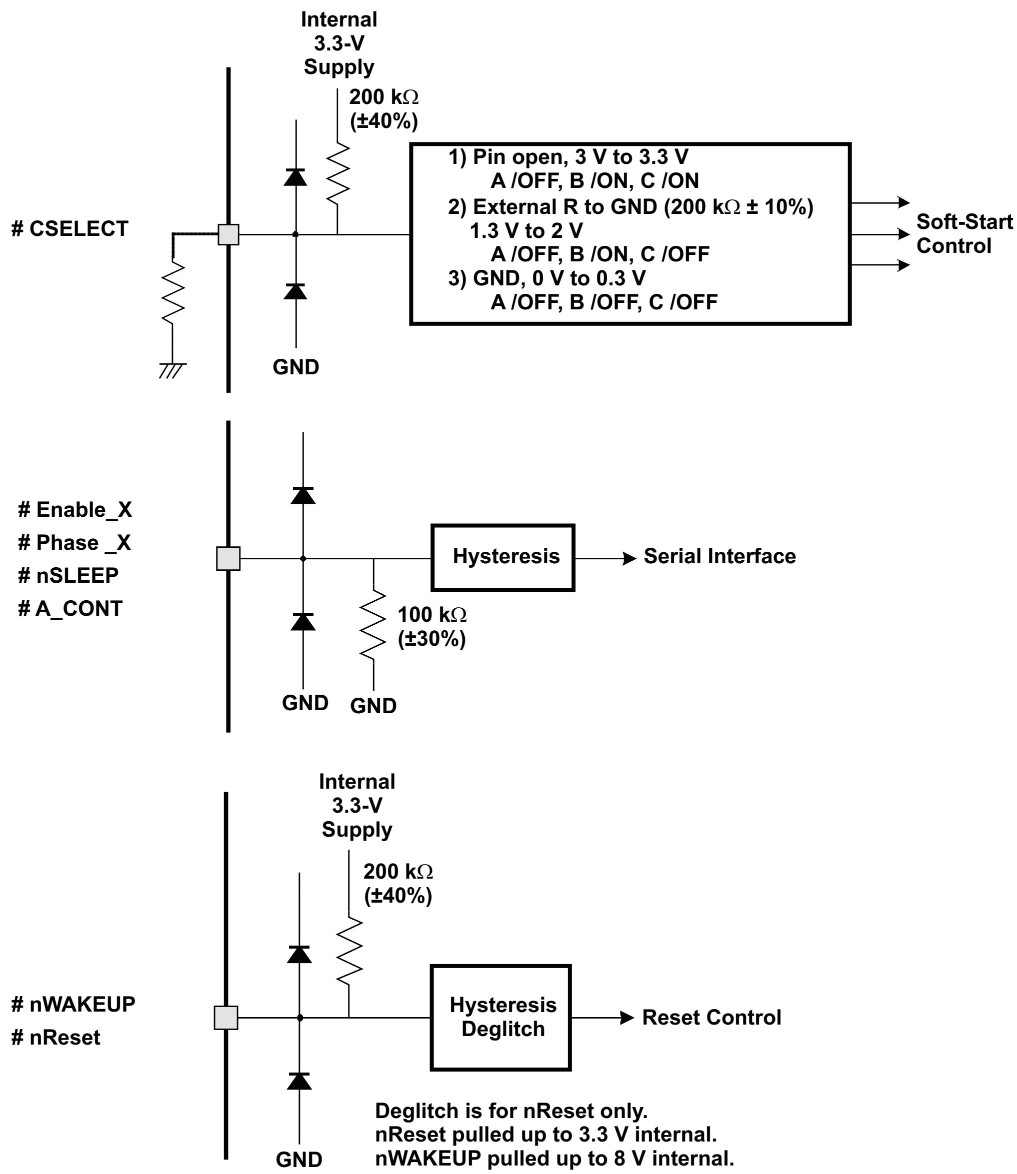


Figure 1. Input Pin Configuration

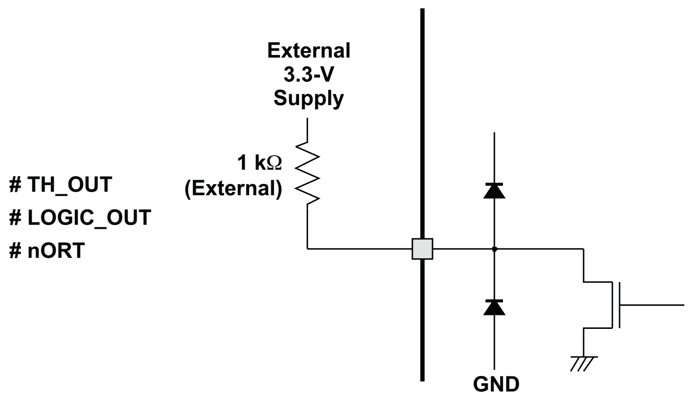


Figure 2. Open-Drain Output Pin Configuration

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_M	Supply voltage		40	V
	Logic input voltage, serial I/F, A_CONT, nReset, and so forth [2]	–0.3	5.5	V
	TH_OUT, nORT, LOGIC_OUT, CSELECT	–0.3	3.6	V
	nWAKEUP	–0.3	8	V
	Continuous total power dissipation (in case $θ_{JA}$ = 20°C/W)		4	W
	Continuous motor-drive output current for each H-bridge (100 ms)		2.5	A
	Continuous DC-DC converter output current[3]		1.35	A
T_J	Operating junction temperature (1 hour)		190	°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The negative spike less than –5 V and narrower than 50-ns width should not cause any problem.
(3) May shut down due to regulator OCP.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage range, V_M for motor control	18	27	38	V
Supply voltage range for DC-DC converter (V_M)	7	27	38	V
Operating ambient temperature range	–10		85	°C
Operating junction temperature range	0		135	°C

6.4 Thermal Information

THERMAL METRIC[1]		DRV8808 HTSSOP (DCA) 48 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	28.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	15.6	
$R_{θJB}$	Junction-to-board thermal resistance	10.2	
$ψ_{JT}$	Junction-to-top characterization parameter	0.3	
$ψ_{JB}$	Junction-to-board characterization parameter	10.1	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = 0°C to 135°C, V_M = 7 V to 38 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY (SLEEP) CURRENT							
I_{SLEEP1}	Supply (sleep) current 1	nSLEEP = L,	DC-DC all off		3	5.5	mA
I_{SLEEP2}	Supply (sleep) current 2	nSLEEP = L, Regulators enabled	V_M = 8 V, No load		6	8	mA
I_{SLEEP3}	Supply (sleep) current 3	nSLEEP = L, Regulators enabled	V_M = 38 V, No load		6	8	mA
I_{DEEP_SL}	Supply (deep sleep) current [(1)]	V_M = 38 V			0.7	1	mA
DIGITAL INTERFACE CIRCUIT							
V_{IH}	Digital high-level input voltage	Digital inputs		2		3.6	V
I_{IH}	Digital high-level input current	Digital inputs				100	µA
V_{IL}	Digital low-level input voltage	Digital inputs				0.8	V
I_{IL}	Digital low-level input current	Digital inputs				100	µA
V_{hys}	Digital input hysteresis	Digital inputs			0.45		V
T_{deg_nReset}	nReset input deglitch time			2.5		7.5	µs
T_{filt_ACONT}	A_CONT filter time [(2)]			30		70	µs
CHARGE-PUMP VCP (CP = 0.1 µF to 0.47 µF, Cblk = 0.01 µF ±20%)							
V_O(CP)	Output voltage	I_{LOAD} = 0 mA,	V_M > 15 V	V_M + 10		V_M + 13	V
f(CP)	Switching frequency				1.6		MHz
t_{start}	Start-up time	$C_{Storage}$ = 0.1 µF,	V_M ≥ 15 V		0.5	2	ms
V3P3 OUTPUT							
V_{3p3}	Output voltage [(3)]			3	3.3	3.6	V
C_{bypass}	Output capacitor			0.08	0.1	10	µF
INTERNAL CLOCK OSCI							
f_{OSCi}	System clock rrequency			5.76	6.4	7.04	MHz
CSELECT FOR DC-DC STARTUP SELECTION							
V_{CS0}	DC-DC all off			0		0.3	V
V_{CS1}	Turn ON ODB	Pull down by external 200-kΩ resistor		1.3		2	V
V_{CS2}	Turn ON ODB then ODC	As pin open		3		3.6	V
VLDO REGULATOR [(4)(5)(6)]							
$VLDO_{IN}$	LDO input voltage			3		3.6	V
$VLDO_{FB}$	Feedback voltage				1		V
$VLDO_{OUT}$	Output voltage range	1 V ≤ $VLDO_{OUT}$ ≤ 1.8 V			±5%		
		1.8 V ≤ $VLDO_{OUT}$ ≤ 2.5 V			±3%		
I_{OUT}	Load capability					500	mA
I_{OCP}	OCP current				725	1100	mA
t_{Ideg}	OCP deglitch			3	8	13	µs
V_{ovp}	Overvoltage protection	% to nominal Voutx detected at VFB (VFB increasing)		25%	30%	35%	
V_{uvp}	Undervoltage protection	% to nominal Voutx detected at VFB (VFB decreasing)		–25%	–30%	–35%	

(1) Deep Sleep shuts down majority of the device and runs minimal circuits (internal bias circuits and the nWAKEUP pin). Deep Sleep is entered by writing 1 to Setup Register, Bank 1, Bit 11. Device is restarted by pulling nWAKEUP pin low or power cycling V_M. Deep Sleep functionality only available for V_M > Vth_{VM+}.
(2) A_CONT is filtered for both high and low levels.
(3) V3p3 bypass pin is not meant to be used as a supply.
(4) LDO can be bypassed by either load configuration 1 or 2.
(5) Typical values for external components should be chosen such that when the tolerance is added to the typical, the values remain between the maximum and minimum specifications listed.
(6) When LDO is not used, recommend connecting VLDO_IN to GND, VLDO_OUT to GND, and VLDO_FB to FB_B.

Electrical Characteristics (continued)

T_J = 0°C to 135°C, V_M = 7 V to 38 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{Vdeg}	UVP/OVP deglitch time			3	8	13	µs
C_{L1}	Load bypass configuration 1	Electrolytic load capacitance		27		120	µF
C_{ESR1}		ESR of load capacitance		0.05		2	Ω
C_{C1}		Ceramic load capacitance		0		0.4	µF
C_{L2}	Load bypass configuration 2	Electrolytic load capacitance		80	100	120	µF
C_{ESR2}		ESR of load capacitance		0.05		0.2	Ω
C_{C2}		Ceramic load capacitance		0		3	µF
THREE DC-DC CONVERTER							
$V_{M\ OPE\_X}$	Operating supply voltage range ratio to V_{OUT}	I_O < 0.6 A	Vth $_{VM-}$ < V_M < 7 V			0.8 x V_M	V
			20 V < V_M < 38 V			0.9 x V_M	
ODx	Regulator output voltage	20 V < V_M < 40 V	0℃ < T_J < 125℃	-3%	V_O	3%	
			125℃ < T_J < 135℃	-4%	V_O	4%	
		6.5 V < V_M < 20 V		-5%	V_O	5%	
		V_M = 7 V, V_O = 5.5 V		-5%	V_O	5%	
		V_M = 7 V, V_O = 1 V	0℃ < T_J < 125℃	-3%	V_O	3%	
			125℃ < T_J < 135℃	-4%	V_O	4%	
		Vth_{VM-} < V_M < 6.5 V , V_O ≤ 3.3 V		-5%	V_O	5%	
FBx	FBx pin voltage				1		V
$I_{O\ ODx}$	Output current (DC)	V_M > 15 V				1.35	A
$I_{O\ ODx2}$	Output current (DC) at low V_M	V_M = 7 V, V_O = 5.5 V				0.6	A
$I_{O\ ODx3}$	Output current (DC) at low V_M	V_M = 7 V, V_O = 3.3 V				1.2	A
R_{DSON} (7)	FET on-resistance at 0.8 A for OD_x V_M > 15 V	T_J = 70 °C			0.85	1.05	Ω
		T_J = 135 °C			1	1.2	
L	Inductor	V_{OUT} = 1.0 V			150		µH
		V_{OUT} ≥ 3.3 V			330		
C	Capacitor	V_{OUT} = 1.0 V		270		330	µF
		V_{OUT} ≥ 3.3 V			220		
THREE DC-DC CONVERTER PROTECTION							
$I_{O\ DD\ ODx}$	Overcurrent detect for OD_x source	Peak current in each ON cycle		1.35		2.7	A
t_{ODXdeg}	Cycle by cycle Idetect deglitch			100	200	400	ns
t_{ODXSD}	DC-DC shutdown filter	Number of consecutive cycles with Idetect			4		chop cycles
V_{ovpx}	Overvoltage protection	% to nominal Voutx detected at VFB (VFB increasing)		25%	30%	35%	
V_{uvpx}	Undervoltage protection	% to nominal Voutx detected at VFB (VFB decreasing)		–25%	–30%	–35%	
t_{VXdeg}	UVP/OVP deglitch time			3	8	13	µs
t_{sst}	Start-up time with soft start					56	ms
V_{stover}	Start-up overshoot	Ratio to Vo				3%	
V_M SUPERVISORY (8) (9)							
$Vth_{VM–}$	nORT, for V_M low threshold	V_M decreasing		4.5	5	6	V
Vth_{VM+}	nORT, for V_M high threshold	V_M increasing		5.5	6	6.79	V

(7) R_{DSON} at T = 135°C guaranteed by characterization. Production test will be done at T = 25°C/70°C.
(8) V_M must be V_M > Vth_{VM+} to start up internal DC-DC converter.
(9) When V_M goes down below Vth_{VM+}, the VUVPx (undervoltage protection in DC-DC) are masked. The DC-DC converter is shut off by nORT assertion at $Vth_{VM\ –}$.

Electrical Characteristics (continued)

T_J = 0°C to 135°C, V_M = 7 V to 38 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vth_{VMh}	nORT, for V_M detect hysteresis	$Vth_{VM+} – Vth_{VM–}$	0.5	1		V
Vth_{VM2}	For motor driver off(10)				15	V
t_{VMfilt}	Vth V_M monitor filtering time	For Vth V_M detect	4		30	µs
$t_{VM2filt}$	Vth V_{M2} monitor filtering time	For Vth V_{M2} detect	30		60	ms
THERMAL SHUTDOWN: TSD (11) (12)						
T_{TSD}	Thermal shutdown set points		150	170	190	°C
t_{TSDdeg}	TSD deglitch time		30	60	90	µs
TEMPERATURE WARNING: PRE-TSD(13) (12)						
PreTSD	Temperature warning	Assert at TH_OUT pin	115	135	155	°C
OPEN-DRAIN OUTPUTS (NORT, LOGIC_OUT, TH_OUT)						
V_{OH}	High-state voltage	RL = 1 kΩ to 3.3 V	3			V
V_{OL} (14)	Low-state voltage	RL = 1 kΩ to 3.3 V			0.3	V
I_{OL} (14)	Low-state sink current	Vo = 0.25 V	2			mA
t_r (15)	Rise time	10% to 90%			1	µs
t_f (15)	Fall time	90% to 10%			50	ns
NORT DELAY: STARTUP SEQUENCE (16) (17)						
Tord1	nORT delay 1	Reset deassertion from $Vth_{VM+} < V_M$, for DC/DC wake up failing	200	300	390	ms
Tord3	DC-DC turn on delay	From one DC-DC wake up to following DC-DC to go soft-start sequence	5	10	15	ms
Tord4	nORT delay 4	Reset deassertion from 2nd DC-DC wake up	60	120	180	ms
NRESET INPUT(16)						
Treset	nReset assertion to nORT assertion delay	nReset falling to nORT failing		5	10	µs
H-BRIDGE DRIVERS (OUTX+ AND OUTX–) CONDITION: V_M = 15 V to 38 V (18)						
$I_{OUT1(max)}$	Peak output current 1	Less than 500-ns period			6.8	A
$I_{OUT2(max)}$	Peak output current 2	Less than 100-ms period			2.42	A
R_{DSON}	FET ON resistance at 0.8 A	T_J = 70°C		0.55	0.65	Ω
		T_J = 135°C		0.7	0.85	
I_{CEX}	Output leakage current	VOUTX = 0 V or 10			10	µA
$I_{OC\ Motor}$	Motor overcurrent threshold for each H-bridge (18)		3		8	A
Fchop	Motor chopping frequency = FOSCM/8		90	100	110	kHz
DC MOTOR DRIVERS						
t_r	Rise time	V_M = 35 V 20% to 80%	50		200	ns
t_f	Fall time	V_M = 35 V 20% to 80%	50		200	ns
t_{PDOFF}	Enable or strobe detection to sink or source gate OFF delay		50	150	400	ns

(10) No nORT assertion to Vth_{VM2} detection.
(11) TSD does not need thermal hysteresis.
(12) Parametric guaranteed by characterization. Not tested in production.
(13) PreTSD does not need thermal hysteresis.
(14) Production test only measures Vol and Iol to ensure timing.
(15) t_r and t_f dominated by external capacitance, pullup resistance, and open-drain NMOS R_{DSON}.
(16) This includes asynchronous timing deviation between the event to the timer clock.
(17) nORT assertion delay is configurable and defined in the serial register section.
(18) When the overcurrent is detected, all the H-bridges are shut down and assert nORT per shutdown configuration.

Electrical Characteristics (continued)

T_J = 0°C to 135°C, V_M = 7 V to 38 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{COD}	Crossover delay time to prevent shoot through		100 [19]	600	1000	ns
t_{PDON}	Enable or strobe detection to sink or source gate ON delay			750		ns
t_{ldeg}	MISD BLANK	[00] [20]	1.80	2.25	2.95	µs
		[01] [21]	1.20	1.50	2.30	
		[10] [22]	2.35	3.00	3.65	
		[11] [23]	2.95	3.75	4.30	
T_{blank}	TBLANK	[00] [24]	3.05	3.45	5.50	µs
		[01] [25]	1.90	2.20	4.15	
		[10] [26]	4.15	4.70	6.75	
		[11] [27]	5.30	5.95	8.25	
VRS_{TRIP}	Internal current trip	00	1.18	1.4	1.62	A
		01	1.48	1.7	1.92	
		10	1.68	1.9	2.12	
		11	1.98	2.2	2.42	
	External resistor sense voltage trip threshold	00	165	185	205	mV
		01	190	210	230	
		10	240	260	280	
		11	290	310	330	
P_{minp}	Minimum pulse width (phase)	[19]			1	µs
P_{mine}	Minimum pulse width (enable)	[19]			1	µs
SERIAL INTERFACE [28]						
f(CLK)	Clock frequency				25	MHz
t_{wh}(CLK)	Minimum high-level pulse width		10			ns
t_{wl}(CLK)	Minimum low-level pulse width		10			ns
t_{dcs}	Setup time, DATA to CLK↓		10			ns
t_{dch}	Hold time, CLK↓ to DATA		10			ns
t_{dss}	Setup time, DATA to STROBE↑		10			ns
t_{dsh}	Hold time, STROBE↑ to DATA		10			ns
t_{css}	Setup time, CLK↓ to STROBE↑		20 [29]			ns
t_{csh}	Hold time, STROBE↑ to CLK↓		20 [29]			ns
t_{nss}	Setup time, nSLEEP↓ to STROBE↑		4 [30]			µs
t_{nsh}	Hold time, STROBE↑ to nSLEEP↑		10			ns
t_w(STRB)	Minimum strobe pulse width		20			ns

(19) t_{COD}, P_{minp}, and P_{mine} not production tested.
(20) 3 to 4 periods Fosc/4 + 1 Fosc
(21) 2 to 3 periods Fosc/4 + 1 Fosc
(22) 4 to 5 periods Fosc/4 + 1 Fosc
(23) 5 to 6 periods Fosc/4 + 1 Fosc
(24) 3 Fosc/8 (can add up to 1 additional Fosc/8 + 1.5 Fosc at phase or enable change due to asynchronous ambiguity)
(25) 2 Fosc/8 (can add up to 1 additional Fosc/8 + 1.5 Fosc at phase or enable change due to asynchronous ambiguity)
(26) 4 Fosc/8 (can add up to 1 additional Fosc/8 + 1.5 Fosc at phase or enable change due to asynchronous ambiguity)
(27) 5 Fosc/8 (can add up to 1 additional Fosc/8 + 1.5 Fosc at phase or enable change due to asynchronous ambiguity)
(28) Serial interface timing will not be tested parametrically in production.
(29) DATA value at STROBE is address bit for Setup and Extended Setup register so setup and hold times apply to DATA relative to STROBE. CLK and DATA also require setup and hold times relative to each other. Therefore, CLK and STROBE setup and hold timing is the summation of both.
(30) Internal filter on nSLEEP to STROBE drives this specification.

Electrical Characteristics (continued)

T_J = 0°C to 135°C, V_M = 7 V to 38 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE: ID MONITOR FUNCTION AT LOGIC_OUT PIN, EXTENDED SETUP MODE (31)						
t_{ODL}	0 data output delay bit 3 to 0 (ext-setup) = (1100)	From strobe rise to Logic_out (1 kΩ to external 3.3 V)			4000	ns
t_{ODH}	1 data output delay bit 3 to 0 (ext-setup) = (1111)				4000	ns

(31) Serial interface timing will not be tested parametrically in production.

6.6 Typical Characteristics

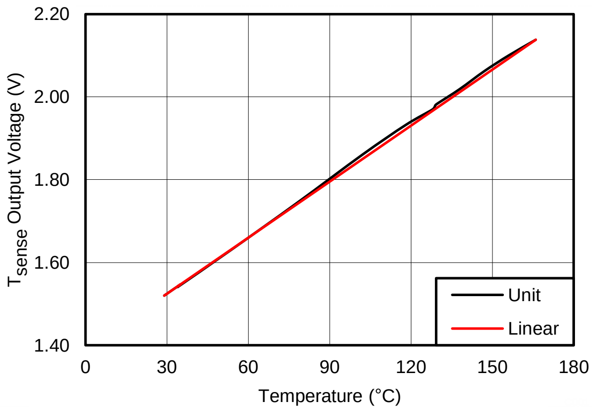


Figure 3. Tsense (Analog Out) Temperate Coefficient: Voltage Plot Example (Typical)

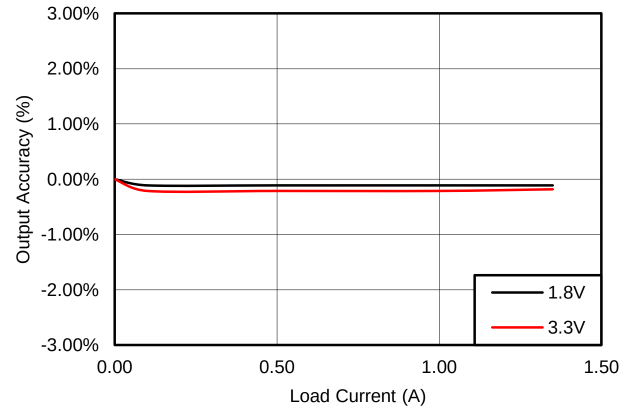


Figure 4. DC-DC Converter - DC Load Regulation Example (Typical)

7 Detailed Description

7.1 Overview

The Combo Motor Driver provides the integrated motor driver solution for printers and other applications. The chip has three full H-bridges and three Buck DC-DC converters, and one LDO.

The output driver block for each consists of N-channel power MOSFET's configured as full H-bridges to drive the motor windings. Device can be configured to utilize internal or external current sense for winding current control.

The SPI input pins are 3.3-V compatible and 5-V tolerant inputs.

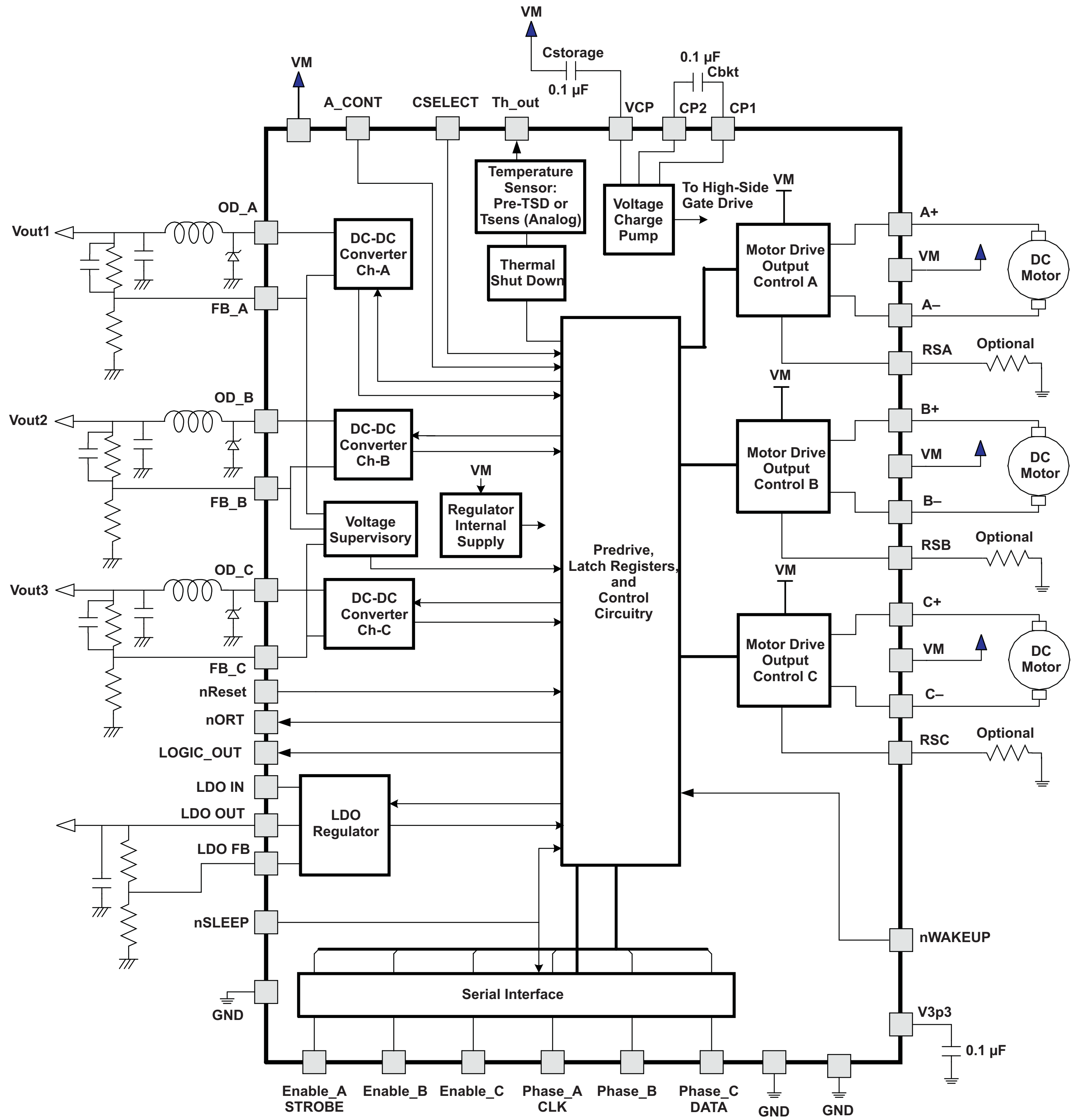
The Combo Motor Driver has three, DC-DC switch mode buck converters to generate a programmable output voltage.

The device is configured using the CSELECT terminal at start up, and serial interface during run time.

An internal shutdown function is provided for over current protection, short circuit protection, under voltage lockout and thermal shutdown.

The device also has the reset function at power on, and the input on nReset pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Setup Mode, Extended Setup Mode, Power-Down Mode

The motor output mode is configured through the SIP (DATA, CLK and STROBE) when nSLEEP = L. After set up, the nSLEEP pin must be pulled high for normal motor drive control. The value on the DATA line at the positive edge of STROBE when nSLEEP is low, selects whether the data is written to the Setup or Extended Setup registers. Setup is selected for DATA = L; Extended Setup is selected for DATA = H.

The condition, which the device requires for set up (initialize), is after the nORT (Reset) output goes H level from L level (power on, recovery from V_M < 7 V). During nSLEEP in L level, all the motor-drive functions are shut down and their outputs are high-impedance state. This device forces motor-driver functions to shut down for the power-down mode, and is not damaged even if nSLEEP is asserted during motor driving.

Data is shifted at all times, regardless of nSLEEP. Care must be taken to ensure valid data has been shifted into the internal shift register, before the STROBE rising edge, occurs while nSLEEP is LO.

7.3.1.1 Operation Setup Register Bit Assignment

Table 1. Setup Registers (1) (2) (3)

BANK	BIT	FUNCTION	DEFAULT	COMMENT
0	0	Tblank A 0	0	00: 3.75 µs, 01: 2.50 µs 10: 5.00 µs, 11: 6.25 µs
	1	Tblank A 1	0	
	2	Tblank B 0	0	00: 3.75 µs, 01: 2.50 µs 10: 5.00 µs, 11: 6.25 µs
	3	Tblank B 1	0	
	4	Tblank C 0	0	00: 3.75 µs, 01: 2.50 µs 10: 5.00 µs, 11: 6.25 µs
	5	Tblank C 1	0	
	6	DC-DC A Minoff Time	0	0: 2.2 µs, 1: 6.6 µs
	7	DC-DC A SW	1	0: On 1: Off
	8	DC-DC B SW	CSELECT	
	9	DC-DC C SW	CSELECT	
	10	MOTOR CHOPPING 0	0	00: 100 kHz, 01: 50 kHz 10: 133 kHz, 11: 200 kHz
	11	MOTOR CHOPPING 1	0	
	12	RESET DELAY CONTROL	0	0: Disable, 1: Enable
	13	LDO ENABLE	Note 1	0: On, 1: Off
	14	DC-DC B Minoff Time	0	0: 2.2 µs, 1: 6.6 µs
	15	Bank Change	0	0: Bank0, 1: Bank1

(1) The LDO default follows the DC/DC B default value based on CSELECT.
(2) All bits go to default for VM < Vth_{VM}, nReset = L.
(3) RESET DELAY CONTROL set to 1 delays nORT assertion by 100 us typical. Range is 85 us to 125 us.

Feature Description (continued)

Table 1. Setup Registers (1) (2) (3) (continued)

BANK	BIT	FUNCTION	DEFAULT	COMMENT
1	0	MISD BLANK AB 0	0	00: 2.25 µs, 01: 1.50 µs 10: 3.00 µs, 11: 3.75 µs
	1	MISD BLANK AB 1	0	
	2	MISD BLANK C 0	0	00: 2.25 µs, 01: 1.50 µs 10: 3.00 µs, 11: 3.75 µs
	3	MISD BLANK C 1	0	
	4	VRS A	0	0: Disable, 1: Enable
	5	VRS A Level 0	0	VRSA = 0: 00: 1.4 A, 01: 1.7 A 10: 1.9 A, 11: 2.2 A VRSA = 1: 00: 185 mV, 01: 210 mV 10: 260 mV, 11: 310 mV
	6	VRS A Level 1	0	
	7	DC-DC C Minoff Time	0	0: 2.2 µs, 1: 6.6 µs
	8	VRS B	0	0: Disable, 1: Enable
	9	VRS B Level 0	0	VRSB = 0: 00: 1.4 A, 01: 1.7 A 10: 1.9 A, 11: 2.2 A VRSB = 1: 00: 185 mV, 01: 210 mV 10: 260 mV, 11: 310 mV
	10	VRS B Level 1	0	
	11	DEEP SLEEP	0	0: Disable, 1: Enable
	12	VRS C	0	0: Disable, 1: Enable
	13	VRS C Level 0	0	VRSC = 0: 00: 1.4 A, 01: 1.7 A 10: 1.9 A, 11: 2.2 A VRSC = 1: 00: 185 mV, 01: 210 mV 10: 260 mV, 11: 310 mV
	14	VRS C Level 1	0	
	15	Bank Change	0	0: Bank0, 1: Bank1

7.3.1.2 Operation Extended Setup Register Bit Assignment

Table 2. Extended Setup Register (1) (2)

BANK	BIT	FUNCTION	DEFAULT	COMMENT
NA	0	Signal Select 0	0	See Logic_Out Table
	1	Signal Select 1	0	
	2	Signal Select 2	0	
	3	Signal Select 3	0	
	4	DCDC/LDO ISD Mask	0	0: Disable, 1: Enable
	5	DCDC/LDO VSD Mask	0	0: Disable, 1: Enable
	6	Motor ISD Mask	0	0: Disable, 1: Enable
	7	TSD Mask	0	0: Disable, 1: Enable
	8	Reset Mask C	0	0: Disable, 1: Enable
	9	Reset Mask B	0	0: Disable, 1: Enable
	10	Reset Mask A	0	0: Disable, 1: Enable
	11	Reset Mask SR	0	0: Disable, 1: Enable
	12	Pre TSD	0	0: TSD-20C, 1: Analog output
	13	TSD Cont0	0	See TSD Control Table
	14	TSD Cont1	0	
	15	MISD Cont	0	See MISD Control Table

(1) All bits go to default for $V_M < Vth_{VM–}$, nReset = L.
(2) Bits [11:8] are selective shutdown bits. Setting to a 1 makes faults on the associated regulator only shutdown that regulator and allows restart on an nSLEEP L > H transition. Setting to 0 shuts everything down and restarts only for $V_M < Vth_{VM–}$ or nReset = L.

Table 3. TSD Control – Operation After Detected TSD

TSD CONT1	TSD CONT0	DC-DC	MOTORS	NORT	LDO	RELEASED BY
0	0	OFF	OFF	LOW	OFF	$V_M < Vth_{VM–}$ or nReset = L
0	1	ON	OFF	HIGH	ON	$V_M < Vth_{VM–}$ or nReset = L or nSLEEP L > H transition
1	0	ON	OFF	PULSE	ON	$V_M < Vth_{VM–}$ or nReset = L or nSLEEP L > H transition
1	1	OFF	OFF	LOW	OFF	$V_M < Vth_{VM–}$ or nReset = L

Table 4. MISD Control – Operation After Detected Motor OCP

MISD CONT	DC-DC	MOTORS	NORT	LDO	RELEASED BY
0	ON	OFF	PULSE (1)	ON	$V_M < Vth_{VM–}$ or nReset = L or nSLEEP L > H transition
1	OFF	OFF	LOW	OFF	$V_M < Vth_{VM–}$ or nReset = L

(1) PULSE in Control Tables is 40-ms duration.

Table 5. Logic_Out

SIGNAL SELECT	FUNCTION (LOGIC_OUT OUTPUT)
0000	Detect OCP/UVP/OVP on A, output L
0001	Detect OCP/UVP/OVP on B, output L
0010	Detect OCP/UVP/OVP on C, output L
0011	Detect OCP on DC-DC/LDO regulator, output L
0100	Detect UVP, output L
0101	Detect OVP, output L
0110	Detect OCP on motor, output L
0111	Detect TSD, output L
1000	Revision code bit 0
1001	Revision code bit 1
1010	Revision code bit 2
1011	Device code bit 0
1100	Device code bit 1
1101	N/A
1110	Detect OCP/UVP/OVP on LDO regulator, output L
1111	Fix, output H

7.3.1.3 Deep Sleep Mode

Deep sleep mode can be entered by setting the deep sleep bit (bit 11) on the Setup register to HI. Once deep sleep mode is entered, every single subsystem is disabled, except the block necessary to regain power by making the nWAKEUP input pin LO.

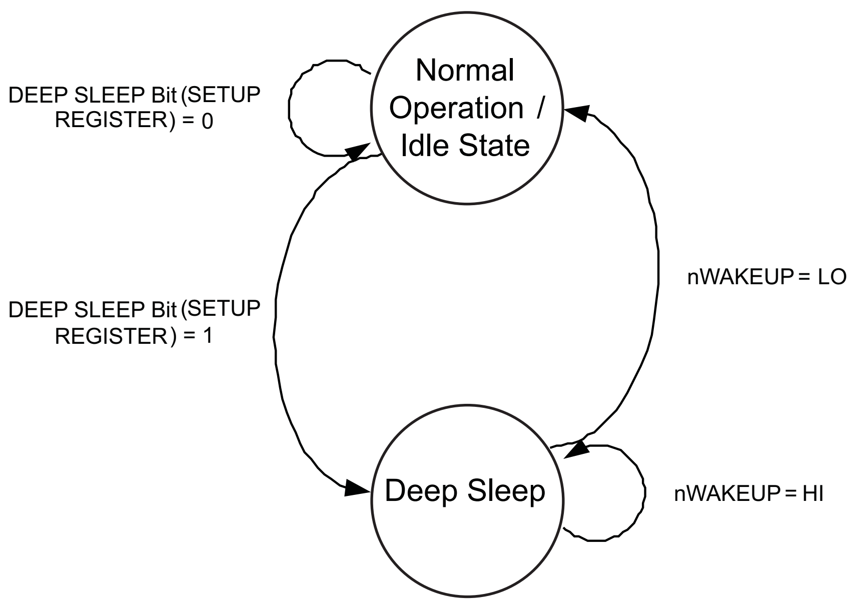


Figure 5. Deep Sleep Mode

7.3.1.4 DC Motor Drive

H-bridges A, B, and C can be controlled by using the ENABLE_X and PHASE_X control lines.

The H-bridge driver operation is available for V_M > 15 V.

Internal current sense functionality is present by default. External sensing can be enabled through the serial interface. If enabled, the sense resistor must be placed externally.

NOTE

A capacitor, not larger than 2200 pF, can be placed between each H-bridge output to GND for EMI suppression purposes. It will increase the peak current but will have no impact on the operation.

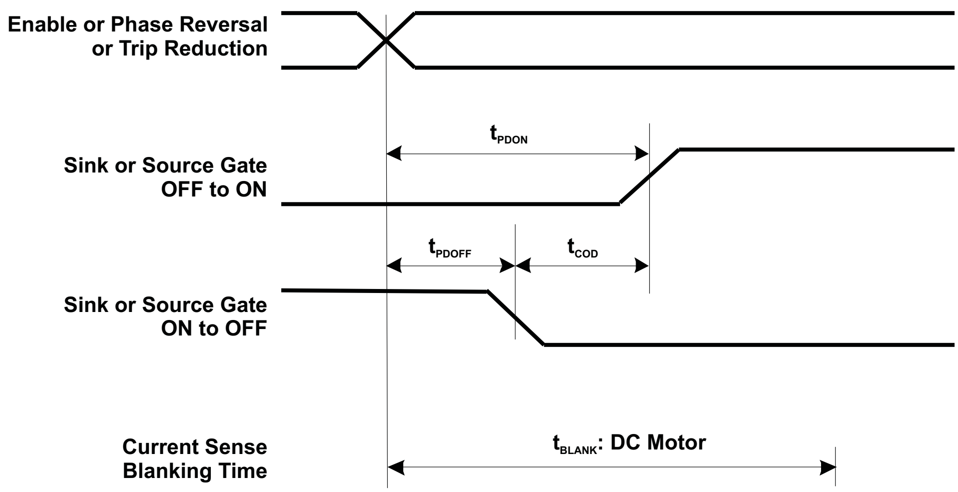


Figure 6. Crossover and Blanking Timing for H-Bridge

The dc motor H-bridges include a t_{BLANK} period to ignore huge current spike due to rush current to varistor capacitance.

7.3.1.5 Short/Open for Motor Outputs

When a short/open situation happens, the protection circuit prevents device damage under certain conditions (short at start-up, etc).

Shutdown is released based on MISD Control in the Extended Setup register.

Table 6. DC Motor-Drive Truth Table (1)

FAULT CONDITION	NSLEEP	ENABLEX	PHASEX	+ HIGH SIDE	+ LOW SIDE	– HIGH SIDE	– LOW SIDE
0	0	X	X	OFF	OFF	OFF	OFF
0	1	0	X	OFF	OFF	OFF	OFF
0	1	1	0	OFF	ON	ON	OFF
0	1	1	1	ON	OFF	OFF	ON
Motor OCP	X	X	X	OFF	OFF	OFF	OFF
TSD	X	X	X	OFF	OFF	OFF	OFF

(1) X = Don't care

7.3.1.6 Charge Pump

The charge-pump voltage generator circuit utilizes, external storage, and bucket capacitors. It provides the necessary voltage to drive the high-side switches, for both DC-DC regulators and motor driver. The charge-pump circuit is driven at a frequency of 1.6 MHz (nom). Recommended bucket capacitance (connected from CP1 to CP2) is 10 nF, rated at 55 V (minimum), and storage capacitance is 0.1 µF, at 16 V (minimum). The charge-pump storage capacitor, Cstorage, should be connected from the CP output to V_M.

For power save in sleep mode, the charge pump is stopped when N_SLEEP = L and all three regulators are turned OFF. When the part is powered up, the charge pump is started first after the CSELECT capture and, 10 ms later from the CP startup, the first regulator is started up.

Table 7. Charge Pump (1) (2)

FAULT CONDITION	DC-DC CH-A	DC-DC CH-B	DC-DC CH-C	NSLEEP	CHARGE PUMP
X	OFF	OFF	OFF	0	OFF
X	ON	X	X	X	ON
X	X	ON	X	X	ON
X	X	X	ON	X	ON
0	X	X	X	1	ON
Motor OCP	X	X	X	1	ON
TSD	OFF	OFF	OFF	X	OFF

(1) X = Don't care
(2) DC=DC status in fault condition is determined by serial register settings, TSD Control table, and MISD Control table. These tables define status of charge pump.

7.3.1.7 DC-DC Converters

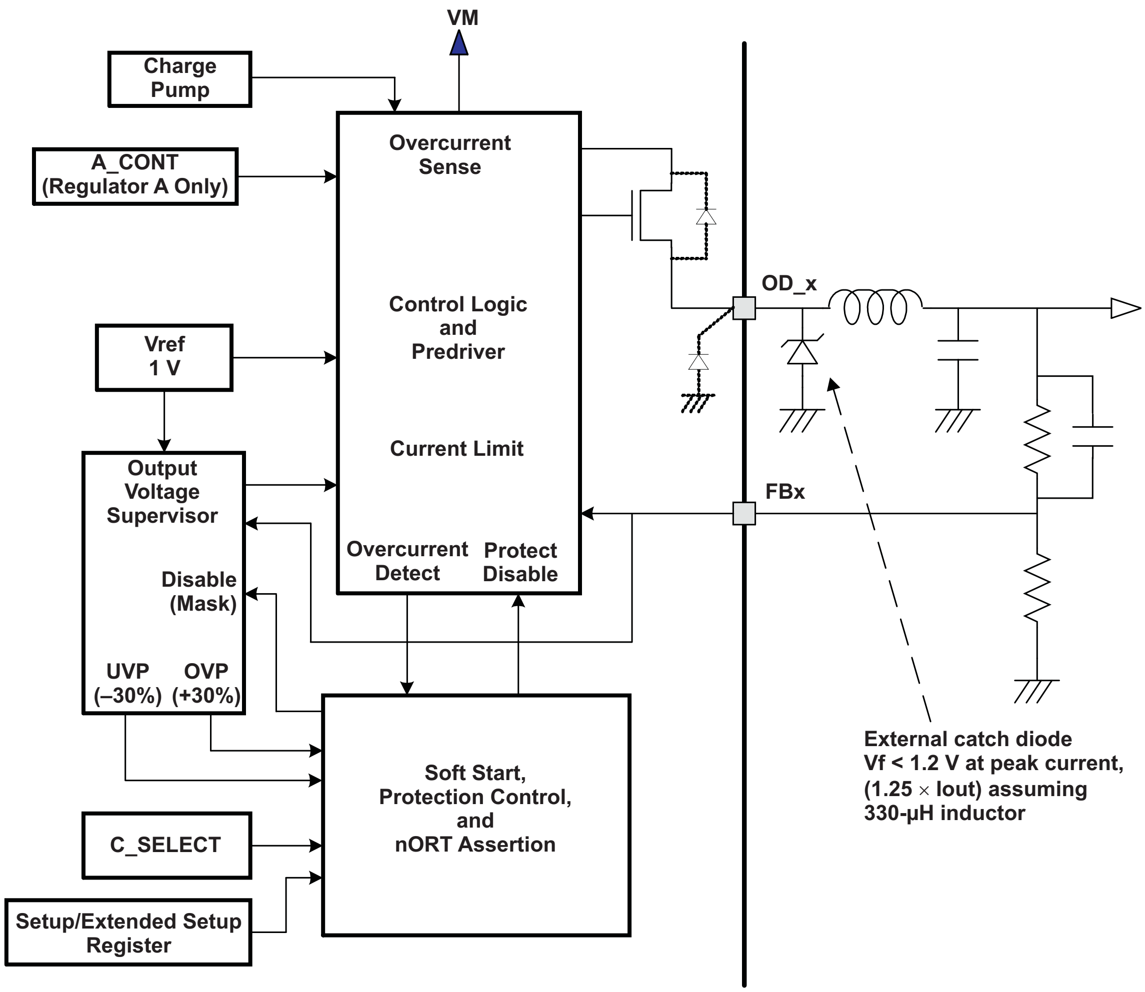


Figure 7. DC-DC Converter

This is a switch-mode regulator with integrated switches, to provide a programmed output set by the feedback terminal. The DC-DC converter has a variable duty cycle topology. External filtering (inductor and capacitor) and external catch diode are required. The output voltage is short circuit protected.

The regulator has a soft-start function to limit the rush current during start-up. It is achieved by using VFB ramp during soft start.

For unused DC-DC converter channels, the external components can be removed if the channel is set to inactive by the CSELECT pin and register bits. Recommend connecting unused FB pin to GND or V3p3 (pin 17).

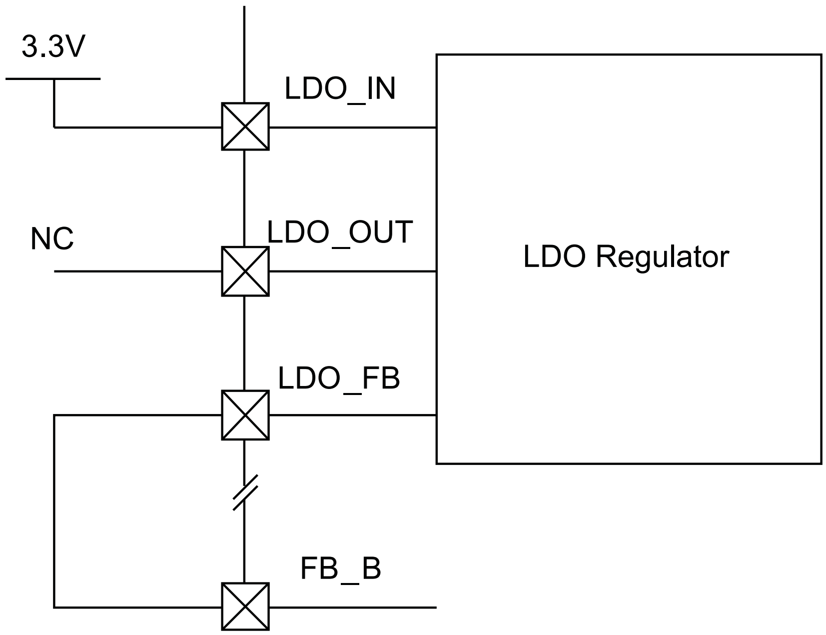


Figure 8. Unused LDO Recommended Connections

For proper termination, it is recommended that, if left unused, the LDO terminals be connected in the following fashion:

1. LDO IN must be powered by an input voltage greater than 1 V.
2. LDO OUT must be left disconnected.

LDO Feed Back must be connected to the DC/DC Converter Channel B Feed Back terminal.

Table 8. CSELECT for Start-Up (1) (2) (3)

CSELECT	PIN VOLTAGE	DCDC_A	DCDC_B	DCDC_C
Gnd	0 V to 0.3 V	OFF	OFF	OFF
Pull down (by external 200 kΩ)	1.3 V to 2.0 V	OFF	ON	OFF
OPEN	3.0 V to 3.3 V	OFF	ON	ON

(1) The CSELECT pin is connected to internal 3.3-V supply through 200-kΩ resister.
(2) This CSELECT pin control is valid after the PowerON Reset is initiated. Once the Setup Register is set, the DC-DC control follows the bits 7 to 9 on the Setup Register, bank 0, until the next PowerON Reset event occurred.
(3) For OPEN case, B starts up 1st and C follows after 10-ms delay.

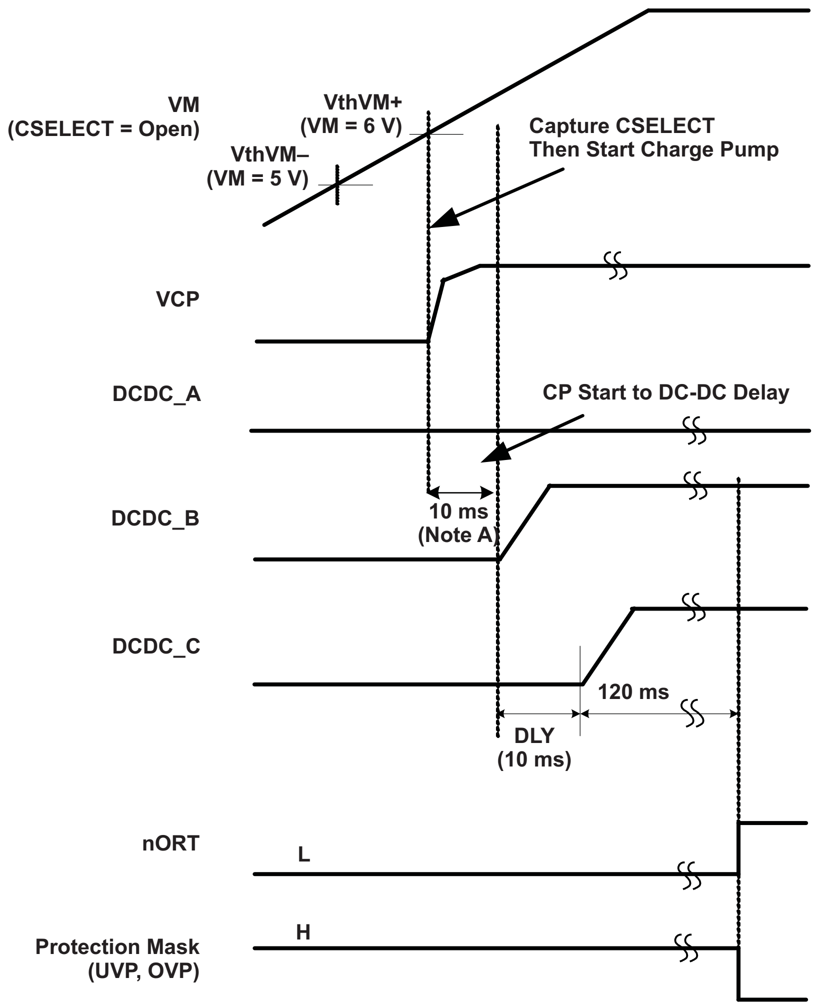
Table 9. Regulator A Control

SETUP REGISTER BANK 0, BIT 7	A_CONT	DCDC_A
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

7.3.1.8 nReset: Input for System Reset

nReset pin assertion stops all the DC-DC converters and H-bridges. It also resets all the register contents to default values. After deassertion of input, device follows the initial start-up sequence. The CSELECT state is captured after the nReset deassertion (L > H).

The input is pulled up to internal 3.3 V by a 200-kΩ resistor. When the pin is H or left open, the reset function is released. Also it has deglitch filter of 2.5 µs to 7.5 µs.



A. Charge-pump wakeup delay, from 10 ms to 20 ms due to asynchronous event capture.

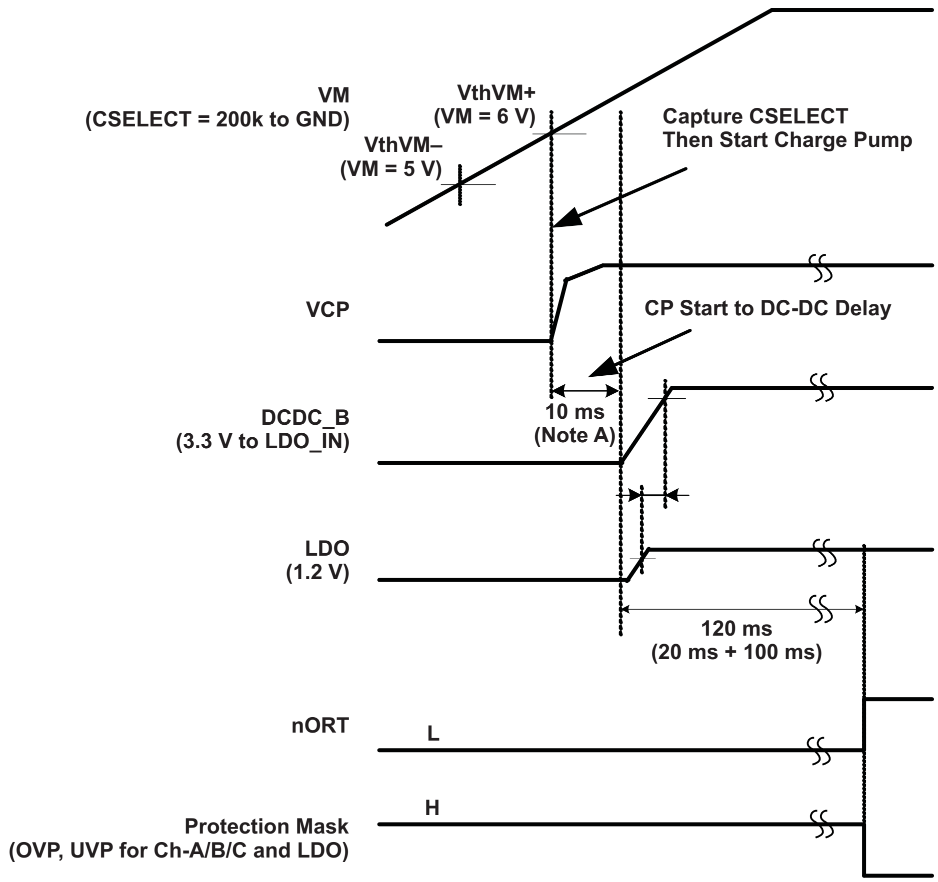
B. When V_M crosses the Vth_{VM+} (about 6.0 V), the CSELECT state is captured. In case of the CSELECT being open (pulled up to internal 3.3 V), DC-DC regulator channels B and C are turned on.

C. LDO OCP is masked during protection M\mask time.

D. In order to avoid false SPI data latching caused by a rising edge on the STB signal, nSLEEP will remain high during the power up stage (VM rising) and until nORT is released.

E. DC/DC Channel A follows the Regulator A Control table. During power up, DC/DC Channel A starts up disabled (SETUP BANK 0 [7] = 1).

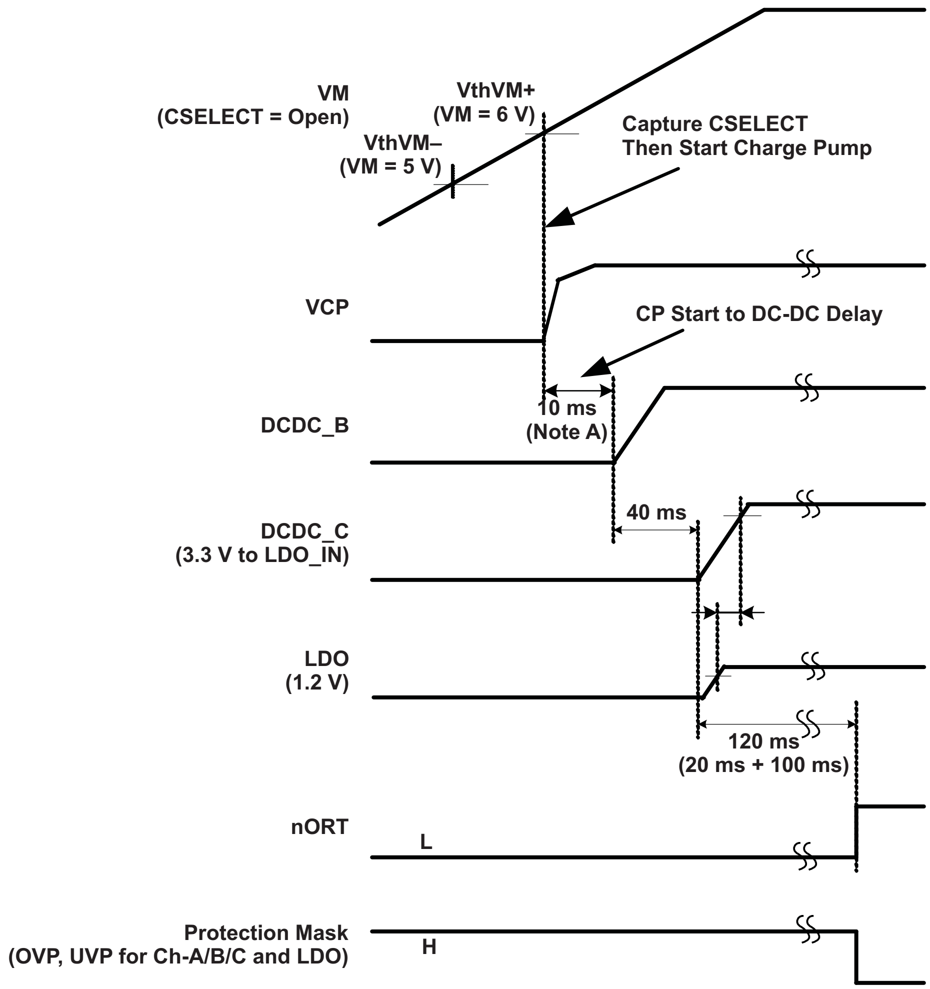
Figure 9. Power-Up Timing (Power-Up With DC-DC Turnon by CSELECT)



A. Charge-pump wakeup delay, from 10 ms to 20 ms due to asynchronous event capture.

B. LDO Enable follows DC/DC B Enable during power up and can be controlled using the SETUP register after power up.

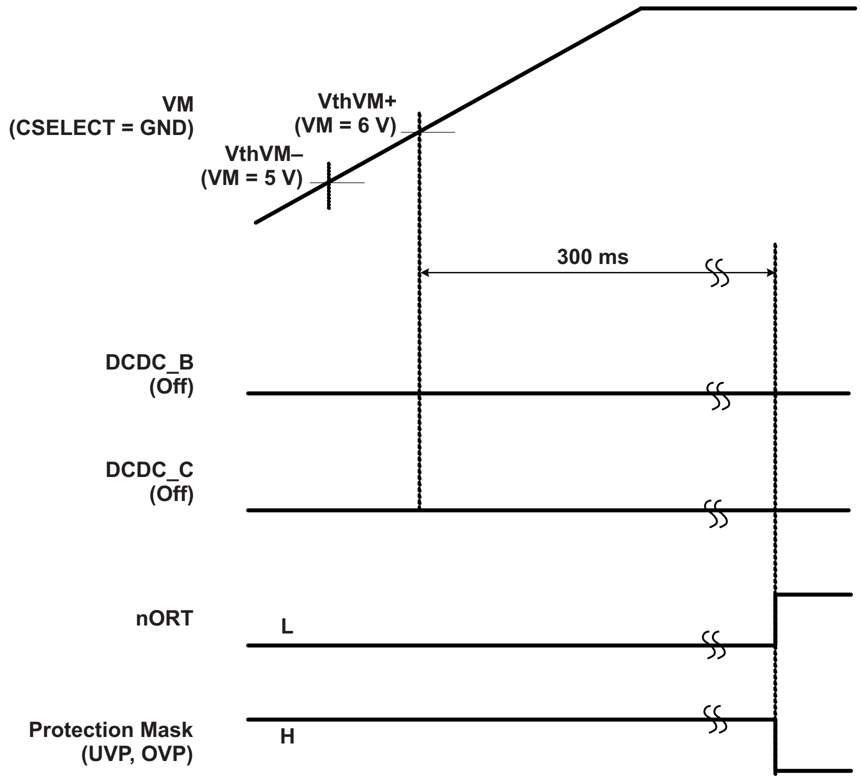
Figure 10. Power-Up Timing (Power-Up With LDO, Supplied by DCDC_B)



A. Charge-pump wakeup delay, from 10 ms to 20 ms due to asynchronous event capture.

B. LDO Enable follows DC/DC B Enable during power up and can be controlled using the SETUP register after power up. In this case, since LDO_IN is driven by DC/DC Channel C, LDO_OUT will follow DC/DC Channel C.

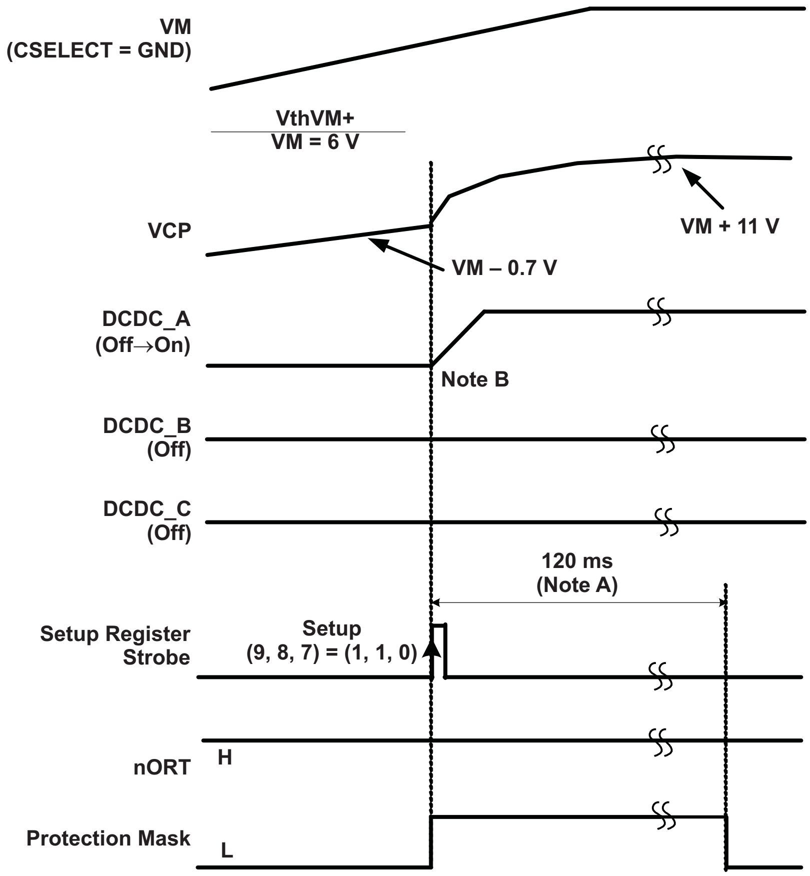
Figure 11. Power-Up Timing (Power-Up With LDO, Supplied by DCDC_C)



A. When V_M crosses the Vth_{VM+} (about 6 V) with CSELECT = GND, none of three regulators are turned ON. The nORT output is released to H after 300 ms from Vth_{VM+} crossing.

B. LDO OCP is masked during protection mask time.

Figure 12. Power-Up Timing (Power-Up Without DC-DC Turnon, CSELECT = GND)

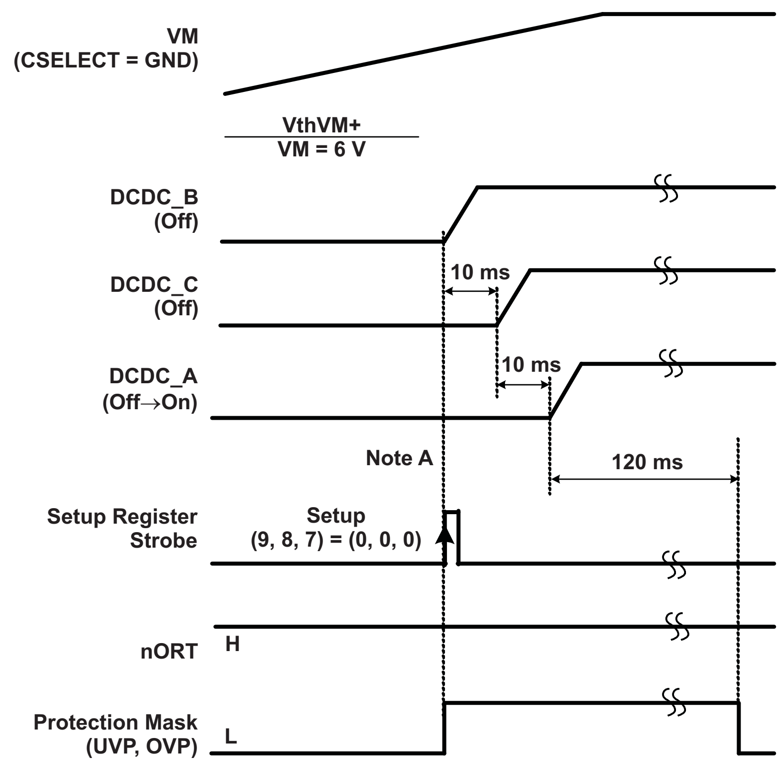


A. The regulator is started from the strobe input, same as the charge pump. No 10-ms waiting, because the VCP pin already reached to V_M – 0.7 V.

B. LDO OCP is masked during protection mask time.

C. A_CONT must be LOW or OPEN for regulator A to turn on.

Figure 13. Power-Up Timing (DC-DC Regulator Wakeup by Setup Register)



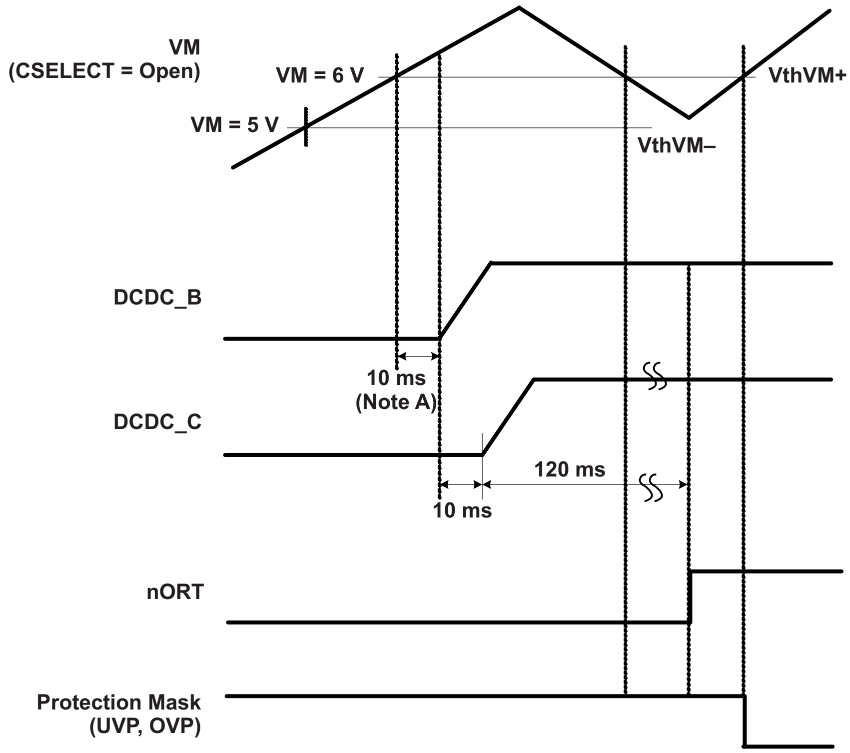
A. A_CONT must be LOW or OPEN for regulator A to turn on.

B. LDO OCP is masked during protection mask time.

Figure 14. Power-Up Timing (DC-DC Regulator Wakeup by Setup Register, All Three Channels ON)

7.3.1.9 V_M Start-up/Power-Down and Glitch Condition

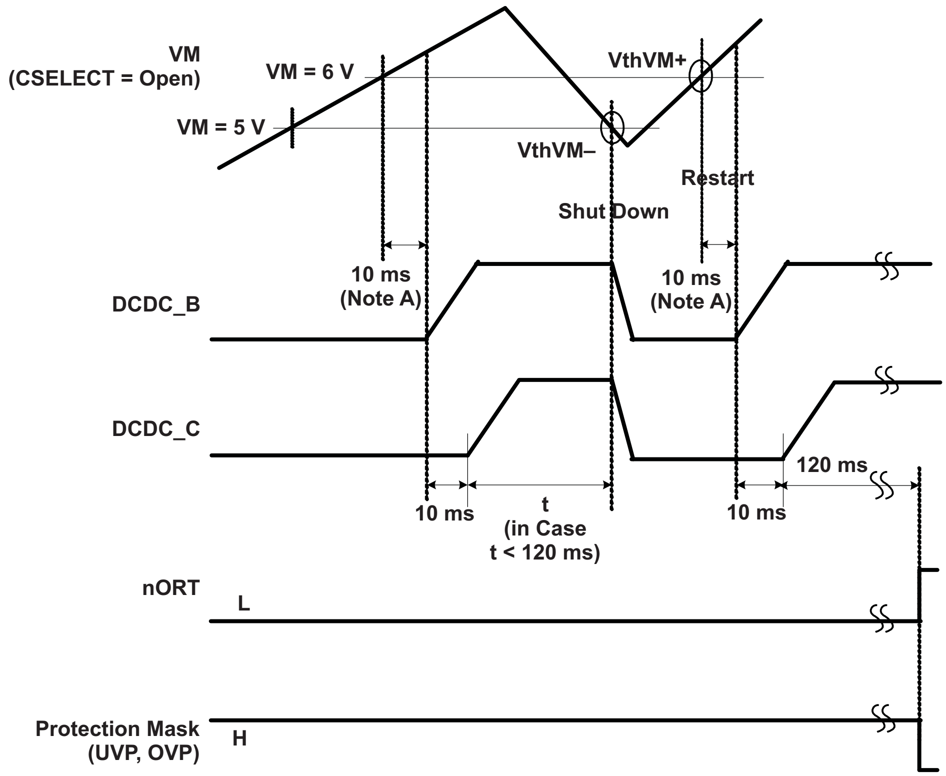
1. Start up with V_M glitch (not below Vth_{VM-})



A. LDO OCP is masked during protection mask time.

Figure 15. Power-Up Timing With VM Glitch Condition (Not Below Vth_VM-)

2. Start up with V_M glitch (below Vth_{VM-})



A. LDO OCP is masked during protection mask time.

Figure 16. Power-Up Timing With VM Glitch Condition (Below Vth_VM-)

3. Power down (normal)

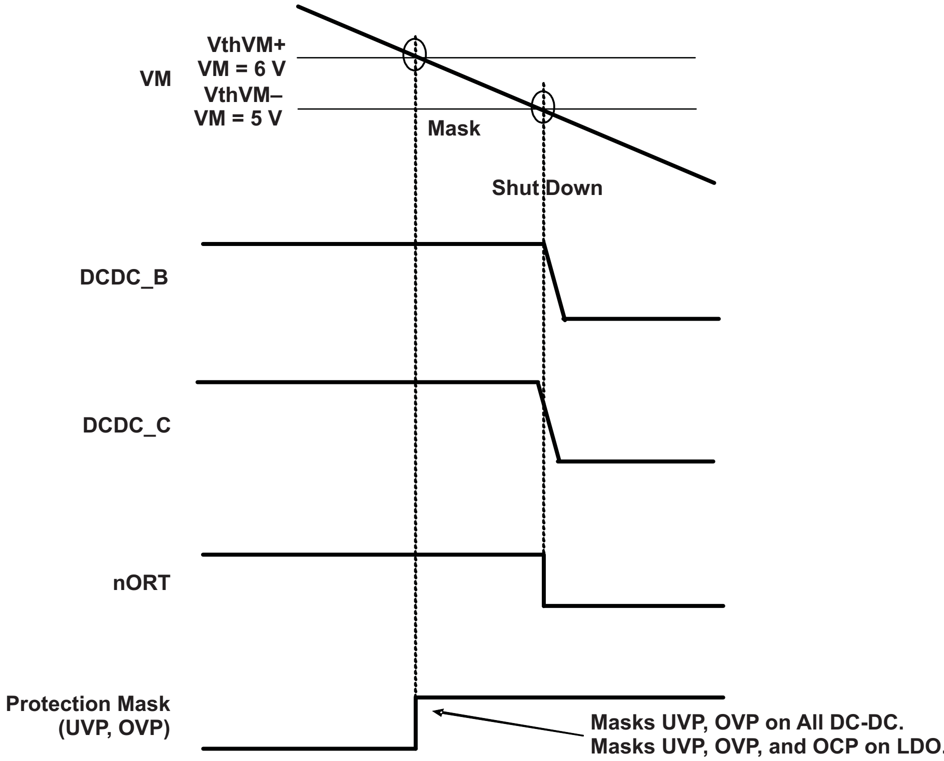


Figure 17. Power-Down Timing

4. Power down (glitch on V_M)

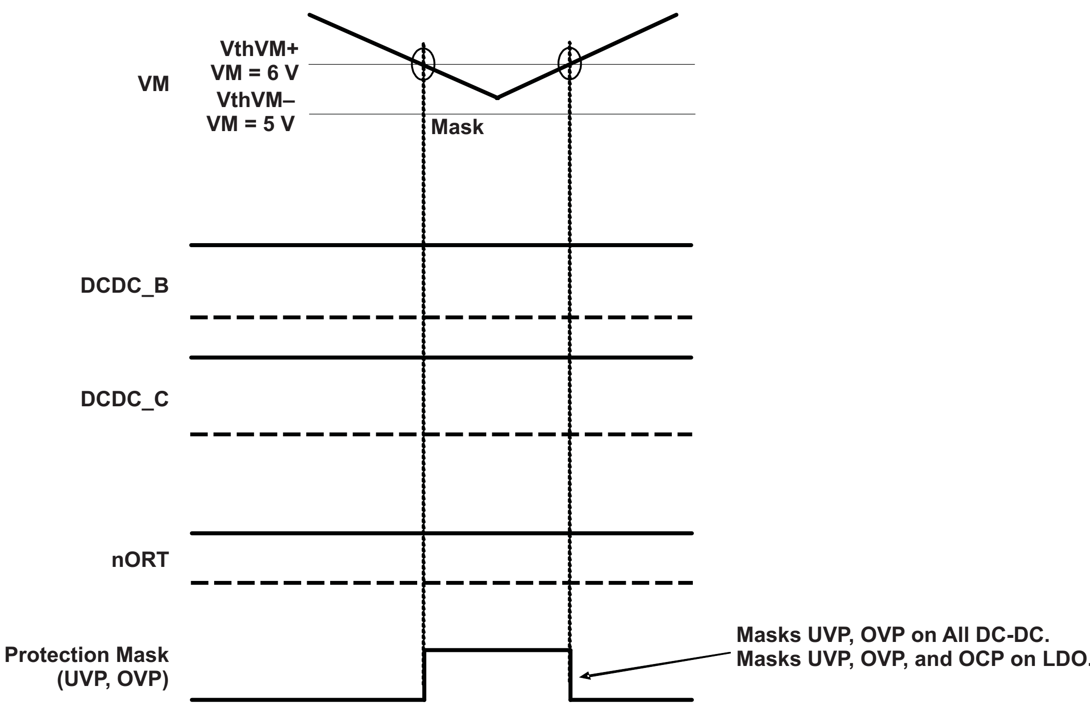
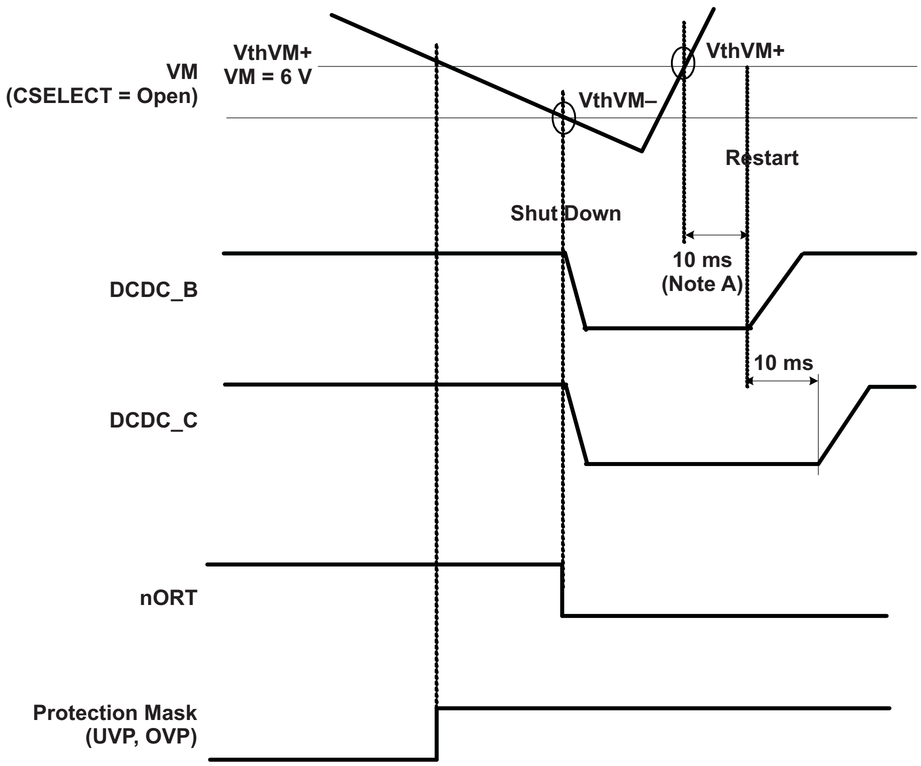


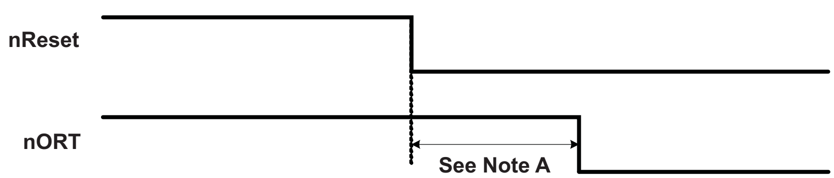
Figure 18. Power-Down Timing (With Glitch on VM)

5. Power down (glitch on V_M below Vth_{VM-})



A. LDO OCP is masked during protection mask time.

Figure 19. Power-Down Timing (With Glitch on VM Below VthVM-)



A. 2.5 µs < (nReset Deglitch + Output Delay) < 10 µs

Figure 20. Shut Down by nReset

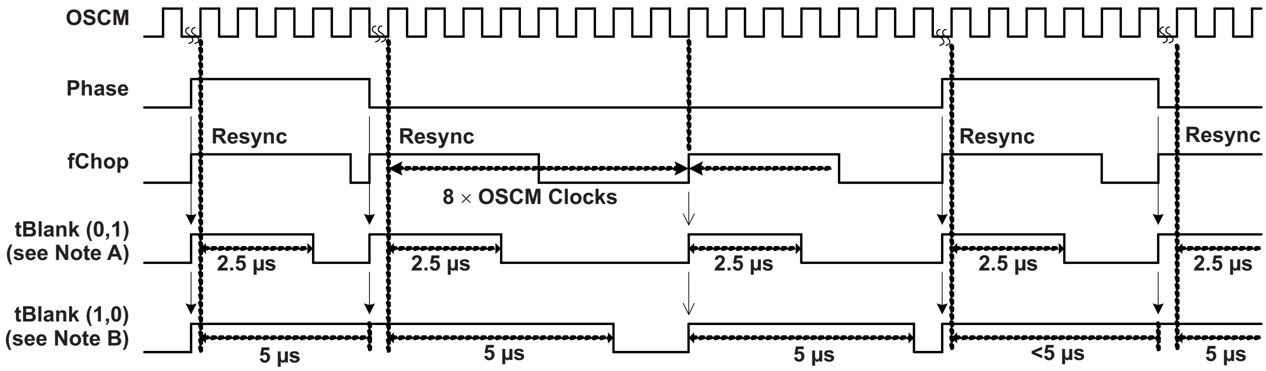
7.3.2 Blanking Time Insertion Timing for DC Motor Driving

For the dc motor-driving H-bridge, tBlank is inserted at each phase reversal and following each chopping cycle (once in every eight OSCM clocks).

For a large n number (5 or 6), tBlank setup may decrease the Itrip detect window. Care must be taken when optimizing this in the system.

Case A: Phase duty = 25%

- A*1 for setup bit = (1,0)
- A*2 for setup bit = (0,1)



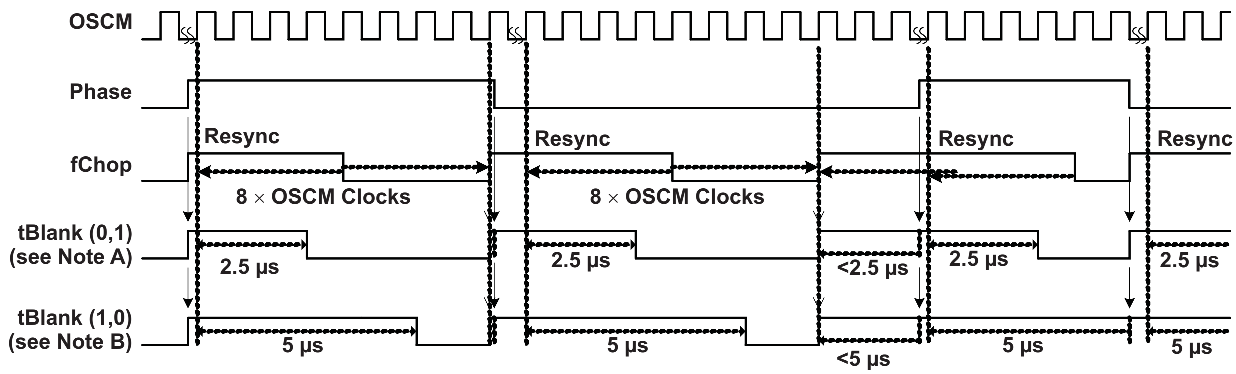
A. Setup register bit <1:0> = (1,0), tBlank = 5 µs (or bits <3:2>/<5:4> for H-bridge B/C channel)

B. Setup register bit <1:0> = (0,1), tBlank = 2.5 µs (or bits <3:2>/<5:4> for H-bridge B/C channel)

Figure 21. Timing for Case A

Case B: Phase duty = 40%

- B*1 for setup bit = (1,0)
- B*2 for setup bit = (0,1)



A. Setup register bit <1:0> = (1,0), tBlank = 5 µs (or bits <3:2>/<5:4> for H-bridge B/C channel)

B. Setup register bit <1:0> = (0,1), tBlank = 2.5 µs (or bits <3:2>/<5:4> for H-bridge B/C channel)

Figure 22. Timing for Case B

7.3.3 Function Table in nORT, Power Down, V_M Conditions

The following is valid only when the protection control bits (in Extended Setup register) are all 0.

Table 10. Block Conditions by Device Status

DEVICE STATUS	CHARGE PUMP	OSCM	nORT	MODE SETTING
nSleep	Active	Active	Inactive	Available
nORT	Inactive	Active	Active	Depend on power down
V_M < 6 V during power down	Active	Active	See timing chart	Depend on power down
4.5 V < V_M	Inactive	Inactive	Active	Unavailable

Table 11. Shutdown Functions

FAULT CONDITION	DCDC_A	DCDC_B	DCDC_C	MOTOR	nORT
DCDC_A UVP/OVP/OCP	Shut down	Shut down	Shut down	Shut down	Asserted (low)
DCDC_B UVP/OVP/OCP	Shut down	Shut down	Shut down	Shut down	Asserted (low)
DCDC_C UVP/OVP/OCP	Shut down	Shut down	Shut down	Shut down	Asserted (low)

Table 11. Shutdown Functions (continued)

FAULT CONDITION	DCDC_A	DCDC_B	DCDC_C	MOTOR	nORT
Motor OCP	See MISD Control Table	See MISD Control Table	See MISD Control Table	See MISD Control Table	See MISD Control Table
TSD	See TSD Control Table	See TSD Control Table	See TSD Control Table	See TSD Control Table	See TSD Control Table

- Table is valid when the Protection and Reset Mask bits in the Extended Setup register are all 0.
- If Reset Mask (selective shutdown) bits are set, shutdown and release description is in the note following the Extended Setup register definition.
- DC-DC regulators are released at $V_M > Vth_{VM+}$ when V_M increasing. When V_M decreasing, regulators are shut down when $V_M < Vth_{VM–}$. When $Vth_{VM+} > V_M > Vth_{VM–}$, OVP and UVP are masked.
- Motor OCP shutdown release is specified in MISD Control Table.
- TSD shutdown release is specified in TSD Control Table.

7.4 Device Functional Modes

7.4.1 Operation With 7 V < VM < 18 V

The devices starts operating with input voltages above 6.0 V typical. Between 7 V and 18 V, DC-DC converters can operate. Enabling motors in not allowed.

7.4.2 Operation With 18 V ≤ VM ≤ 38 V

The device can operate with full function. Both DC-DC converter and Motor Drivers can be enabled.

7.5 Programming

7.5.1 Serial Interface

The device has a serial interface port (SIP) circuit block to control DC motor H-bridges, DC-DC regulators, and other functions, such as blanking time, OFF time, and so forth. Because the SIP shares its three lines with three of the motor control signals, the SIP is only available when nSLEEP is low.

Table 12. Serial Interface

nSLEEP	PIN 9	PIN 10	PIN 14	SIP FUNCTIONALITY
L	STB	CLK	DATA	Yes
H	ENA	PHA	PHC	No

Sixteen-bit serial data is shifted least significant bit (LSB) first into the serial data input (DATA) shift register on the falling edge of the serial clock (CLK). After 16-bit data transfer, the strobe signal (Strobe) rising edge latches all the shifted data. During the data transferring, Strobe voltage level is ok with L level or H level.

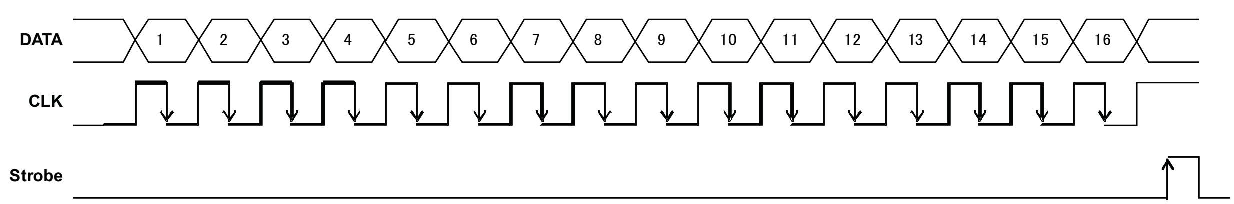
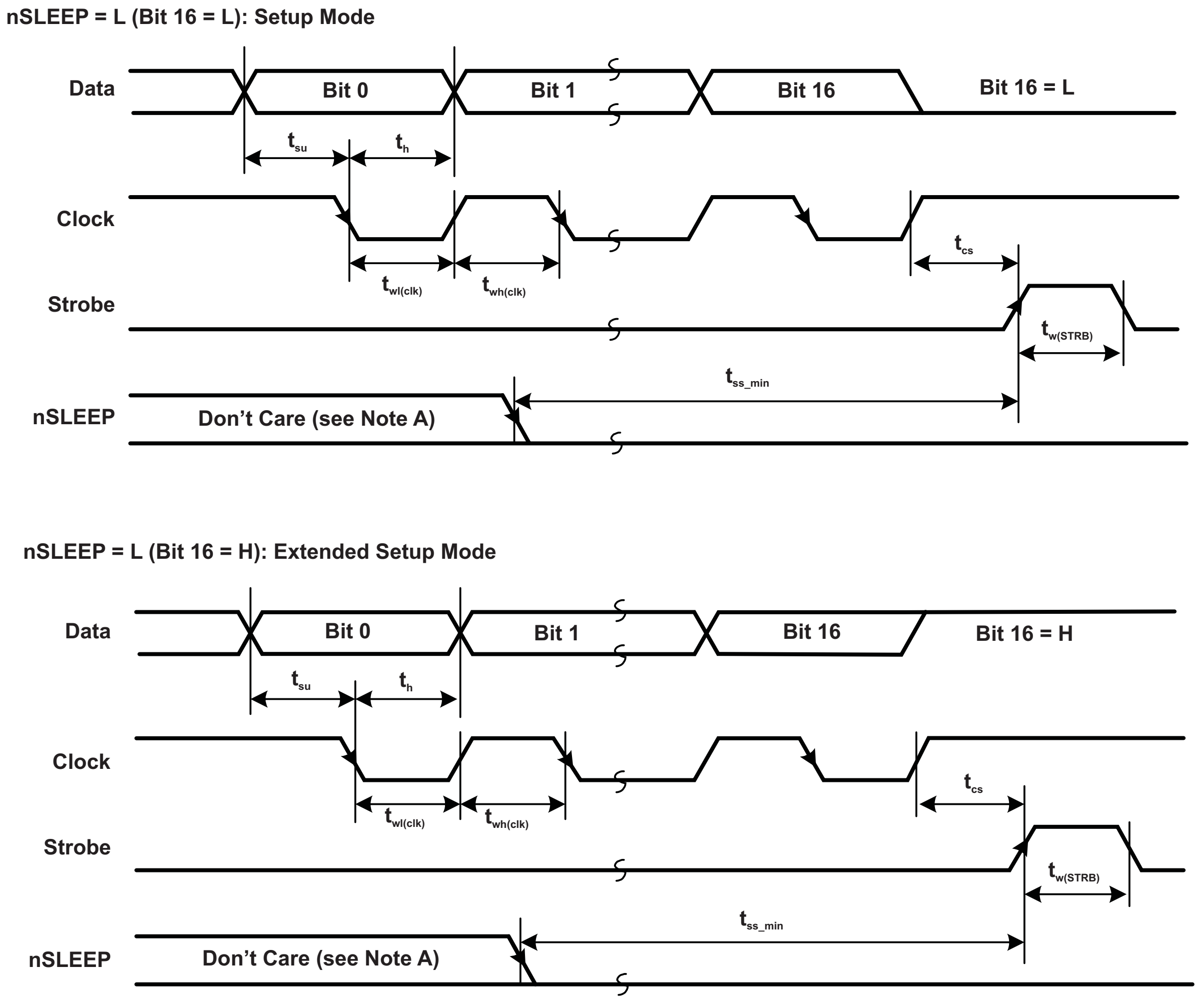


Figure 23. Serial Interface

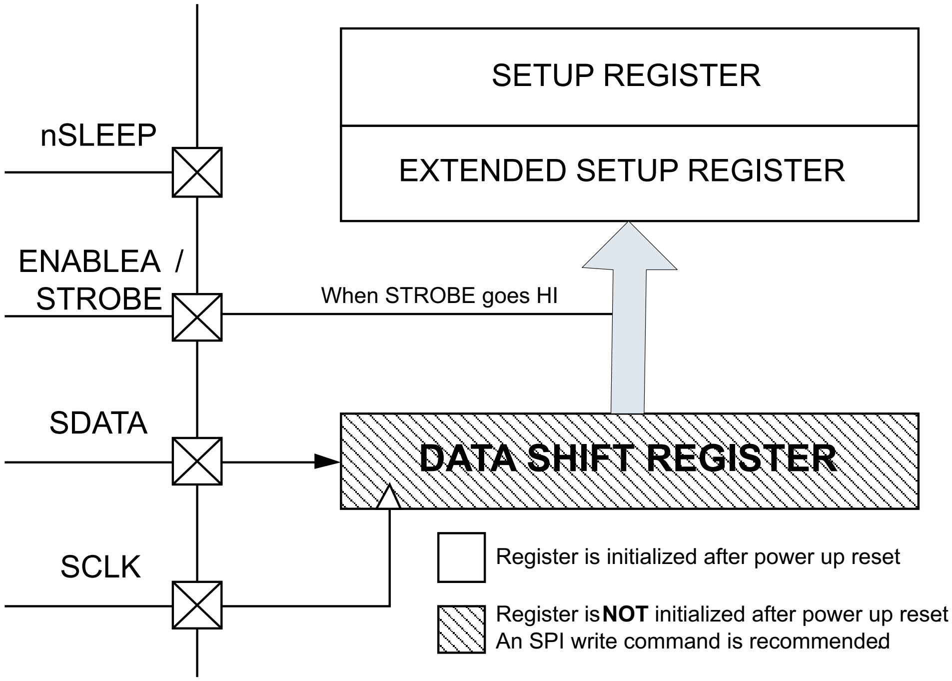
NOTE

During startup (VM rising), nSLEEP input is set HI, suppressing false data latching caused by a rising edge on the STB signal. nSLEEP will remain HI until nORT is released (120 ms after DC-DC regulators come up).



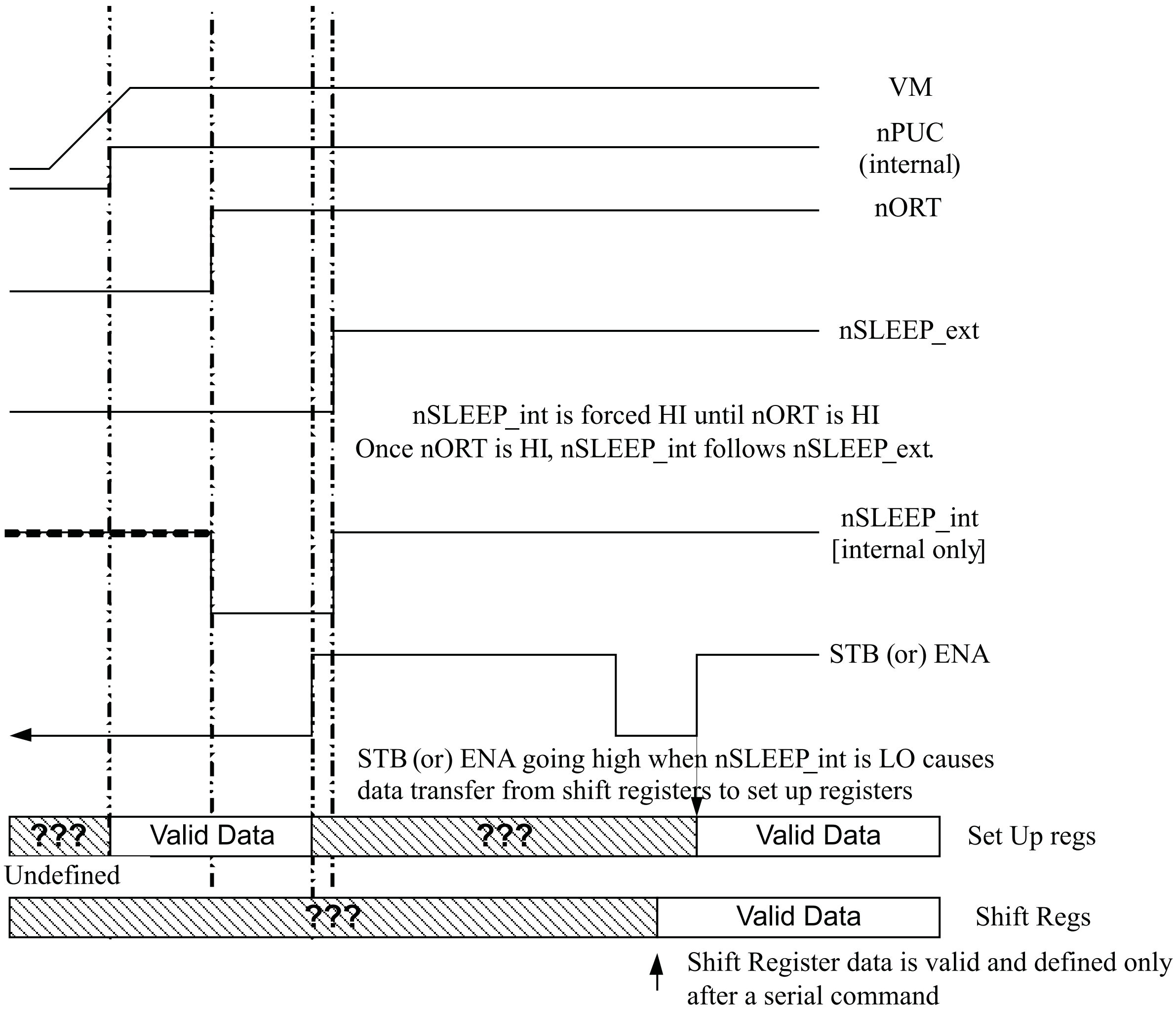
A. For initial setup, nSleep state can be "Don't care" before the tss_min timing prior to the strobe.

Figure 24. Serial Interface Timing



A. It is recommended that after initial power up sequence, a serial command be performed to clear undefined data in the internal shift register. This will help avoid latching undefined data into SETUP and EXTENDED SETUP registers. SETUP and EXTENDED SETUP registers are properly initialized during power up, but internal shift register is not initialized.

Figure 25. Serial Peripheral Interface Block Diagram



A. During startup (VM rising), internally nSLEEP de-asserted to HI, suppressing false data latching caused by a rising edge on the STB signal. nSLEEP will remain HI until nORT is released (120 ms after DC-DC regulators come up).

Figure 26. Serial Peripheral Interface STROBE Blocking During Power Up

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8808 provides an integrated motor driver solution. The chip has three H-bridges internally and is configurable to different settings by SPI communication.

8.2 Typical Application

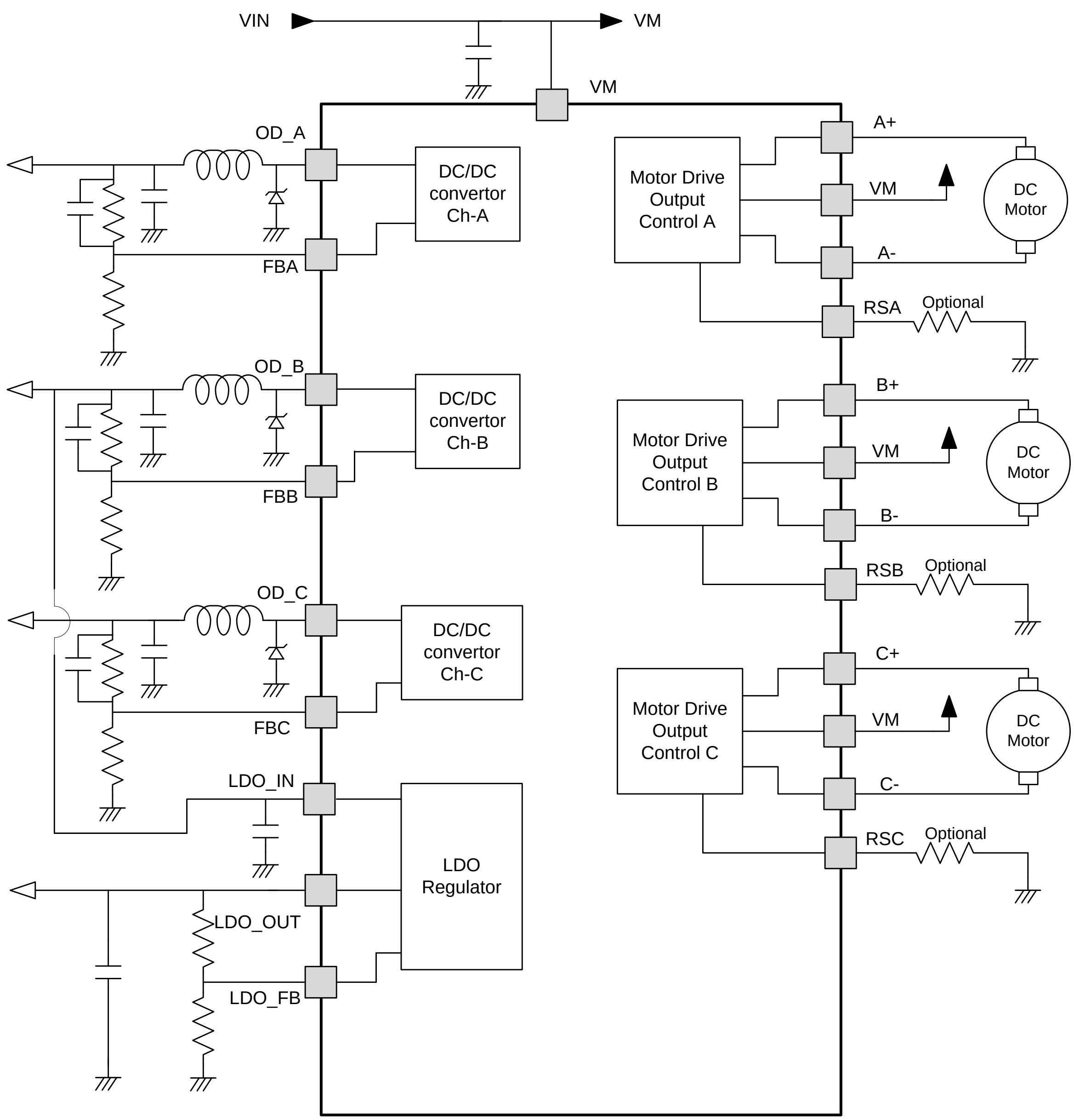


Figure 27. 3 DC Motors, 3 Switching Regulators and 1 LDO Usage Case

Typical Application (continued)

8.2.1 Design Requirements

To begin the design process, determine the following:

- Output voltage for each DC-DC converter and LDO.
- Output voltage start up sequence.
- Other parameters through SPI.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage for Each DC-DC Converter

Output voltage is set by external feedback resister network. For example,

1.5-V Output : 1.0 KΩ and 2.0 KΩ
1.0-V Output : 0 Ω and 3.0 KΩ
3.3-V Output : 6.8 KΩ and 1.5 KΩ

8.2.2.2 Output Voltage Start Up Sequence

DC-DC converters start up sequence is determined by CSELECT pin. See *DC-DC Converters* for details.

8.2.2.3 Other Parameters

Other parameters are programmed through SPI.

8.2.2.4 Motor Configuration

Many parameters are set by SPI register setting. Ramp up device with nSLEEP = Low, then write setup registers through SPI.

8.2.3 Application Curves

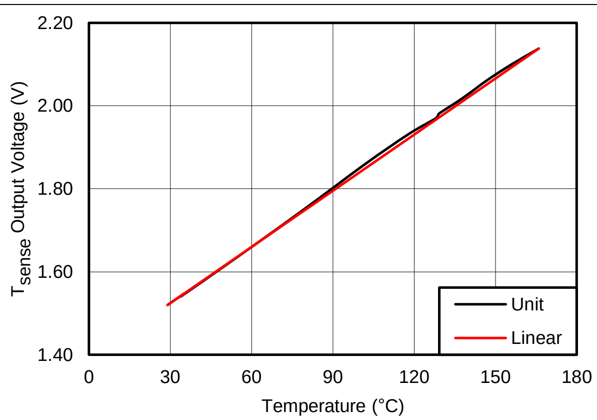


Figure 28. Tsense (Analog Out) Temperate Coefficient: Voltage Plot Example (Typical)

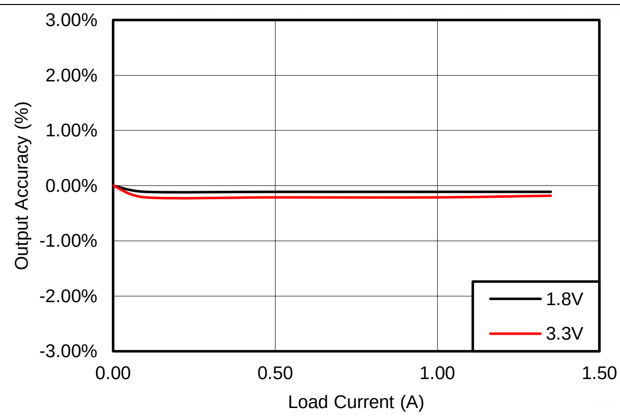


Figure 29. DC-DC Converter - DC Load Regulation Example (Typical)

9 Power Supply Recommendations

This device requires a single voltage supply only. Supply to VM and LDOIN pins can be supplied by one of the switching regulator outputs.

10 Layout

10.1 Layout Guidelines

- Recommended to have GND plane layer for better thermal performance. Thermal pad directly going down to GND layer just under the device is the best way.
- Distance between Odx to Inductance should be as close as possible. This line has switching from 0 V to VM.
- FBx pin and external feedback resistor should be as close as possible. This is the analog sensing pin for the DC-DC converter.
- V3p3 pin is for internal analog reference voltage, and should be quiet. External 0.1 µF should be located closer.

10.2 Layout Example

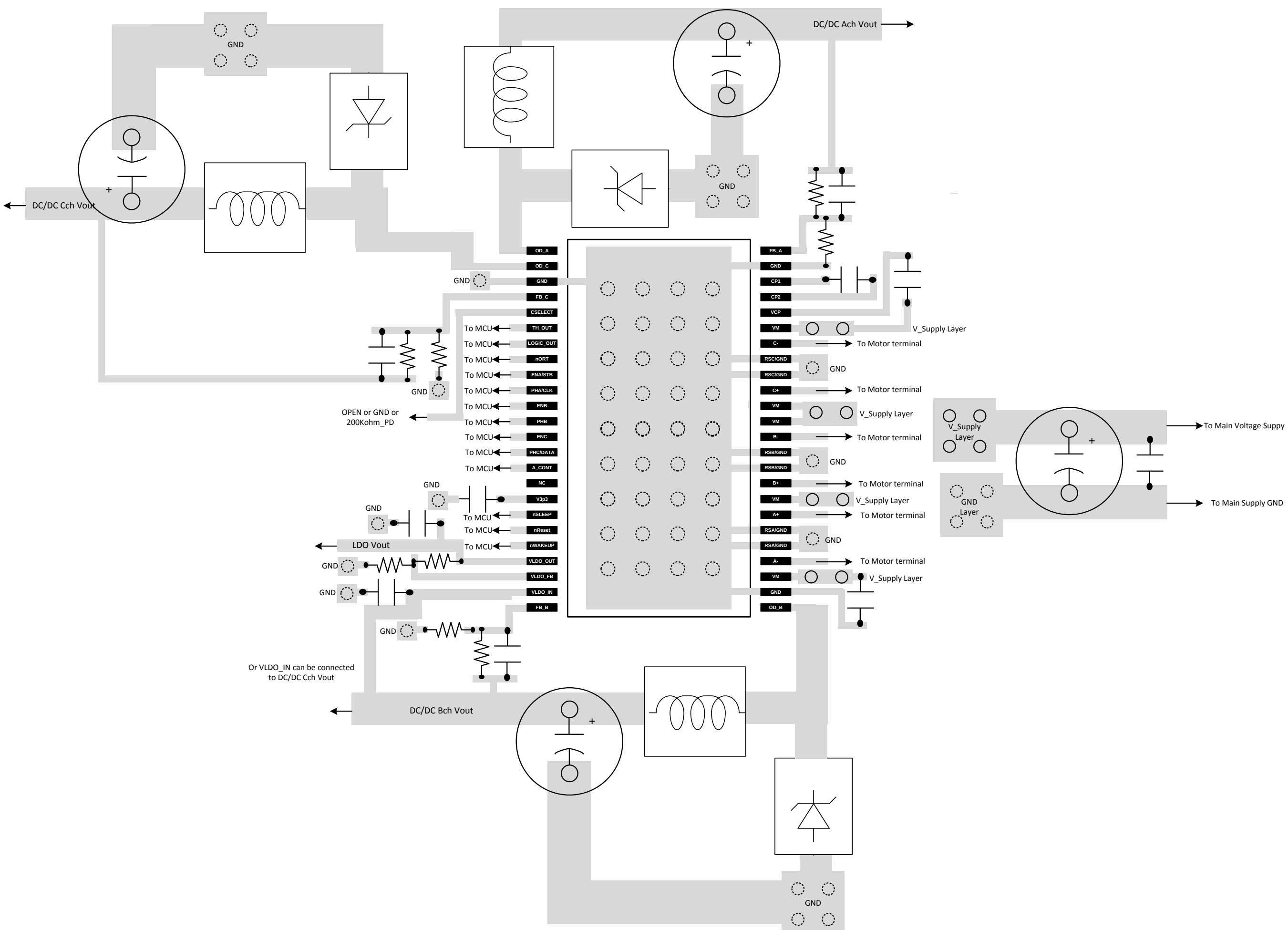


Figure 30. Layout Schematic

11 Device and Documentation Support

11.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8808DCAR	ACTIVE	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	8808	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

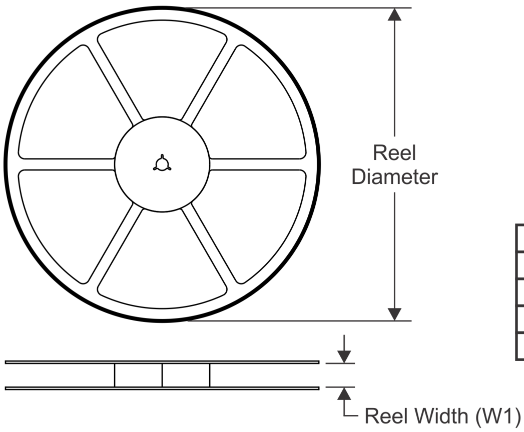
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

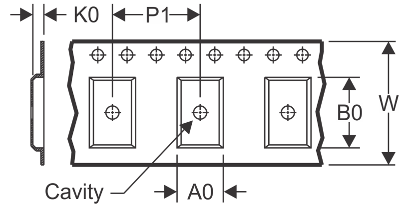
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

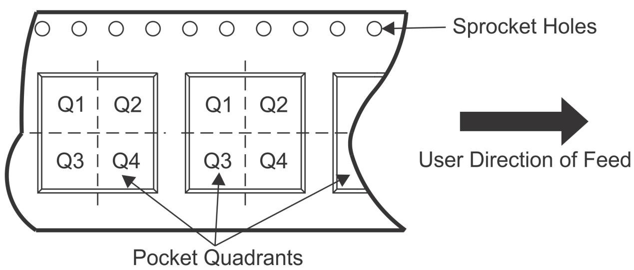


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

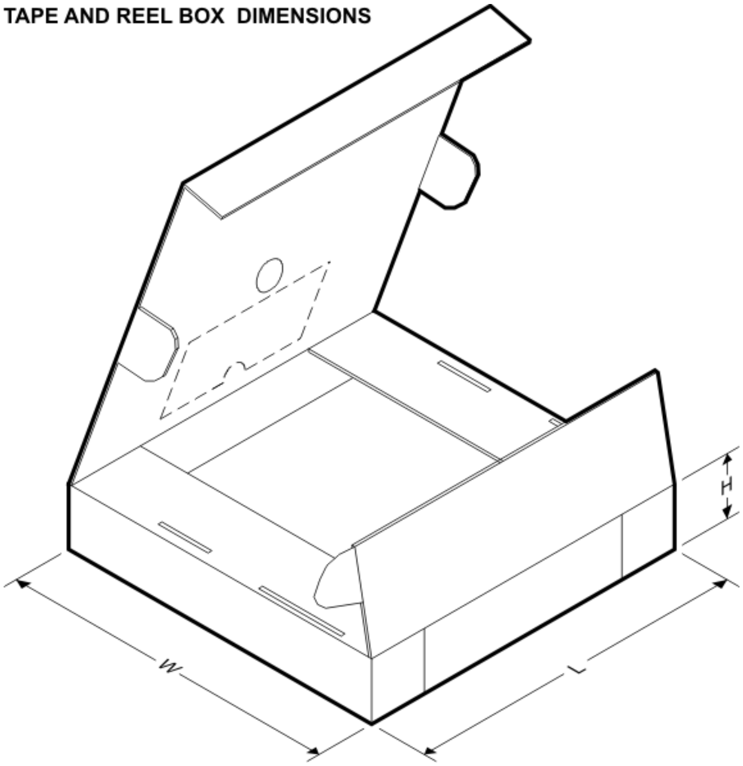
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8808DCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

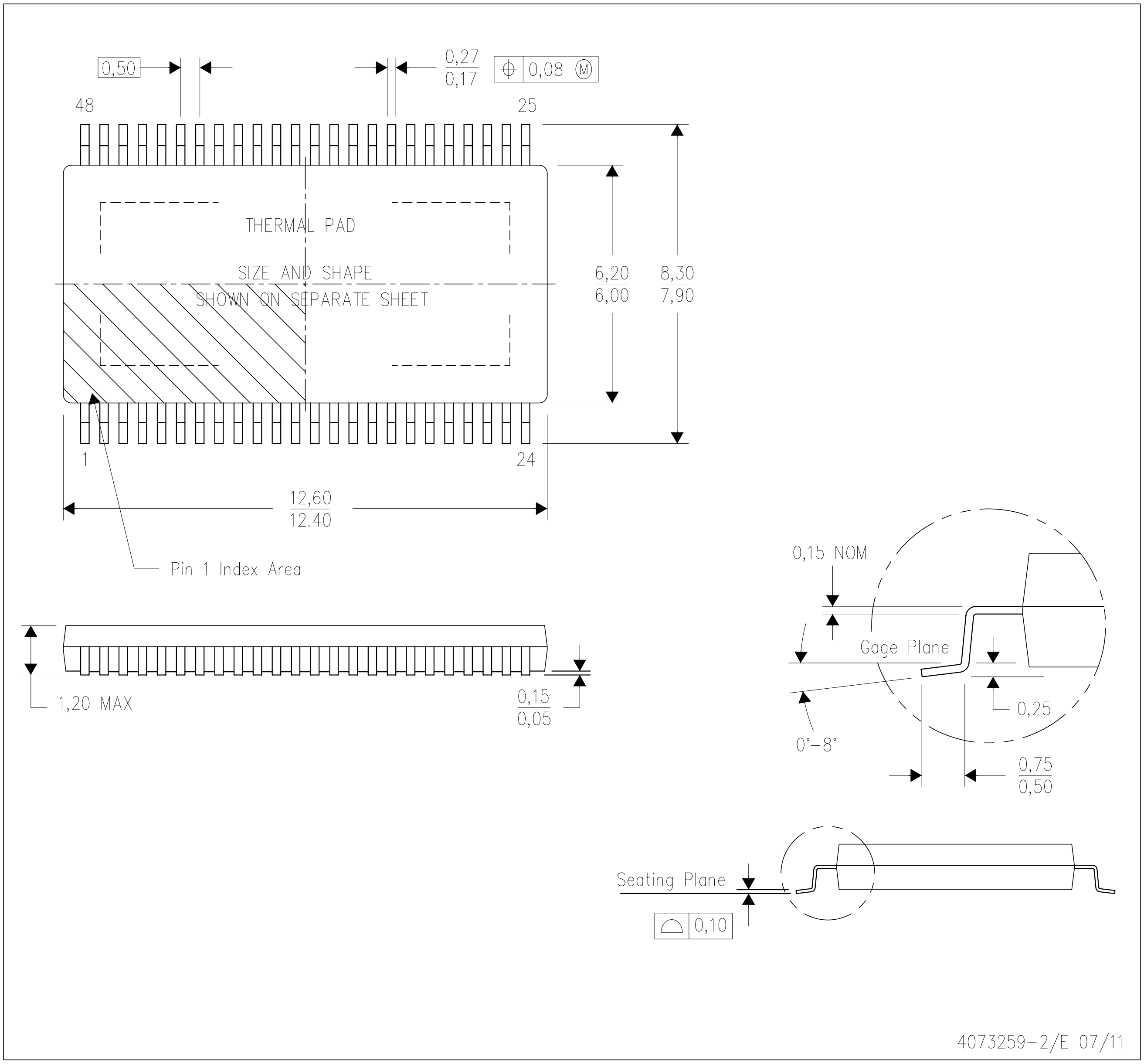
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8808DCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

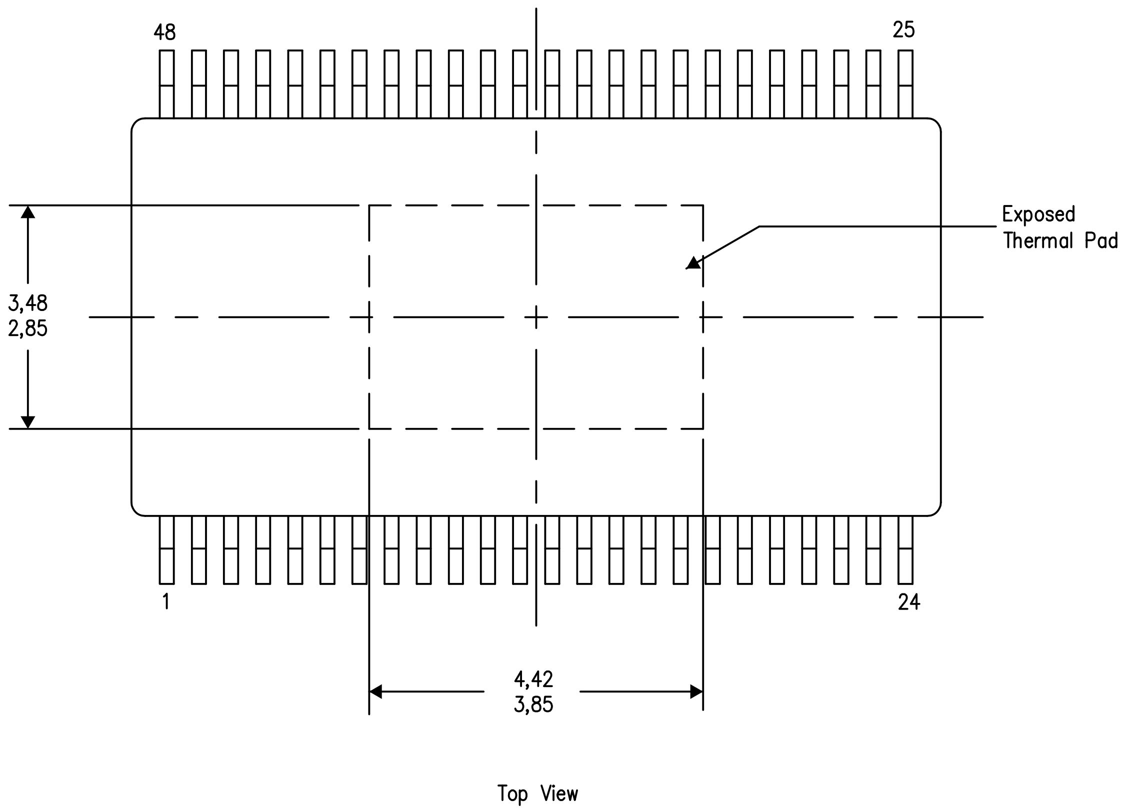
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

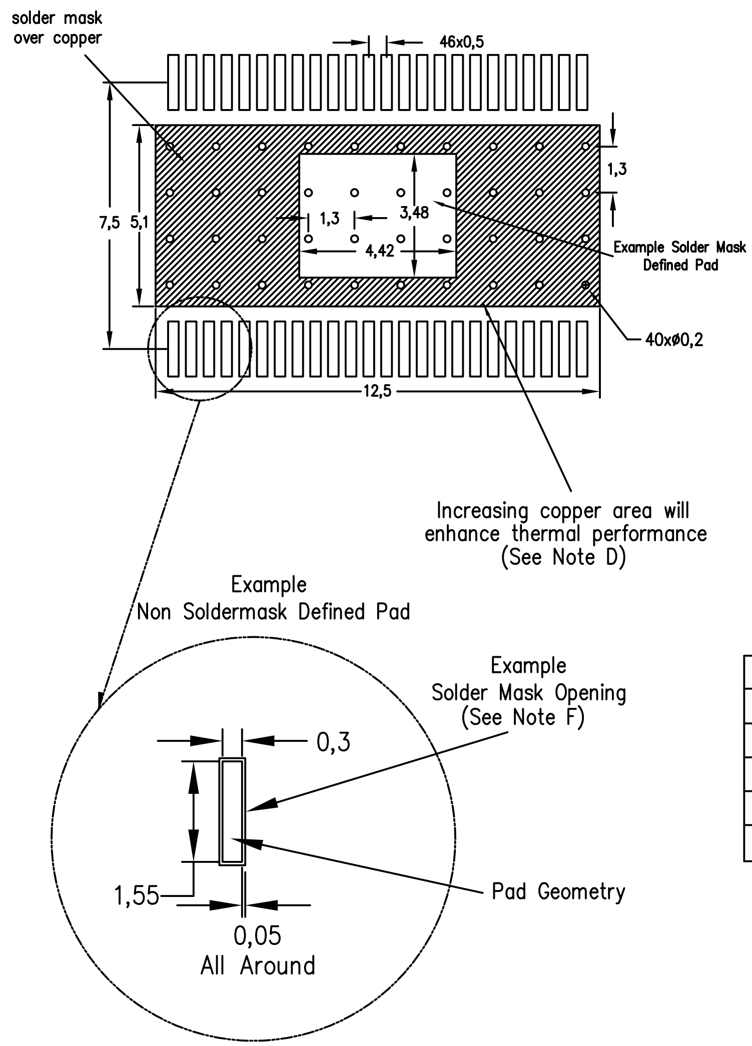
4206320–3/S 11/14

NOTE: A. All linear dimensions are in millimeters

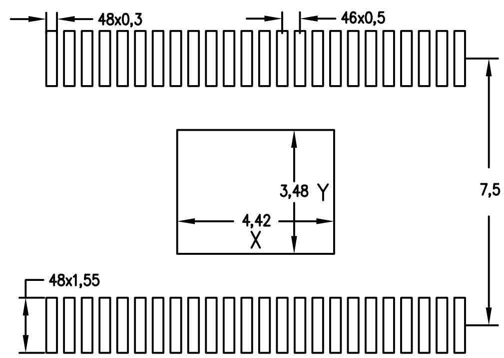
PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.98	3.92
0.127mm	4.42	3.48
0.152mm	4.04	3.18
0.178mm	3.73	2.94

4208546–2/H 11/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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